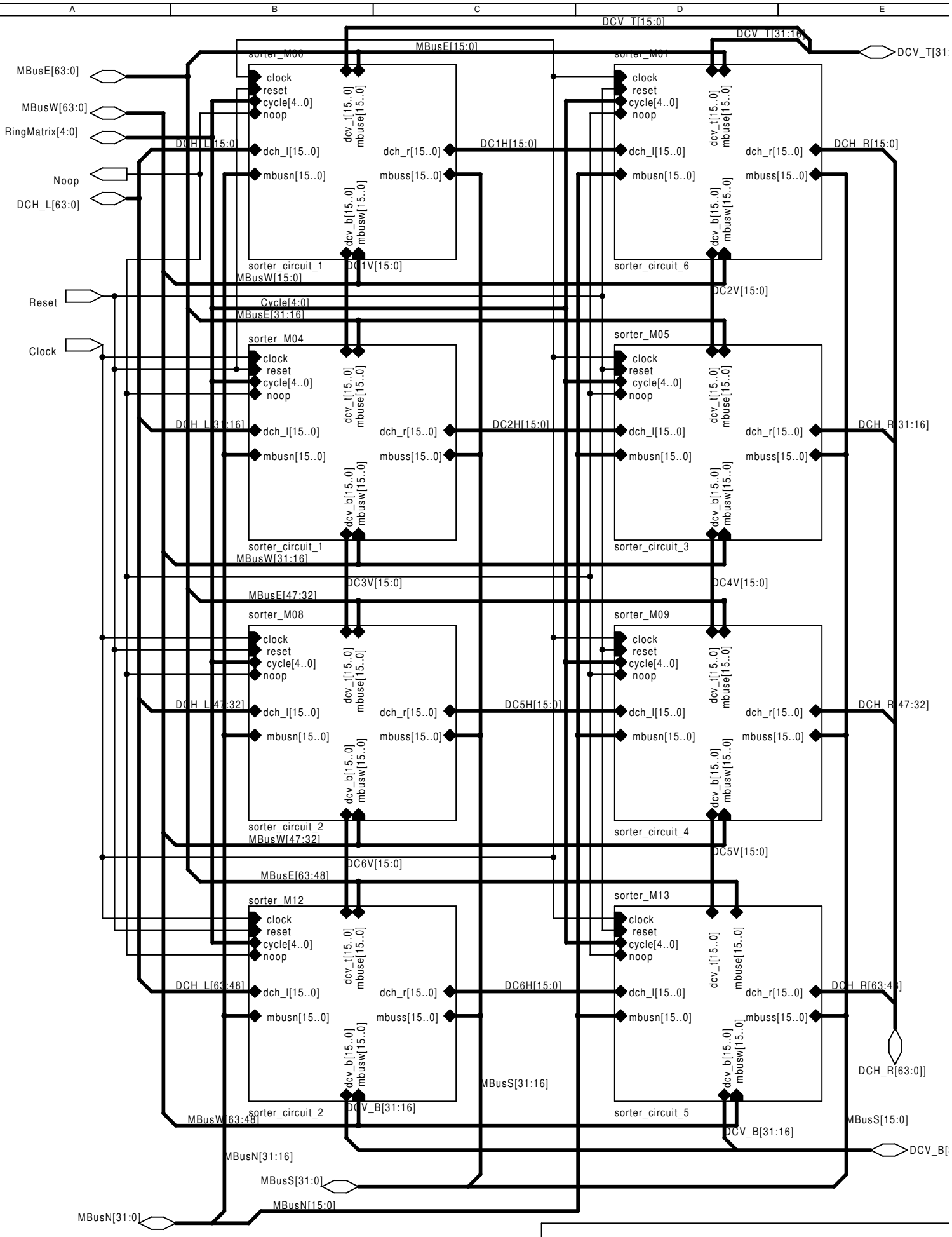
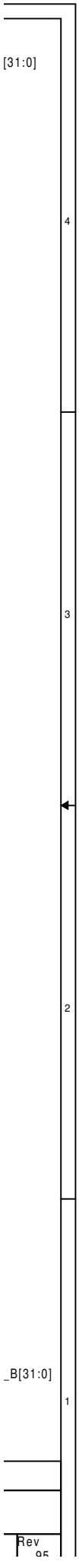

A
B
C
D
E
MBusE[63:0]
MBusW[63:0]
RingMatrix[4:0]
Noop
DCH_L[63:0]
Reset
Clock
DCV_T[15:0]
DCV_T[31:16]
DCV_T[31
MBusE[15:0]
sorter_M00
sorter_M01
clock
reset
cycle[4..0]
noop
dch_l[15..0]
dch_r[15..0]
mbusn[15..0]
mbuss[15..0]
dcv_t[15..0]
mbuse[15..0]
dcv_b[15..0]
mbusw[15..0]
DC1H[15:0]
DCH_R[15:0]
sorter_circuit_1
sorter_circuit_6
DC1V[15:0]
MBusW[15:0]
Cycle[4:0]
MBusE[31:16]
DC2V[15:0]
sorter_M04
sorter_M05
DCH_L[31:16]
DC2H[15:0]
DCH_R[31:16]
sorter_circuit_1
sorter_circuit_3
MBusW[31:16]
DC3V[15:0]
DC4V[15:0]
MBusE[47:32]
sorter_M08
sorter_M09
DCH_L[47:32]
DC5H[15:0]
DCH_R[47:32]
sorter_circuit_2
sorter_circuit_4
MBusW[47:32]
DC5V[15:0]
DC6V[15:0]
MBusE[63:48]
sorter_M12
sorter_M13
DCH_L[63:48]
DC6H[15:0]
DCH_R[63:48]
DCH_R[63:0]]
MBusS[31:16]
sorter_circuit_2
sorter_circuit_5
DCV_B[31:16]
MBusW[63:48]
MBusS[15:0]
DCV_B[
MBusN[31:16]
MBusS[31:0]
MBusN[15:0]
MBusN[31:0]
Title
FPGA Matrix Schematic
Size
Custom
Document Number
1


[31:0]
4
3
2
_B[31:0]
1
Rev
95

Size	Document Number	
Custom	1	
Date:	Friday, June 12, 1998	Sheet 1 of 1

A | B | C | D | E

Rev
.95