QUANTUM-DOT CELLULAR AUTOMATA CARRY-LOOK-AHEAD ADDER AND BARREL SHIFTER

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Abstract - The use of quantum-dots is a promising emerging technology for implementing digital systems at the nano-scale level. Recently studied computational paradigms for quantum-dot technology include the use of locally connected quantum-dot cellular automata (QCA). This technique is based on the interaction of electrons within quantum dots that take advantage of quantum phenomena; the same phenomena that may prove problematic in future integrated circuit technologies as feature sizes continue to decrease. This paper proposes layouts for a carry-look-ahead adder and barrel shifter based on QCA. The potential application in telecommunications technologies of QCA and the proposed devices is widespread and clear. By taking full advantage of the unique features of this technology, we are able to create complete circuits on a single layer of QCA. Such devices are expected to function with ultra low power consumption and very high operating speeds.

I. QUANTUM-DOT CELLULAR AUTOMATA

A QCA cell is a structure comprised of four quantum-dots arranged in a square pattern as shown in Figure 1.

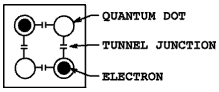

Figure 1. QCA cell

The quantum-dots within the cell provide 3D electron confinement and are capable of confining a controllable number of electrons. If the cell is charged with two excess electrons, they will tend to occupy antipodal sites as a result of their mutual electrostatic repulsion. These electrons are able to tunnel between dots if the potential barrier that separates the dots is low. Provided that the electrons will always tend to occupy antipodal sites, there are two possible configurations, which can be used to encode binary information as shown in Figure 2.

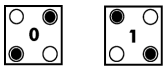

Figure 2. Binary encoding

Arrays of interacting QCA cells have been shown capable of all the logic functions required for universal digital design.[1] QCA architectures have been proposed with potential barriers between the dots that can be controlled and used to clock QCA circuits.

To date, experiments have been performed using QCA cells created from four aluminum metal islands connected via tunnel junctions made of Al/AlO_x.[4-5] Although these techniques have been used to verify the QCA concept, they suffer in that they require operating temperatures as low as 15mK. The operating temperature of QCA cells is highly dependent on the overall size of the quantum-dots. As the size of the dots shrink, the operating temperature of the cell rises. This is a result of the dependence of charging energy on dot size. To avoid problems associated with thermal fluctuations, the devices must be in an environment where the quantum-dot charging energy is much higher than the thermal energy i.e. $E_{charge} >> kT$. As nano fabrication technologies advance, the operating temperatures will rise. It is predicted that the operating temperature of QCA cells with dots that are 2nm will be above room temperature, eliminating the need for refrigeration systems.[7]

Switching in QCA is accomplished by switching the occupancy of the two electrons. Signals are carried down arrays of QCA cells as a result of the interaction of adjacent cells. The topology of the

QCA layout determines the interaction of the cells and hence the functionality of the overall circuit. The power consumption of QCA is low since only two electrons are moving.[2-3] Most of the power required by QCA circuits will be used by the clocking scheme.

QCA Clocking

The clocking of QCA can be accomplished by controlling the potential barriers between adjacent quantum-dots. When the potential is low the electron wave functions become delocalized resulting in no definite cell polarization. Raising the potential barrier decreases the tunneling rate, and thus, the electrons begin to localize. As the electrons localize, the cell gains a definite polarization. When the potential barrier has reached its highest point, the cell is said to be latched. Latched cells act as virtual inputs and as a result, the actual inputs can start to feed in new values. This enables easy pipelining of QCA circuits. It has been shown that four clocking zones each $\pi/2$ degrees out of phase is all that is required by any QCA circuit as shown in Figure 3.[8]

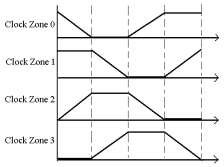

Figure 3. QCA clocking zones

These clocking zones provide a means of controlling signal propagation. This control is accomplished by attaching cells to clocking zones in such a way that they latch in succession in the direction of desired signal flow. The different clocking zones are indicated in our layouts by the different shades of gray background of the cells as shown in Figure 4

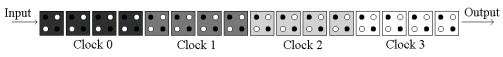

Figure 4. Different clocking zones.

QCA Logic

Adjacent QCA cells interact in an attempt to settle to a ground state determined by the current state of the inputs. This is most clear in the case of the QCA wire shown in Figure 5.

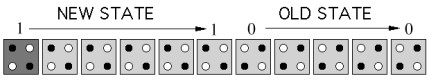

Figure 5. QCA wire

The polarization of the input cell is propagated down the wire, as a result of the system attempting to settle to a ground state. Any cells along the wire that are anti-polarized to the input would be at a higher energy level, and would soon settle to the correct ground state.

Computation with QCA is accomplished by designing QCA layouts, which exhibit the desired interaction of states. Consider the arrangements in Figure 6, demonstrating the QCA implementation of an inverter and a majority gate.

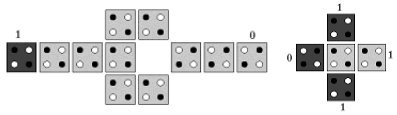

Figure 6. Inverter and majority gate

The ground state of the output cell of the above systems is a function of the shaded input cells and performs the desired logic function.

The majority gate is the fundamental QCA logic gate. The output cell will polarize to the majority polarization of the input cells. The Boolean expression for majority with inputs *a*, *b* and *c* is *m(a,b,c)=ab+bc+ca*. By fixing the polarization of any one of the inputs to the majority gate as logic 1 or logic 0, we obtain an OR gate or an AND gate respectively. Other important logic layouts are described in reference (1).

II. CARRY-LOOK-AHEAD ADDER

The University of Notre Dame first proposed the design of a QCA full adder.[1] The full adder is created from reduced majority logic. Reduction of sum of product logic to majority will almost always lead to smaller layouts. This is one of the most important advantages of QCA.

Defining the full adder using majority gates follows. Let *m(x,y,z)* be the majority function of

x,y,z. Then the carry output can be defined as follows:

$$C_{out} = a \cdot b \cdot C_{in} + a \cdot b \cdot \overline{C}_{in} + a \cdot \overline{b} \cdot C_{in} + \overline{a} \cdot b \cdot C_{in}$$
$$C_{out} = a \cdot b \cdot C_{in} + a \cdot b \cdot \overline{C}_{in} + a \cdot b \cdot C_{in} + a \cdot \overline{b} \cdot C_{in} + a \cdot b \cdot C_{in} + \overline{a} \cdot b \cdot C_{in}$$
$$C_{out} = a \cdot b \cdot (C_{in} + \overline{C}_{in}) + b \cdot C_{in} \cdot (a + \overline{a}) + a \cdot C_{in} \cdot (b + \overline{b})$$
$$C_{out} = a \cdot b + b \cdot C_{in} + a \cdot C_{in}$$
$$C_{out} = m(a,b,C_{in})$$

The majority function definition for the *Sum* output is as follows:

$$Sum = a \cdot b \cdot C_{in} + \overline{a} \cdot \overline{b} \cdot C_{in} + \overline{a} \cdot b \cdot \overline{C}_{in} + a \cdot \overline{b} \cdot \overline{C}_{in}$$
$$Sum = (a \cdot b \cdot C_{in} + \overline{a} \cdot \overline{b} \cdot C_{in}) + (a \cdot b \cdot C_{in} + \overline{a} \cdot b \cdot \overline{C}_{in}) + (a \cdot b \cdot C_{in} + a \cdot \overline{b} \cdot \overline{C}_{in})$$
$$Sum = (\overline{a} \cdot b + \overline{a} \cdot C_{in} + b \cdot C_{in})(a \cdot \overline{b} + a \cdot C_{in} + \overline{b} \cdot C_{in}) + (a \cdot \overline{b} + \overline{b} \cdot C_{in} + a \cdot C_{in})(a \cdot b + b \cdot \overline{C}_{in} + a \cdot \overline{C}_{in}) + (\overline{a} \cdot b + \overline{a} \cdot C_{in} + b \cdot C_{in})(a \cdot b + a \cdot \overline{C}_{in} + b \cdot \overline{C}_{in})$$
$$Sum = m(\overline{a},b,C_{in}) \cdot m(a,\overline{b},C_{in}) + m(a,\overline{b},C_{in}) \cdot m(a,b,\overline{C}_{in}) + m(\overline{a},b,C_{in}) \cdot m(a,b,\overline{C}_{in})$$
$$Sum = m(m(\overline{a},b,C_{in}),m(a,\overline{b},C_{in}),m(a,b,\overline{C}_{in}))$$

The full adder is a good example of a system where the majority circuit uses less logic gates than the best sum of products decomposition. The layout for a single full-adder with carry-look-ahead is shown in Figure 7.

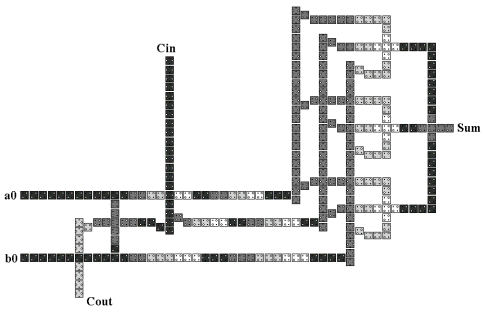

Figure 7. Full adder

To create an *n*-bit adder, we would arrange *n* such structures vertically in a column. The clocking of the cells within the circuit is designed such that the carry will propagate down to the last bit before the sum is calculated.

Unlike the Manchester Carry Chain the carry is not obtained simultaneously. But the clocking is arranged in such a way so as to obtain the *Sum* simultaneously.

The carry-look-ahead adder layout has been simulated using QCADesigner; a layout and simulation tool for QCA.[6] The simulation results for a single full adder with carry-look-ahead are shown in Figure 8.

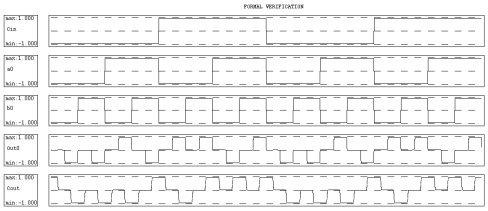

Figure 8. Simulation results for single CLA.

Using the above layout we have designed a 4-bit carry-look-ahead adder, which is shown in Figure 9.

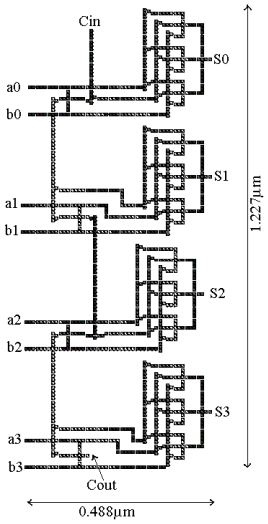

Figure 9. QCA carry-look-ahead adder

The design takes full advantage of the very unique features of QCA[1] to create the entire system on one layer. Features such as co-planer wire crossings were heavily employed to transmit signals throughout the system.

Currently, QCA technology has no specific clocking implementation that has been fully developed. As a result, we are still unsure about the

requirements of clocking structures and hence, design restrictions. In the proposed design, we tried to keep the clocking structures as simple as possible although there are areas where more complex clocking zones were required.

To maintain consistency with size measurements in previous publications, we assume that the QCA cells are made of 2nm quantum dots. The cells are separated by 10nm. The dimensions of the 4-bit design are 0.488μm x 1.227μm. This represents a clear reduction in layout size over the same design using CMOS technology.

III. BARREL SHIFTER

In this section we describe a 4-bit barrel shifter designed in QCA. The input signals can be shifted 1-4 bits depending on the applied selection signal. The design is composed of 4 shifting units each of which shifts the output by a different number of bits. The use of separate shifting units for each shift count is suitable for a small number of bits, but may be unsuitable for signals with large number of bits. The design uses a 2-to-4 bit QCA decoder to select the appropriate shifting unit. Once activated, the incoming bits are shifted. The output of the barrel shifter is generated by collecting the output of the shifting units using series connected OR gates made by fixing one of the inputs to the majority gate to 1. The design assumes that all shifting units output 0 unless selected. The shifting unit, decoder and serial OR array are described below.

Again, we made an effort to maintain simple clocking zone structures.

Shifting Unit

The layout of the individual shifting unit is shown in Figure 10.

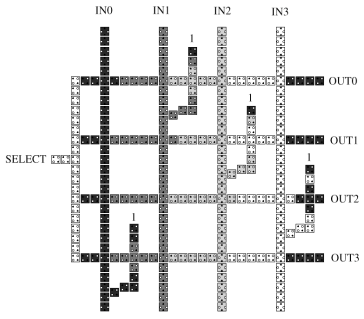

Figure 10. Shifting unit

When selected, the input lines are fed to the appropriate output. In this example unit, we see that when selected *IN0* is transmitted to *OUT3*, *IN1* to *OUT0*, *IN2* to *OUT1*, and *IN3* to *OUT2*.

Decoder

Figure 11 shows the layout of a decoder.

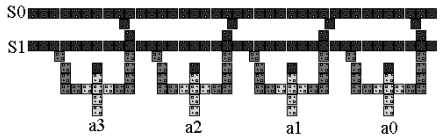

Figure 11. QCA decoder

This is a simple implementation of the decoder circuit. The two control lines *S0* and *S1* run as inversion chains.[1] These signals are tapped off at appropriate spots so as to obtain the required logic for *a0*, *a1*, *a2* and *a3*. This implementation of the decoder is close to optimal and can easily be scaled to larger circuits. The simulation results of the decoder are shown in Figure 12.

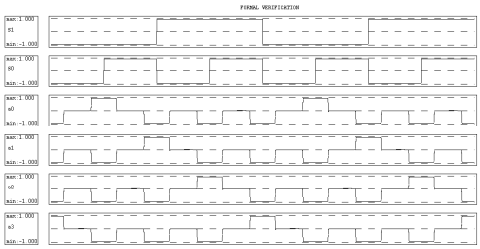

Figure 12. QCA decoder simulation results

Serial OR Array

An n-bit serial OR array is used when a particular input has to be collected from a set of *n* given inputs given that *n-1* of those inputs are forced to logic 0. The figure of a 4-bit serial OR array is shown in Figure 13.

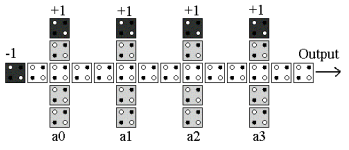

Figure 13. 4-bit serial OR array

The serial OR array is very helpful in selecting an output from a set of intermediate values of which only one value can be logic 1. This operation is typically performed using tri-state buffers, which are not available in QCA at this time.

The layout of the barrel shifter is shown in the figure below. The dimensions of the design are 0.754μm x 1.015μm using cell sizes as described in the previous section.

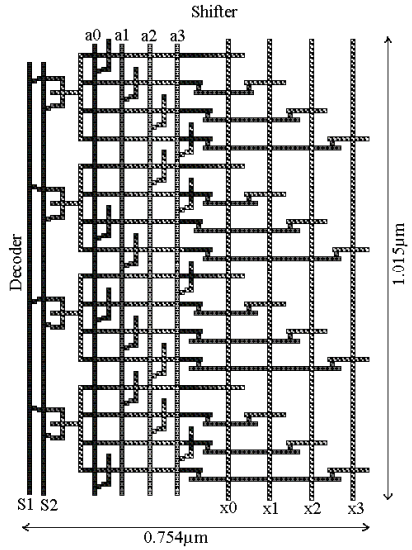

Figure 14. QCA barrel shifter

IV. CONCLUSIONS

In this work the authors have described the QCA computing paradigm and provided some detail into the current state of the technology. We have provided a brief description of switching and clocking in this technology. We have proposed a layout of a carry-look-ahead adder based on this technology. The carry-look-ahead adder is easily pipelined as a result of the clocking scheme used with QCA. We have also proposed a QCA layout for a 4-bit barrel shifter.

The proposed layouts are clearly significantly smaller than the same circuits using standard CMOS technology. The size reduction over standard CMOS is due to both the extremely small device size, as well as, the use of majority logic. The size measurements for both layouts are based on QCA cells, which are predicted to operate at room temperature. Using the unique features of QCA, we are able to layout both circuits on a single layer eliminating the requirement for complex interconnects found in CMOS.

Both designs are carefully clocked using as simple a clocking layout as possible since clocking design rules have yet to be determined. As well, both circuits were functionally verified using QCADesigner.

V. ACKNOWLEDGEMENTS

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VI. REFERENCES

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