Selecting an appropriate FPGA development board for the Image Matching Project in ECE 573 / Winter 2008

The existing project uses two 16x16 images to store the original images and an extra 16x16 image to store the result. Each image consists out of a real and an imaginary data part. Using 8 bit per pixel would mean a use of 16*16*8 bit*2 = 4k bit per Image and 12k bit over all usage. For the new project the proposed goal is to make use of 128x128 pixel images and to save memory use one of the input image to store the output image. The use of memory for the images only would already be 512k bit. Additional memory for the FFT will be used too regarding to the specification available from Altera and Xilinx.

As far as one can read out of the existing report. The author stated that the whole implementation would use up a total of 533% of the available resources in a Spartan A. He also printed the detailed usage of a Virtex 4 (XC4VLX15) with an overall usage of 177%.

XC4VLX15	Available Resources	Usage
Logic Cells	13.824	N.A.
Slices	6.144	10929 (177%)
Block Ram Bits	864k	30%
Dedicated Multipliers	N.A	N.A.

The table above shows that a device with about twice the number of Slices would be needed. Targeting an even bigger project this would not be enough. Below a table of available FPGAs from the Xilinx Spartan Series and the Altera Cylone Series which suit the requirements. Due to the fact that Altera doesn‘t use the term Slices the devices are compared by the number of Logic Cells Block Ram Bits and Dedicated Multipliers.

Device	Logic Cells/ Elements	Block Ram Bits	Multipliers
Spartan 3			
XC3S1500	29952	576k	32
XC3S2000	46080	720k	40
XC3S4000	62208	1728k	96
XC3S5000	74880	1872k	104

Device	Logic Cells/ Elements	Block Ram Bits	Multipliers
Spartan 3A / 3DSP			
XC3S1400A	25344	576k	32
XC3SD1800A	37440	1512k	84
XC3SD3400A	53712	2268k	126
Cyclone 2			
EP2C35	33216	483k	35
EP2C50	50528	594k	86
EP2C70	68416	1152k	150
Cyclone 3			
EP3C40	39600	1134k	126
EP3C55	55856	2340k	156
EP3C80	81264	2745k	244
EP3C120	119088	3888k	288

After searching through a big variety of companies with development boards the following were found suitable. Some thing which should also be kept in mind is that a RS232 with a maximum of 128k bsp speed is not capable of transferring images fast enough, a faster connection like usb will be needed.

The ‘development and education board Altera DE2-70‘ with an EP2C70 has a broad range of I/O opportunities and would be also an investment for the future when project are getting bigger and the applications more sophisticated. The I/O possibilities include USB, Ethernet, VGA, RS232, Audio line in/out, LED‘s, switches and several general I/O pins etc. The external memory includes 2Mbyte SSRAM and 32Mbyte DDR-SDRAM. The company Terasic which states on its homepage (direct link: Altera DE2-70) that a lot of education institutes use this board, sell it for 599$ and for educational users it is available for only 329$.

Another option is the ‘XtremeDSP Starter Platform - Spartan-3A‘ with an XC3SD1800. Unfortunately it has only DDR2-SDRAM and no fast and easier accessible SSRAM. It also

has less I/O possibilities and no usb controller. It is distributed from NuHorizons.com and Avnet.com for 300$.

As an conclusion this report shows that the Terasic DE2-70 has the best price performance ratio. Especially with the good documentation and sample designs available. And compared to the Xilinx board which is 29$ cheaper but it also has way less value. The Xilinx board has almost no I/O option and the used FPGA has only half the number of Logic cells and Multipliers.