Broadcast Transmission

Programmable Solutions for the Broadcast Industry
Broadcasting Standards

- Many standards across the world, existing and emerging, with just a few shown here
- However, each transmission scheme based on similar models
  - Parameterised FEC and modulation blocks will cover most requirements
- Some major standards highlighted in this presentation - contact Xilinx for more details on others
Introduction to DVB

• Digital Video Broadcasting organisation
• Formed in September 1993
• DVB now has more than 300 members
  – Broadcasters
  – Manufacturers
  – Network operators
  – Regulatory bodies
• Mission: “The creation of a harmonious digital broadcast market for all service delivery media”
• Mainly covers Europe but also promoting in U.S. and Japan
• Competes against ATSC (U.S.) and ISDB (Japan)
DVB in the Broadcast Chain

Return channels not shown
Also DVB-H emerging standard for broadcast to portables/handsets
Introduction to ATSC

- Advanced Television Systems Committee
- Formed in September 1982
- ATSC currently has around 200 members
  - Broadcasters
  - Manufacturers
  - Network operators
  - Regulatory bodies
- Co-ordinates television standards among different communications media focusing on digital television, interactive systems, and broadband multimedia communications. Also developing digital television implementation strategies
- Adopted by U.S., Canada, S. Korea, Taiwan and Argentina
Issues & Requirements

• Higher throughput
  – Particularly in cable networks, higher video/data bandwidth required

• Lower cost-per-channel
  – Support for multiple channels in less chips

• Fast time-to-market
  – Need to recoup huge infrastructure investments as soon as possible
DVB Standards for Broadcast

- DVB-S (Satellite) EN 300 421
- DVB-C (Cable) EN 300 429
- DVB-T (Terrestrial) EN 300 744
- DVB-S2 (2nd Generation Satellite) EN 302 307
- DVB-CS (Satellite Master Antenna TV/SMATV) EN 300 473
- DVB-MS (Multipoint Video Distribution Systems/MVDS) EN 300 748
- DVB-MC (Microwave Multipoint Distribution Systems/MMDS) EN 300 749
- DVB-SI (Service Information) EN 300 468
- DVB-TXT (Teletext) EN 300 472
- DVB-MHP (Multimedia Home Platform) TS 101 812
- 100 specifications/guidelines documents FOC from ETSI (including revisions)
ATSC Broadcast Standards

- ATSC Digital Television Standard
- Digital Audio Compression (AC-3) Standard
- Transmission Measurement and Compliance for Digital TV
- Conditional Access System for Terrestrial Broadcast
- Modulation & Coding Requirements for DTV Apps Over Satellite
- Data Broadcast Standard
- Delivery of IP Multicast Sessions over Data Broadcast Standard
- Around 20 specifications/guidelines documents free of charge from ATSC (inc. revisions)
- This presentation focuses solely on standard A/53B
  - ATSC Digital Television Standard
DVB/ATSC Features

• Cable
  – High bitrate, stationary receivers
  – High bitrate interactivity
  – Interactivity mostly using cable modem
  – 8MHz cable channel with DVB-C gives approx 38-40MBits/s
  – 6MHz cable channel with ATSC gives 38.57MBits/s

• Satellite
  – High bitrate, stationary receivers
  – Low bitrate interactivity currently
  – Interactivity mostly using PSTN although DVB-RCS (Return Channel for Satellite) is emerging
  – 36 MHz satellite transponder with DVB-S gives approx 40MBits/s

• Terrestrial
  – Medium or low bitrate, portable or mobile receivers
  – Low bit-rate interactivity
  – Interactivity mostly using PSTN, but DVB-T return channel systems may appear
  – 8MHz terrestrial channel with DVB-T offers around 4-27 MBits/s
DVB-C Transmitter/Receiver

- Multiplexed MPEG Transport Stream
- Mux Adaptation, Energy Dispersal
- Reed-Solomon Coder
- Convolution Interleaver
- Byte to m-tuple Conversion
- Reed-Solomon Decoder
- Convolution Deinterleaver
- Reed-Solomon Decoder
- SYNC Inversion & Energy Dispersal Removal
- Symbol to Byte Mapping
- Convolution Demodulation
- Matched FIR Filter & Equalizer
- Differential Decoding
- RF Conversion
- QPSK/QAM Modulation
- Baseband Shaping FIR Filter
- Differential Encoding

RF Cable Channel

- Non-Xilinx
- Memory
- CPU
- Embedded
- Xilinx
DVB-S Transmitter/Receiver

- Multiplexed MPEG Transport Stream
- Mux Adaptation, Energy Dispersal
- Reed-Solomon Coder
- Convolution Interleaver
- Inner Coder
- Baseband Shaping FIR Filter
- QPSK Modulation
- RF Conversion
- RF Conversion
- QPSK Demodulation
- Matched FIR Filter
- Inner Decoding
- Convolution Deinterleaver
- Reed-Solomon Decoder
- SYNC Inversion & Energy Dispersal Removal
- Multiplexed MPEG Transport Stream

Xilinx Memory CPU
Non-Xilinx Mixed Signal Embedded
DVB-T Transmitter/Receiver

Multiplexed MPEG Transport Stream

- Mux Adaptation, Energy Dispersal
- Reed-Solomon Coder
- Convolution Interleaver
- Inner Coder
- Inner Interleaver
- Mapper
- Frame Adaptation, Pilot & TPS Insertion
- OFDM Inverse FFT
- Guard Interval Insertion
- Baseband Shaping FIR Filter
- RF Conversion
- Aerial
- RF Conversion
- Guard Interval Removal
- OFDM Removal FFT
- Pilot/TPS Removal & Frame Adaptation
- Remapper
- Inner Deinterleaver
- Inner Decoder
- Convolution Deinterleaver
- Reed-Solomon Decoder
- SYNC Inversion & Energy Dispersal Removal
- Multiplexed MPEG Transport Stream
ATSC Cable Tx/Rx

MPEG Transport Stream → Data Randomizer → Reed-Solomon Encoding → Data Interleaver → Mapper → Mux → Pilot Insertion → 16VSB Modulator → RF Up-converter → RF Cable Channel

Segment Sync → RF Down-converter → 16VSB Demodulator → Pilot Removal → Demux → Field Sync

RF Cable Channel

Unmapper → Data Deinterleaver → Reed-Solomon Decoding → Data Derandomizer → MPEG Transport Stream
Basic DAB Transmitter

1. FIC (Fast Information)
2. Service Information
3. MPEG Layer-II Audio Encoder
4. Optional Conditional Access Scrambler
5. Energy Dispersal Scrambler
6. Convolutional Encoder
7. Time Interleaver
8. Main Service Multiplexer
9. Transmission Frame Multiplexer
10. OFDM Modulator
11. Multiple transmission channels
12. Forward Error Correction
Energy Dispersal Scramblers

Initialisation Code

DAB Polynomial \( P(X) = X^9 + X^5 + 1 \)

- Ensures that ratio of 0’s and 1’s transmitted is fairly equal
- Negligible FPGA resource (1 or 2 CLBs)
  - Particularly with use of SRL16E
Shift Register LUT - SRL16E

- Reading of flip-flop contents is completely independent
  - Address selects which flip-flop is read
- Read process is asynchronous, but dedicated flip-flop is available for synchronization

LUT4

INIT=1234

Becomes

SRL16E

INIT=1234

D, CE, A3, A2, A1, A0

Q

0000 1111

D, CE

A[3:0]

Q
Xilinx Reed-Solomon

- Parameterizable encoder and decoder cores available from Xilinx
- Select DVB or ATSC from the Code Specification menu
- Reed-Solomon tutorials online at Xilinx IP Centre http://www.xilinx.com/ipcenter
- Incorporates Smart-IP
## Xilinx R-S Features

### Reed-Solomon

<table>
<thead>
<tr>
<th>Features</th>
<th>ATSC 1</th>
<th>DVB 1</th>
</tr>
</thead>
<tbody>
<tr>
<td>Symbol Width</td>
<td>N/A</td>
<td>N/A</td>
</tr>
<tr>
<td>Generator Start</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>$R$</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>$k$</td>
<td>187</td>
<td>188</td>
</tr>
<tr>
<td>$n$</td>
<td>207</td>
<td>204</td>
</tr>
<tr>
<td>Field Polynomial</td>
<td>285</td>
<td>285</td>
</tr>
<tr>
<td>Optimization</td>
<td>Speed</td>
<td>Speed</td>
</tr>
<tr>
<td>Create RPM</td>
<td>No</td>
<td>No</td>
</tr>
<tr>
<td>Xilinx Device</td>
<td>X2VP2-FG256-7</td>
<td>X2VP2-FG256-7</td>
</tr>
<tr>
<td>Use IOB Flip-Flop</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td>Area (Slices)</td>
<td>121</td>
<td>109</td>
</tr>
<tr>
<td>Slices Remaining</td>
<td>1287</td>
<td>1299</td>
</tr>
<tr>
<td>Block Memory</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>Latency</td>
<td>3</td>
<td>3</td>
</tr>
<tr>
<td>Maximum Clock Frequency</td>
<td>311 MHz</td>
<td>299 MHz</td>
</tr>
</tbody>
</table>

### Decoder

<table>
<thead>
<tr>
<th>Features</th>
<th>ATSC 1</th>
<th>DVB 1</th>
</tr>
</thead>
<tbody>
<tr>
<td>Generator Start</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>$R$</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>$k$</td>
<td>187</td>
<td>188</td>
</tr>
<tr>
<td>$n$</td>
<td>207</td>
<td>204</td>
</tr>
<tr>
<td>Polynomial</td>
<td>285</td>
<td>285</td>
</tr>
<tr>
<td>Symbol Width</td>
<td>8</td>
<td>8</td>
</tr>
<tr>
<td>Sync Mode</td>
<td>Start Pulse</td>
<td>Start Pulse</td>
</tr>
<tr>
<td>Clock Enable</td>
<td>No</td>
<td>No</td>
</tr>
<tr>
<td>Synchronous Reset</td>
<td>No</td>
<td>No</td>
</tr>
<tr>
<td>Delayed Original Data</td>
<td>No</td>
<td>No</td>
</tr>
<tr>
<td>Erasure Decoding</td>
<td>No</td>
<td>No</td>
</tr>
<tr>
<td>Optimization</td>
<td>Area</td>
<td>Area</td>
</tr>
<tr>
<td>Clock Periods Per Symbol</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>Memory Style</td>
<td>Automatic</td>
<td>Automatic</td>
</tr>
<tr>
<td>Processing Delay</td>
<td>294</td>
<td>204</td>
</tr>
<tr>
<td>Latency</td>
<td>507</td>
<td>414</td>
</tr>
<tr>
<td>Xilinx Device</td>
<td>2VP2-FG256-7</td>
<td>2VP2-FG256-7</td>
</tr>
<tr>
<td>Area (Slices)</td>
<td>783</td>
<td>618</td>
</tr>
<tr>
<td>Slices Remaining</td>
<td>625</td>
<td>790</td>
</tr>
<tr>
<td>Block Memories</td>
<td>2</td>
<td>2</td>
</tr>
<tr>
<td>Maximum Clock Frequency</td>
<td>126 MHz</td>
<td>128 MHz</td>
</tr>
</tbody>
</table>
Xilinx Interleaver/Deinterleaver

- Forney convolutional type architecture
- Parameterizable number of branches and branch lengths
- Symbol size from 1 to 256 bits
- Incorporates Smart-IP
- More info at http://www.xilinx.com/ipcenter
# Xilinx (De)Interleaver Features

<table>
<thead>
<tr>
<th>Options</th>
<th>DVB 1</th>
<th>DVB 2</th>
</tr>
</thead>
<tbody>
<tr>
<td>Mode</td>
<td>Interleaver</td>
<td>De-interleaver</td>
</tr>
<tr>
<td>Number of Branches</td>
<td>12</td>
<td>12</td>
</tr>
<tr>
<td>Branch Length Constant</td>
<td>17</td>
<td>17</td>
</tr>
<tr>
<td>Symbol Width</td>
<td>8</td>
<td>8</td>
</tr>
<tr>
<td>Pipelining</td>
<td>Maximum</td>
<td>Maximum</td>
</tr>
<tr>
<td>Optional Pins</td>
<td>FDO, RDY, RFFD</td>
<td>FDO, RDY, RFFD</td>
</tr>
<tr>
<td>Memory Style</td>
<td>Automatic</td>
<td>Automatic</td>
</tr>
<tr>
<td>Create RPM</td>
<td>No</td>
<td>No</td>
</tr>
<tr>
<td>Xilinx Device</td>
<td>XC2V40-6</td>
<td>XC2V40-6</td>
</tr>
<tr>
<td>Use IOB Flip-Flops</td>
<td>No</td>
<td>No</td>
</tr>
<tr>
<td>Area (slices)</td>
<td>80</td>
<td>109</td>
</tr>
<tr>
<td>Number of Block RAMs</td>
<td>1</td>
<td>2</td>
</tr>
<tr>
<td>Maximum Clock Frequency</td>
<td>208 MHz</td>
<td>187 MHz</td>
</tr>
</tbody>
</table>
Xilinx Convolutional Encoder

- Parameterizable constraint length from 3 to 9
- Parameterizable convolutional codes and puncture codes
- Puncturing Rates from 2/3 to 12/13
- Incorporates Smart-IP
- More info at http://www.xilinx.com/ipcenter
## Convolutional Encoder Features

<table>
<thead>
<tr>
<th></th>
<th>Output Rate=2</th>
<th>Output Rate = 3</th>
<th>Output Rate = 6</th>
<th>Output Rate=7</th>
</tr>
</thead>
<tbody>
<tr>
<td>Constraint Length</td>
<td>7</td>
<td>7</td>
<td>7</td>
<td>7</td>
</tr>
<tr>
<td>Create RPM</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td>Xilinx Part</td>
<td>XC2V40-6</td>
<td>XC2V40-6</td>
<td>XC2V40-6</td>
<td>XC2V40-6</td>
</tr>
<tr>
<td>Area (slices)</td>
<td>7</td>
<td>8</td>
<td>11</td>
<td>12</td>
</tr>
<tr>
<td>Maximum Clock Frequency</td>
<td>517MHz</td>
<td>515MHz</td>
<td>505MHz</td>
<td>463MHz</td>
</tr>
</tbody>
</table>
Xilinx Viterbi Decoder

- General Purpose Parameterizable Netlist
- IEEE802-Compatible Source Code & Netlist
- Parameterizable generator polynomials, puncture rates and constraint lengths
- Built-in BER monitor
- IEEE802-compatible core also supports
  - Best State Calculation for lower latency and improved BER
  - Latency less than 2 microseconds for packet/burst type modems
  - Data rates up to 155Mbps with a single decoder
  - Trellis Coded Modulation
- For more details:
  http://www.xilinx.com/ipcenter
# Viterbi Decoder Features

<table>
<thead>
<tr>
<th>Feature</th>
<th>IEEE 802-Compatible</th>
<th>IEEE 802-Compatible Fixed Nelist</th>
<th>General Purpose Parameterizable Nelist</th>
</tr>
</thead>
<tbody>
<tr>
<td>Adaptive Code Rates (via memory inputs)</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td>Additive Traceback Depth</td>
<td>Yes</td>
<td>Yes</td>
<td>No</td>
</tr>
<tr>
<td>Includes Best State Calculation</td>
<td>Yes</td>
<td>Yes</td>
<td>No</td>
</tr>
<tr>
<td>BER Monitor</td>
<td>Yes$^1$</td>
<td>Yes$^1$</td>
<td>Yes</td>
</tr>
<tr>
<td>Latency</td>
<td>2us @ fclk = 157 traceback = 96</td>
<td>2us @ fclk = 157 traceback = 96</td>
<td>3us @ fclk = 157 traceback = 96</td>
</tr>
<tr>
<td>Parallel/serial Option</td>
<td>No</td>
<td>No</td>
<td>Yes</td>
</tr>
<tr>
<td>Constraint Length (K)</td>
<td>K = 7</td>
<td>K = 7</td>
<td>Parameterizable (3 to 8)</td>
</tr>
<tr>
<td>Generator Polynomials</td>
<td>G0 = 171, G1 = 133; G0 = 133, G1 = 171</td>
<td>G0 = 171, G1 = 133; G0 = 133, G1 = 171</td>
<td>Parameterizable</td>
</tr>
<tr>
<td>Decoder Rate</td>
<td>1/2</td>
<td>1/2</td>
<td>Parameterizable (1/2 to 17)</td>
</tr>
<tr>
<td>Dual Rate</td>
<td>No</td>
<td>No</td>
<td>Parameterizable, rate &amp; code selectable via select pins</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Feature</th>
<th>IEEE 802-Compatible</th>
<th>IEEE 802-Compatible Fixed Nelist</th>
<th>General Purpose Parameterizable Nelist</th>
</tr>
</thead>
<tbody>
<tr>
<td>Trellis Code Modulation Support</td>
<td>Yes$^3$</td>
<td>Yes$^3$</td>
<td>No</td>
</tr>
<tr>
<td>Internal Puncturing Option</td>
<td>No</td>
<td>No</td>
<td>Fixed rate, selectable from 20 to 1213, Parameterizable puncture codes.</td>
</tr>
<tr>
<td>Simulation Support</td>
<td>VHDL Source</td>
<td>Gate Level</td>
<td>VHDL Behavioral Model</td>
</tr>
<tr>
<td>Proposed Applications</td>
<td>IEEE 802.11a/g-compatible fixed wireless applications such as LMDS and MMDS, Also HiperLAN2, DYK, and OC3 data rates.</td>
<td>IEEE 802.11a/g-compatible fixed wireless applications such as LMDS and MMDS, Also HiperLAN2, DYK, and OC3 data rates.</td>
<td>General purpose (Any - DVB, SGPP, etc.)</td>
</tr>
<tr>
<td>Format</td>
<td>Source Code (Parameterizable)</td>
<td>Fixed Nelist</td>
<td>Parameterizable Nelist using the CORE Generator System</td>
</tr>
</tbody>
</table>

---

Virtex V4

Spartan-3E

Viterbi

DVBT/ATSC 25
Smart-IP Technology

- Used in all Xilinx cores
- Results in predictable implementation
  - Consistent functionality and performance
  - Independent of core placement, number of cores used, surrounding user logic, device size and choice of EDA tool
- Vital for easy design of multi-channel systems
Single Frequency Networks

FPGAs widely used in WAN/MAN applications
See xilinx.com/esp/optical for more details
Multipath Signals

- Multipath or reflected signals can cause interference
- Can add constructively or destructively to main (shortest) path
- Reflections are delayed and can cause ISI (*next slide*)
- DVB/DAB solution is to use Coded Orthogonal Frequency Division Multiplex (COFDM)
Inter-Symbol Interference (ISI)

• An echo of the previously received symbol can interfere with present symbol reception

• Area of ISI is also called delay spread and for transmission to work effectively, this must be removed

• Removal is done using a number of steps......
Frequency Division Multiplexing

- FDM is a way of increasing the symbol period so that the delay spread is only a small fraction of it.
- A single high frequency carrier is divided into many lower frequency parallel carriers: up to 6817 in DVB systems.
- The carriers are orthogonal to one another - they are spaced $1/T_u$ apart where $T_u$ is the symbol period.
- FDM is implemented using an Inverse Fast Fourier Transform (IFFT) at the transmitter and a Forward FFT at the receiver.
Baseband Shaping in FPGA

- Before transmission, signals are shaped using a filter such as the Root Raised Cosine (RRC) filter.
- Maximises the use of total available bandwidth whilst also eliminating intersymbol interference (ISI).
- RRC coefficients determined using DSP tools (e.g. Matlab):
  - Designer enters required roll-off and bit rate parameters into RRC generator to produce coefficients.
  - Suggests number of taps and shows resulting waveforms for trial and error iterations.
- Final RRC coefficients simply entered into Xilinx Core Generator to build necessary FIR filter in hardware.
Xilinx Pre-Distortion System

Using a Processor For Coefficient Calculation & Tracking

Virtex-II Pro or Virtex-4 Platform FPGA

Pre-Distortion Function

Amplitude Compression
Linear Filter
Non-Linear Correction
Dual Port Memory
Filter Coefficients,
Non-Linear Transform Table
Correlation
IF to Baseband
Digital Down
Converter

DAC
RF Transmitter
Power Amp
Tx Bandpass
Filter

ADC
RF Receiver

MicroBlaze
or PowerPC
Buffer Memory

Logic
Memory
CPU
Non-Xilinx
Mixed Signal Embedded

From Channel Combiner
I
Q

System Control Bus

Antenna
DVB-S2

Second Generation Broadband Satellite Standard

• Increased system capacity over DVB-S
  – Up to 40% better satellite transponder utilization in broadcast mode
  – Up to 200% more subscribers per unit of bandwidth in interactive mode
  – Still backward compatible with DVB-S

• Improved link margin
  – Increased availability, extended coverage and enhanced robustness to noise and interference

• Flexibility to match a wide range of transponder characteristics

• Multiple input formats supported:
  – MPEG-2, MPEG-4 and HDTV transport streams
  – Generic streams of IP packets and ATM cells

• Multiple transport streams in a single modulated carrier

• Adaptive coding and modulation
DVB-S2 Nearer Shannon Limits
# DVB-S2 vs. DVB-S Example

<table>
<thead>
<tr>
<th>Satellite EIRP (dBW)</th>
<th></th>
<th>51</th>
</tr>
</thead>
<tbody>
<tr>
<td>System</td>
<td>DVB-S</td>
<td>DVB-S2</td>
</tr>
<tr>
<td>Symbol-rate MBaud</td>
<td>27.5 ((\alpha=0.35))</td>
<td>30.9 ((\alpha=0.20))</td>
</tr>
<tr>
<td>Modulation &amp; coding</td>
<td>QPSK 2/3</td>
<td>QPSK 3/4</td>
</tr>
<tr>
<td>(C/N=5.1dB@27.5 MHz)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Useful bit-rate Mbit/s</td>
<td>33.8</td>
<td>46 (gain 39%)</td>
</tr>
<tr>
<td>Number of SDTV programmes (*)</td>
<td>7 MPEG-2; 15 AVC</td>
<td>10 MPEG-2; 21 AVC</td>
</tr>
<tr>
<td>Number of HDTV programmes (*)</td>
<td>1-2 MPEG-2; 3-4 AVC</td>
<td>2 MPEG-2; 5 AVC</td>
</tr>
</tbody>
</table>
Multiple Muxes to DTT Tx

1. TV coder
   - DTT MUX 1
   - Input Interface
   - Input Stream Sync
   - CRC
2. TV coder
   - DTT MUX 2
   - Input Interface
   - Input Stream Sync
   - CRC

DVB-S2 Modulator
- Mode adapter
- Mージン

QPSK rate 5/6
- Stream Adapter
- FEC Coder
- Mod

Constant Coding & Modulation
IP Services over DVB-S2
DVB-S2 Standard

Dotted sub-systems are not relevant for single transport stream broadcasting applications.
Xilinx DVB-S2 FEC Solution

<table>
<thead>
<tr>
<th>Width (W)</th>
<th>Slices</th>
<th>Block RAM</th>
<th>MULT 18x18</th>
<th>Max. Clock Frequency (MHz)</th>
<th>Maximum Encoded Output Rate bits/s</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>430</td>
<td>19</td>
<td>1</td>
<td>230 200 170</td>
<td>230 200 170</td>
</tr>
<tr>
<td>2</td>
<td>600</td>
<td>19</td>
<td>2</td>
<td>230 200 170</td>
<td>460 400 340</td>
</tr>
</tbody>
</table>
J.83 in the Broadcast Chain

Cable Headend

- Web & Application Servers
- Receivers
- MPEG Encoders
- Remultiplexers (StatMuxes)
- Backplane (e.g. Fibre Channel)
- CMTS Router
- Video Servers
- Modulators/Transmitters

Customer Premise

- Cable Modem
- Set Top Box

Internet

TV Broadcast

Xilinx DOCSIS ITU-T J.83 Modulator Solution
J.83 Annex A/B/C Modulators

- J.83 Annex A/C, DVB-C, DVB-MC(EN 300 749), DAVIC, IEEE 802.14 compliant
- Designs may be used in one of two footprints
  - Single Channel : group of 1
  - Four Channel : group of 4
- Multi-channel designs may be constructed out of either granularity
Single Channel J.83 Annex B Modulator
Four Channel J.83 Annex B Modulator
Single Channel J.83
Annex A/C Modulator

Single Channel Granularity of a Group
Four Channel J.83 Annex A/C Modulator

Four Channel Granularity of a Group
Multi-Channel Design

- 1 Group = 1 or 4 channels
- M = #groups per memory
- N = #channels/#memory
- M,N dependent on the max clock speed of the memory and design clock speed.
Additional J.83 Info

• **Multi-channel Design**
  – Granularity of 1 or 4 channels
  – Common Control Parameters for 4 channel granularity
    • Runtime QAM Selection (64 or 256)
    • Runtime Interleaver Switching (16 possible cases)

• **Interface to External Memory for Interleaver**
  – ZBT SRAM (Micron’s ZBT SRAM based controls signals)
  – 7(28) bits memory width for granularity of 1(4)

• **Clock Management Scheme included**
  – Soft as well as Hard Reset for the design
  – Separate Soft reset for each group
  – Single Hard reset for the design

• **Optional RRC Filter provided**

• **Design Source is in combination of sysgen files (.mdl,.m) plus vhdl and .edn**

• **Design will be delivered as set of vhdl and .edn files**
Xilinx DOCSIS J.83 A/B/C

Key Features & Benefits

- **Unprecedented levels of integration**, driving down the cost per channel
- **Variable input symbol rates**, providing support for multiple types of input streams such as MPEG-2 or ATM packets
- **Single and multi-channel solutions**, delivering the optimal integration and flexibility for multi-channel designs in a Virtex-II Pro
  - Multi-channel design leverages unique Xilinx silicon features such as the SRL16, resulting in compact implementation
- **Programmable 64 and 256 QAM modulation**, conforming to the J.83 Annex B specification
- **Variable interleaver and parameterized RRC** filter as defined in the J.83 Annex B specification
- Common controls for multi-channel design, providing efficient resource sharing
- **Supported in the popular System Generator for DSP** software platform design
- Less than $3* per channel in a Spartan-3, providing an extremely low cost solution
Xilinx DOCSIS J.83 A/B/C

More Key Features & Benefits

• Higher Flexibility
  – Designers don’t always want entire solution (differentiate)
  – ASSP limits what the customer can do
  – FPGA enables the designer to create a customized solution around the Xilinx Modulator
    • Customer gets System Generator for DSP model
    • Fully Parameterizable

• Lower Cost
  – Lower price per channel
  – We believe Xilinx to be lower by at least a factor of 2
DAB MPEG Encoder Flow Chart

- Majority of tasks designed for microprocessor

This part used only in joint stereo mode
Flexible Embedded Processing

**PicoBlaze**

- 8-bit Microcontroller
- Simple state-machines and “localised” on-chip control
- Pixel processing & display control

**MicroBlaze PowerPC™**

- 32-bit Microprocessors
- Cost/performance tradeoffs
- Extensive peripherals, RTOS & bus structures
- Networking & wireless comms, control & instrumentation
MPEG Synthesis Subband Filter

- Well suited to parallel FPGA structure
- Increased performance from dedicated hardware co-processing
- Support parallel DAB frame processing on one device
Why FPGAs for Transmission?

High Computational Workloads

256-tap Filter Example

Conventional DSP Processor - Serial

- Data In
- Coefficients
- MAC Unit
- 256 loops needed to process samples
- Data Out

\[
\text{1 GHz} \quad \frac{256 \text{ clock cycles}}{} = 4 \text{ MSPS}
\]

FPGA-based DSP - Parallelism

- Data in
- C0, C1, C2, C3, C4, C5, C6, C7, C254, C255
- Data out

\[
\text{500 MHz} \quad \frac{1 \text{ clock cycle}}{} = 500 \text{ MSPS}
\]
Virtex-4 FPGAs Enable New Development Paradigm

- Ability to run hardware and software in-situ at speed, with real-time observability & debug
- Ability to provide dedicated hardware to all software developers early and at low cost
- Ability to adjust hardware/software tradeoff
  - During definition
  - During debug
  - After shipment
HW/SW Partition Example

DVB-S2 FEC & Modulation (in FPGA Fabric)

- Mode Adapt
- Stream Adapt
- BCH
- LDPC
- Interleave
- Mapper
- Framing
- Modulator

Medium Access Controller (in Software on PowerPC)

Gigabit Network Interface
Xtreme Forward Error Correction

FEC Engine (fabric/multipliers)

PowerPC with Application-Specific Hardware Acceleration

XTREME Processing™

The Virtex-4 Advantage

Traditional

Processing time
Multiple Channels on the Platform FPGA

- Think 3D rather than 2D when designing
  - Reuse resources by multiplexing if extra horsepower available
    - e.g. If running half the max speed of FPGA, you could do twice as much in same period
  - Support multiple channels in less FPGA resources than you’d expect
XDS Case Study

The XDS Advantage

<table>
<thead>
<tr>
<th>The XDS Advantage</th>
<th>Customer's Original Design</th>
<th>XDS Solution</th>
</tr>
</thead>
<tbody>
<tr>
<td>Device Required</td>
<td>Virtex XCV2600E-6BG1156</td>
<td>Virtex XCV400E-6BG676</td>
</tr>
<tr>
<td>Cost*</td>
<td>$12X</td>
<td>$X</td>
</tr>
</tbody>
</table>

- Xilinx Design Services (XDS) solution delivered >90% savings on device price over original design!
  - Relatively slow speed of four paths through FPGA allowed multiplexing
- Use of Xilinx FPGA enabled customer to prototype their product within 4 months
- Customer able to recover one-time development cost before prototype completion
- Engaging XDS enabled customer to develop successful product with viable cost structure and faster time-to-market

*(100+ pricing for comparative purposes only)
Example DVB Receiver System

For more detailed presentations on set top boxes & receivers, check out www.xilinx.com
Conditional Access

• Three key parts to Conditional Access (CA)
  – Scrambling/Descrambling
    • Making the service incomprehensible to unauthorised users
  – Entitlement Checking
    • Providing the access requirement information to users
    • Providing a decryption key to authorised users
  – Entitlement Management
    • Distributing entitlements to receivers

• Xilinx is extremely successful in cryptography (DES, TDES & AES)
  – Relatively low device utilisation and high (Gigabit/s) throughput
  – Faster than any software!
  – Programmable: able to update regularly and on-the-fly
  – Extra level of security can be added as a wrapper
Xilinx Cryptography Solutions

• Spartan-3 encryption solutions are NIST approved
• The programmable nature of these solutions allows easy customization based on end application requirement

<table>
<thead>
<tr>
<th></th>
<th>DES</th>
<th>Spartan-IIIE Solution</th>
<th>AES</th>
<th>AES</th>
</tr>
</thead>
<tbody>
<tr>
<td>Device</td>
<td>2S100E-6</td>
<td>2S150E-6</td>
<td>2S100E-6</td>
<td>2S100E-6</td>
</tr>
<tr>
<td>CLB Slices</td>
<td>235</td>
<td>1611</td>
<td>358*</td>
<td>231**</td>
</tr>
<tr>
<td>Performance</td>
<td>94 MHz</td>
<td>48 MHz</td>
<td>82 MHz</td>
<td>82 MHz</td>
</tr>
<tr>
<td>Area Utilization</td>
<td>19.58%</td>
<td>93.22%</td>
<td>29.83%</td>
<td>19.25%</td>
</tr>
<tr>
<td>Key Size</td>
<td>56-bit</td>
<td>128-bit or two 64-bit</td>
<td>128/192/256-bit</td>
<td>128/192/256-bit</td>
</tr>
</tbody>
</table>

AES aims to replace DES over long term
Program now with DES and replace with AES later via network

Note: Solution includes encryption, decryption and key generation * 128-bit key implementation ** Key Generation offloaded to embedded µC/µP
DVB-RCS Turbo Decoder Core

- Interactive **Return** Channel for **Satellite** customers
- Xilinx Alliance core partner iCODING offers high performance, flexible solution based on turbo coding error correction
  - Fast time-to-market
  - Updateable if the new standards change during development

### Supported Family

<table>
<thead>
<tr>
<th>Supported Family</th>
<th>Device Tested</th>
<th>CLB Slices</th>
<th>Clock IOBs(^1)</th>
<th>IOBs(^1)</th>
<th>Performance (MHz)</th>
<th>Xilinx Tools</th>
<th>Special Features</th>
</tr>
</thead>
<tbody>
<tr>
<td>Virtex-II</td>
<td>2V2000-5</td>
<td>5801</td>
<td>1</td>
<td>35</td>
<td>69</td>
<td>3.3i</td>
<td>15 BlockRAMs</td>
</tr>
<tr>
<td>Virtex-E</td>
<td>V2000E-8</td>
<td>5265</td>
<td>1</td>
<td>35</td>
<td>43</td>
<td>3.3i</td>
<td>29 BlockRAM</td>
</tr>
</tbody>
</table>

**Notes:**

1. Assuming all core I/Os are routed off-chip
Time-to-Market Value

Quicker time to market and reprogrammability provide the best chance of achieving full product profit potential.
Transmitter Solutions

• Xilinx offers IP solutions for
  – Forward Error Correction (FEC)
  – Content encryption and energy dispersal scrambling
  – COFDM modulator and baseband shaping

• Integration of multiple channels on single device
  – Lower BOM
  – Lower cost-per-channel

• Higher performance with XtremeDSP
  – Increased bandwidth and more from available bandwidth
  – Reduce size of “DSP farms”

• Total flexibility
  – Fast time-to-market and differentiation
  – Tuneable solution to different broadcast requirements
Receiver Solutions

• Xilinx CPLDs and FPGAs provide time-to-market and flexibility advantages for receiver systems
  – Quickly interface receiver chipsets to host processor without waiting for ASSP/ASIC re-spin
  – Or add extra features to receiver units, like hard drive or smart card reader

• Ease of integration
  – Small packaging and minimal thermal impact

• Power saving benefits without performance sacrifice
  – Operating mode and battery management
  – Support higher automotive voltages or lower consumer voltages

• Adds additional performance
  – Reduce processor workload by handling interfaces
  – Expand microprocessor I/O
Xilinx Transmission Solutions

- Xilinx offers programmable solutions at all digital stages of the DVB, ATSC, ISDB, DMB & DAB transmit and receive chains
- Multi-channel support available on one chip
  - Parameterisable FEC cores available now
- Plenty of gates available for “back-end” designs and value add functions for complete system-on-chip solution
  - Other DSP blocks including filters and image processing cores
  - Network interface cores available
- Reprogrammability also gives flexibility
  - Faster time-to-market
  - Longer time-in-market
- Xilinx Design Services can help for bespoke solutions
Xilinx in the Broadcast Chain

- Gamma Correction
- Codecs
- Scaling/Resampling
- Colour Space
- Network Interfacing
- Chip Interfacing
- Video Filtering
- Effects (Wipe/Key)
- Memory Control
- FEC/Modulation
- System Control
Real Time HD/Multichannel DSP

- Highest performance on-chip DSP blocks, multipliers and memory
- Reduce size of DSP farms
- Support real time HD processing
- Support multiple channels of SD processing through resource sharing
- Reduce cost-per-channel for FEC and modulation
Cost Effective Connectivity

- Significant cost-per-channel reductions
- Portfolio of audio/video connectivity solutions
  - SDI, HD-SDI and DVB-ASI
  - Video-over-IP
- Wide range of general telecom, datacom and backplane solutions available
  - Ethernet, PCI Express, ATM, Fibre Channel, SONET, SPI RapidIO, HyperTransport...

~70% cheaper than ASSP SDI solutions!
Flexible Embedded Processing

**PicoBlaze™**

- 8-bit Microcontroller
- Simple state-machines and “localised” on-chip control
- Pixel processing & display control

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- 32-bit Microprocessors
- Cost/performance tradeoffs
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- Networking & wireless comms, control & instrumentation
Xilinx in Broadcast

Programmable Solutions for the Broadcast Industry

Interfaces & Connectivity  Codecs  Video & Audio Processing  Transmission & Reception  End Applications

More info on a wide range of applications and technologies

www.xilinx.com/broadcast