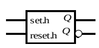
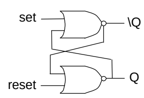
0 Admin
1 Recap
2 FF – edge triggered
3 FSM design methodology
4 FSM design examples

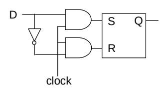
1 Recap

- Set-reset latch:





- D-type latch



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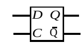
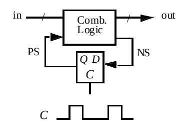
2. D latch/D FF



level sensitive at transparent latch when
$c = 1, Q = D$
$c = 0, Q_{n+1} = Q_n$

Can we use this in Finite State Machine?



Problem?

"Race" since Q follows D and logic probably has glitches.

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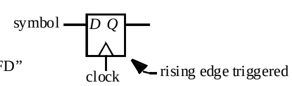
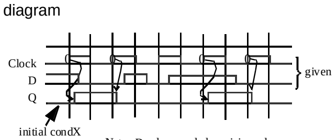
2. D FF (cont.)

2.1 Edge triggered D Flip Flop



Timing diagram



Note: *D* only sampled on rising edge, ignored otherwise

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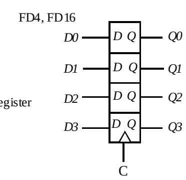
2. D FF (cont.)

2.2 N bit register made from D FF



Use as state register in FSM

3. FINITE STATE MACHINE (FSM)

If N bit register, has 2^N possible states.
state space: set of total unique values of memory

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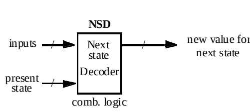
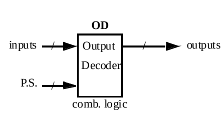
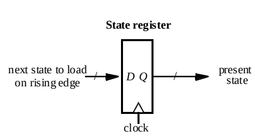
3. FSM (cont.)

3.1 Pieces of FSM







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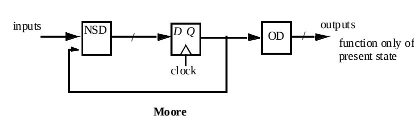
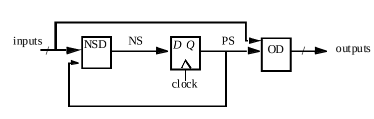
3. FSM (cont.)

3.2 Moore and Mealey FSM



Moore



Mealey

3. FSM (cont.)

3.3 Design method for FSM:

1 identify inputs and outputs (basic block diagram)

2 sketch operation (timing diagram/flow chart) understand problem specification!

3 choose machine type (Mealey/Moore)

4 draw state diagram/assign states

5 construct state transition table

6 simplify and implement

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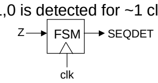
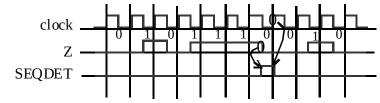
4. EXAMPLE: FSM DESIGN

4.1 Design a Mealey machine that can detect any sequence of "1 followed by 1 followed by 0" on input Z. Output SEQ.DET.H should be asserted as soon as any 1,1,0 is detected for ~1 clock. Input data changes after ↑ of clock.



4.2 Make up data 0,1,0,1,1,1,0,0,1



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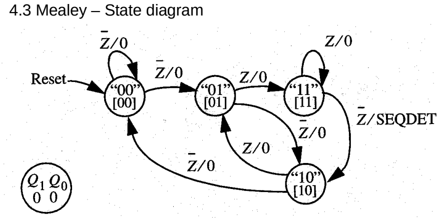
4. EXAMPLE FSM DESIGN

4.3 Mealey – State diagram



Notation (Mealey): Z/SEQDET, where Z are the input variables and SEQDET are the outputs

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4. EXAMPLE: FSM DESIGN (cont.)

4.4 State Transition Table

Present state		Input	Next state		Output
Q_1	Q_0	Z	Q_1 (= D_1)	Q_0 (= D_0)	SEQDET
0	0	0	0	0	0
0	0	1	0	1	0
0	1	0	1	0	0
0	1	1	1	1	0
1	0	0	0	0	0
1	0	1	0	1	0
1	1	0	1	0	1
1	1	1	1	1	0

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4. EXAMPLE: FSM DESIGN (cont.)

4.5 Simplify and implement

$$\text{SEQDET} = Q_1 Q_0 \cdot \overline{Z}$$

$$Q_0^+ = Z,\ Q_1^+ = Q_0$$