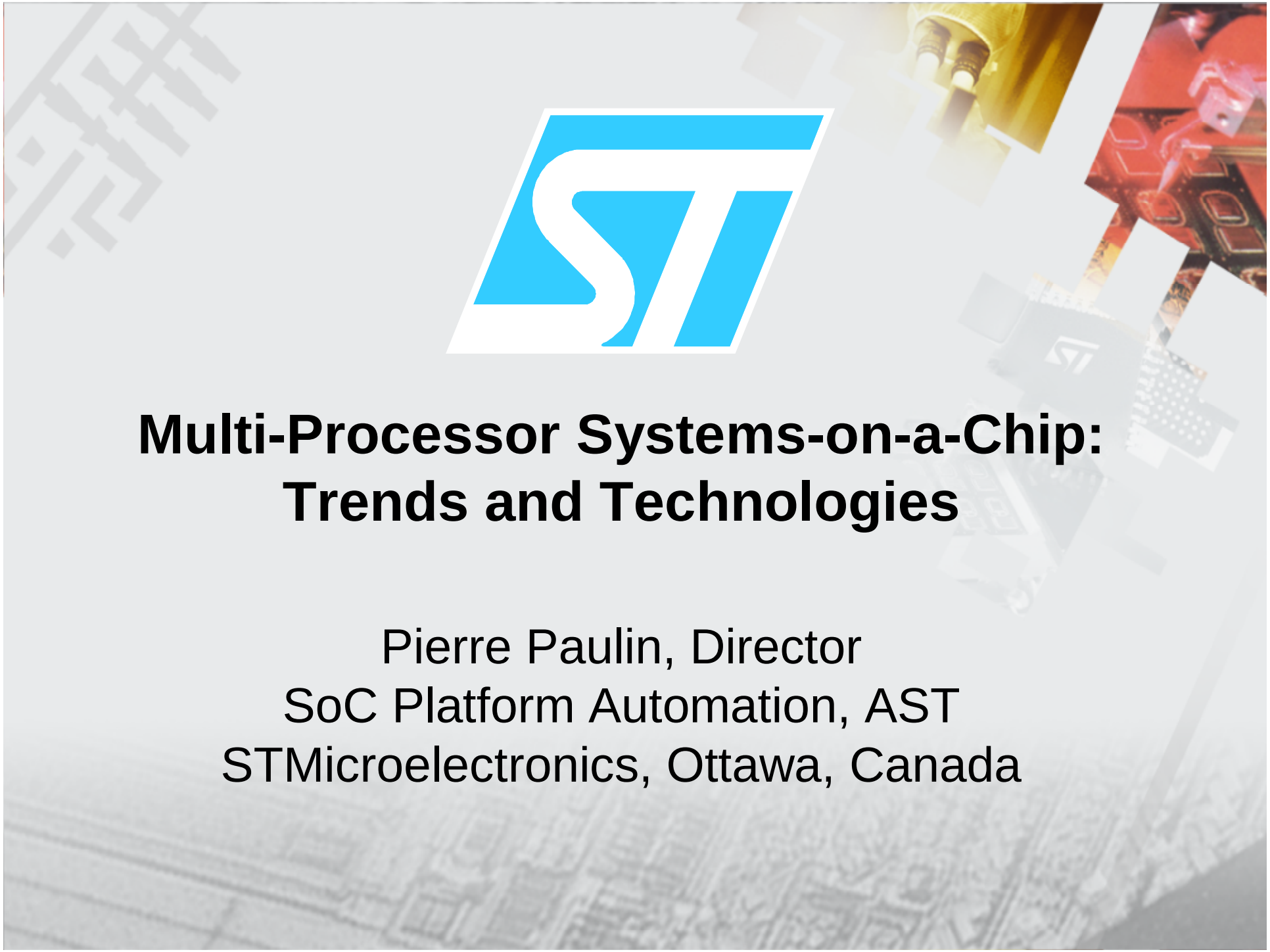


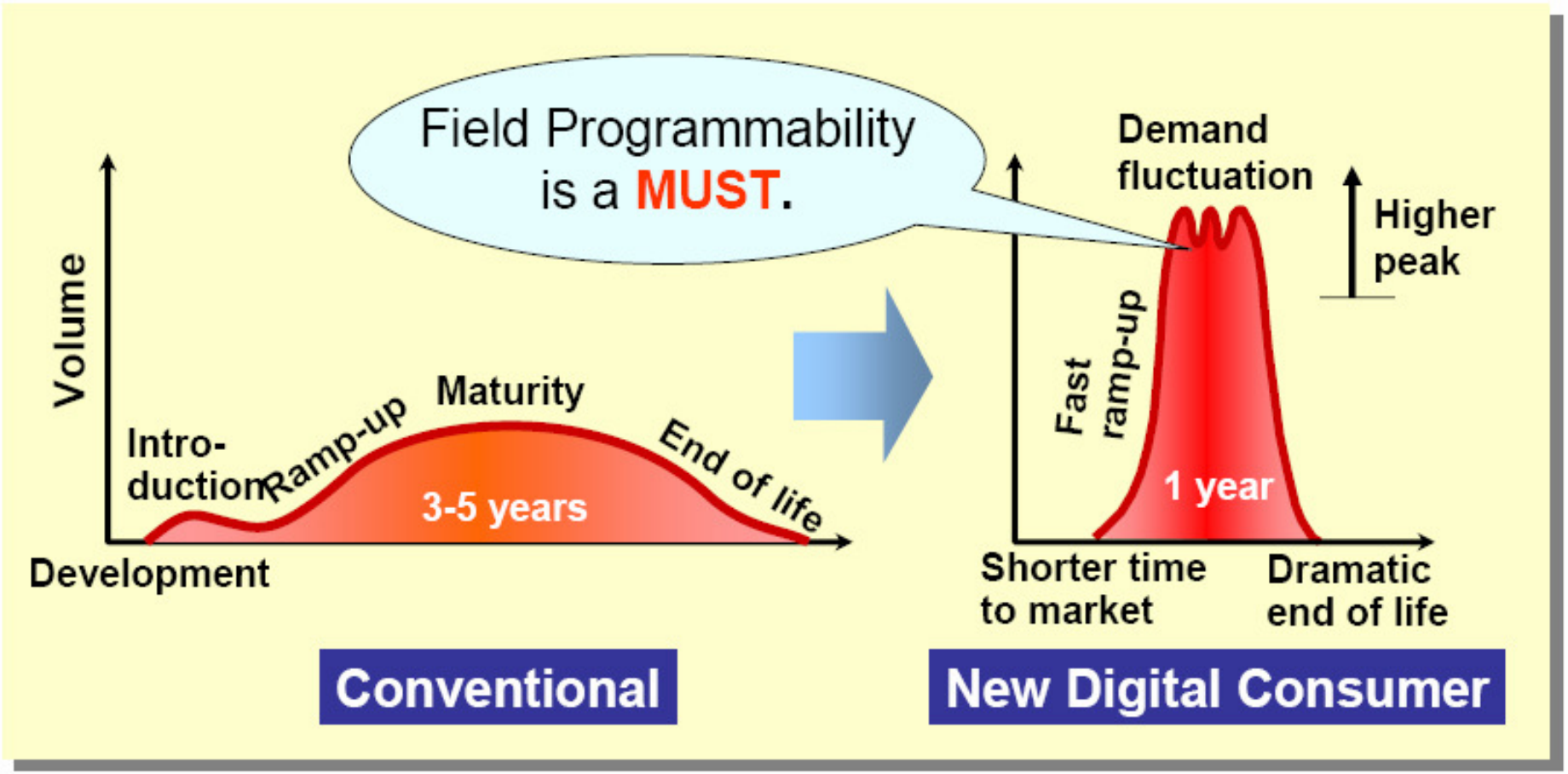
Multi-Processor Systems-on-a-Chip: Trends and Technologies

Pierre Paulin, Director
SoC Platform Automation, AST
STMicroelectronics, Ottawa, Canada

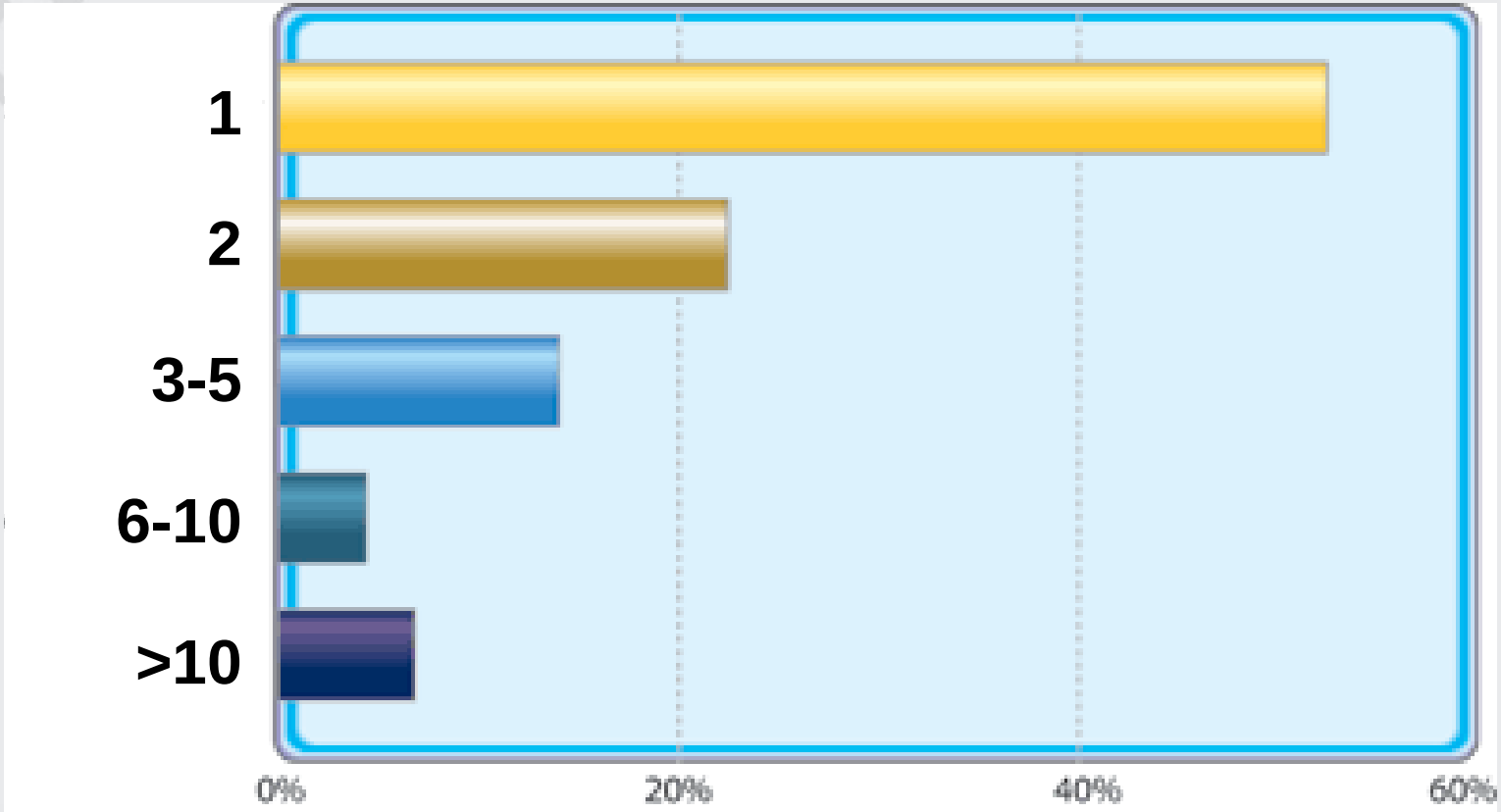
Outline

- MP-SoC Trends
  - Key market trends
  - Key technology trends
- MP-SoC Technology Objectives
- ST's MP-SoC Technologies
  - Application to platform mapping
- Applications: Multimedia, Networking
- R&D Outlook

Dramatic Change in Product Life Cycle



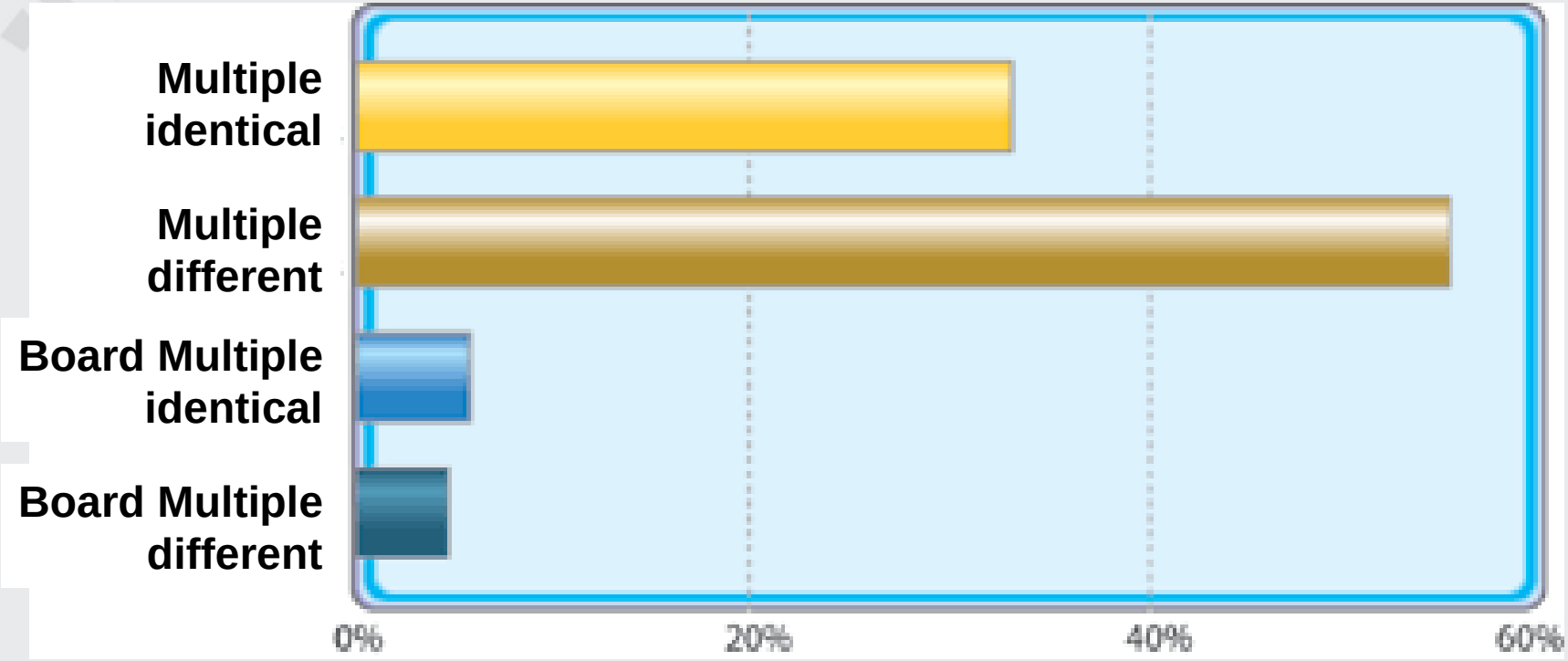
Emb. Systems Prog. Survey 2005: Number of Processors per chip



- Nearly 50% of chips use multiple processors
- Over 100 projects used >10 processors

Source: Embedded Systems Programming Magazine, 2005

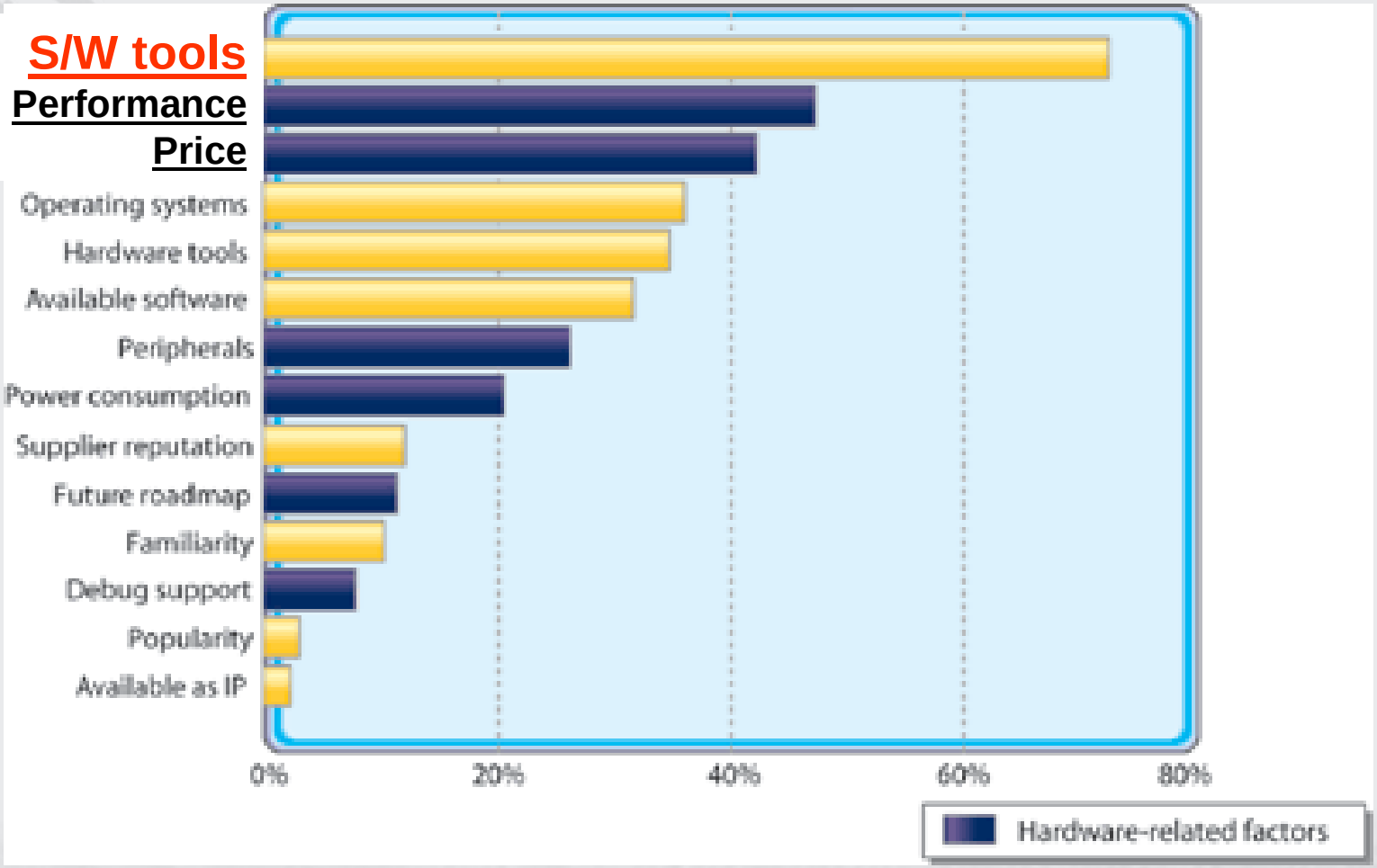
Processor Heterogeneity



- 60% of systems are heterogeneous MP

Source: Embedded Systems Programming Magazine, 2005

Processor Selection Criteria



- Quality of software tools sells the processor

Source: Embedded Systems Programming Magazine, 2005

Market Trends Summary

- Continued reduction in time-to market
  - Fast changing specs, requirements
  - Need for high-level capture and mapping

- Increasing cost of developing SoC platforms
  - 10M$ to 80 M$ for today's 90nm SoC's
- Need to increase time-*in*-market
- Implies higher flexibility is needed
  - Rising proportion of SoC function in eS/W
  - Currently 50% to 75% of design costs
- Majority of all SoC's have 2 or more processors
  - Leading edge (20%) have 6-10 processors

Outline

- MP-SoC Trends
  - **Key market trends**
  - ***Key technology trends***
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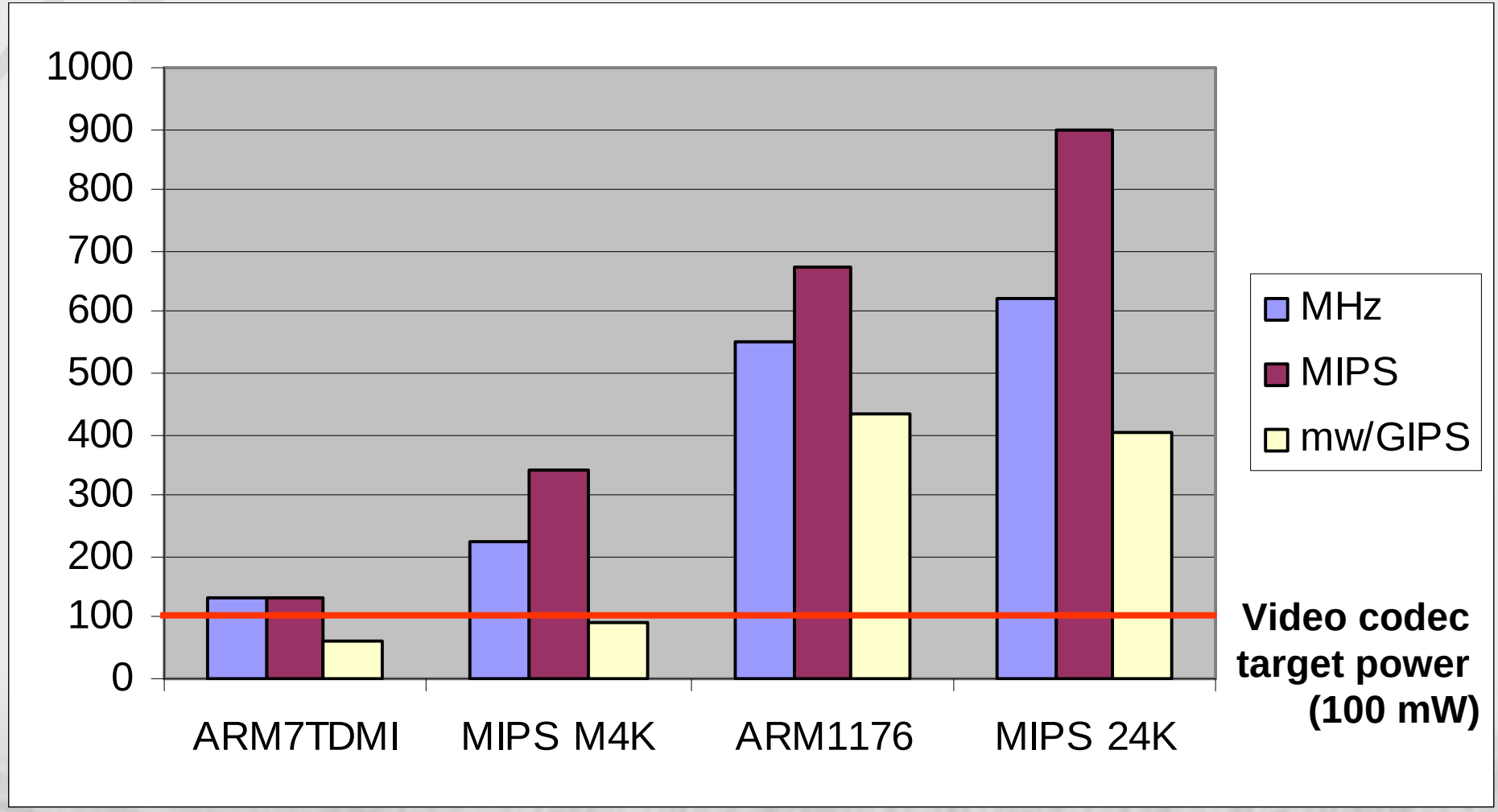
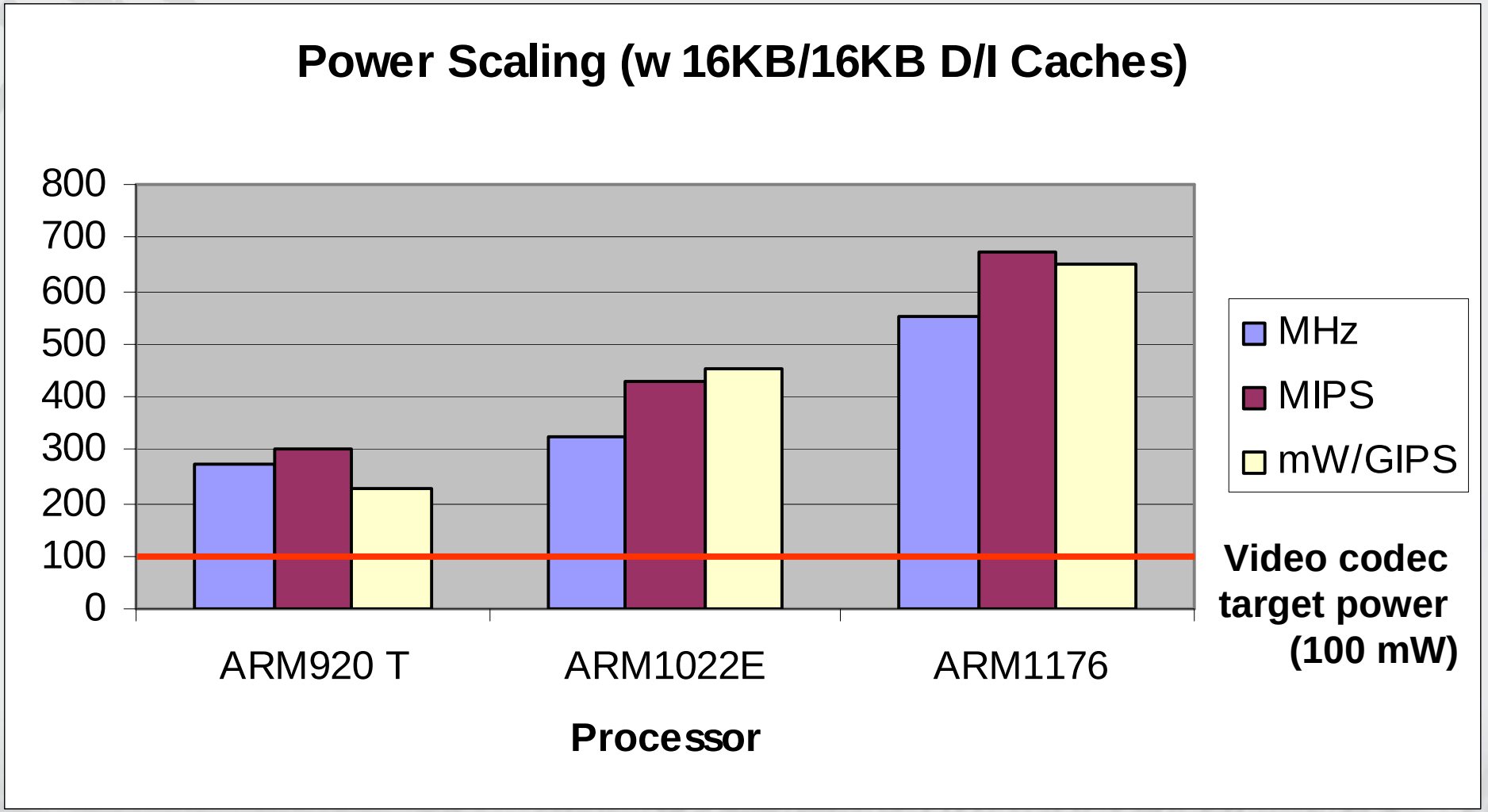
- Applications
- R&D Outlook

Power Scaling (Core Only)
Commercial Cores



Source: ARM, MIPS

Power Scaling (Cores + Caches)



Source: ARM

Voltage and Frequency Scaling (ADI Blackfin DSP)

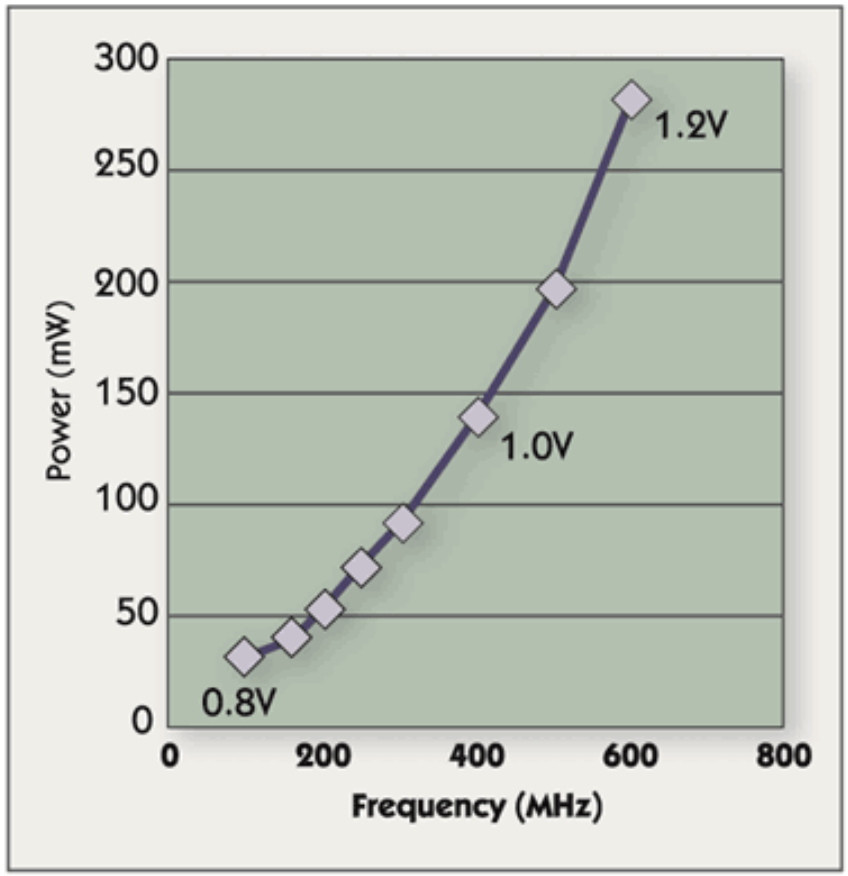
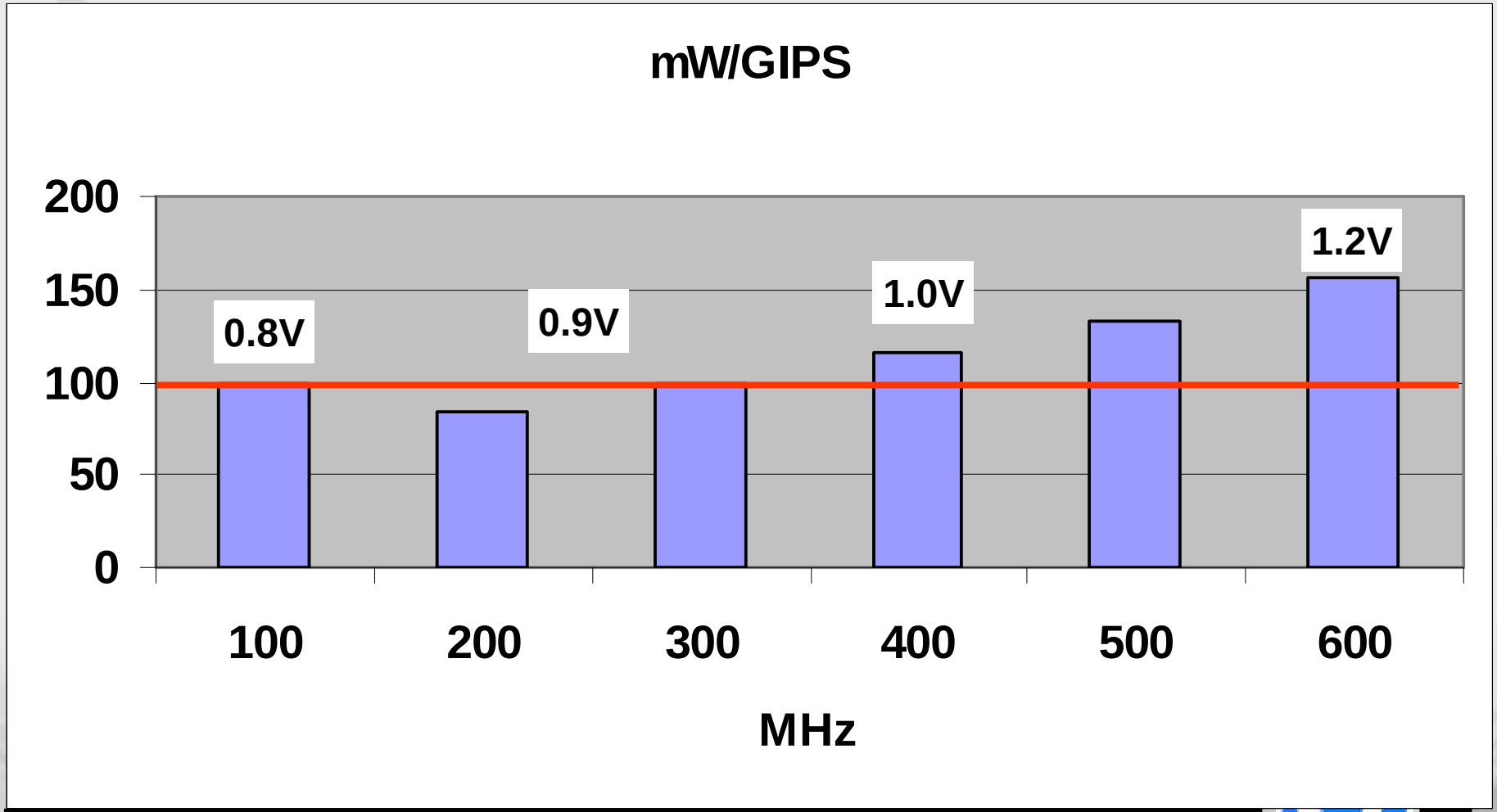


Fig. 2 Power consumption vs. operating frequency and voltage, ADI Blackfin.

Source: ADI

Voltage and Frequency Scaling (ADI Blackfin DSP)

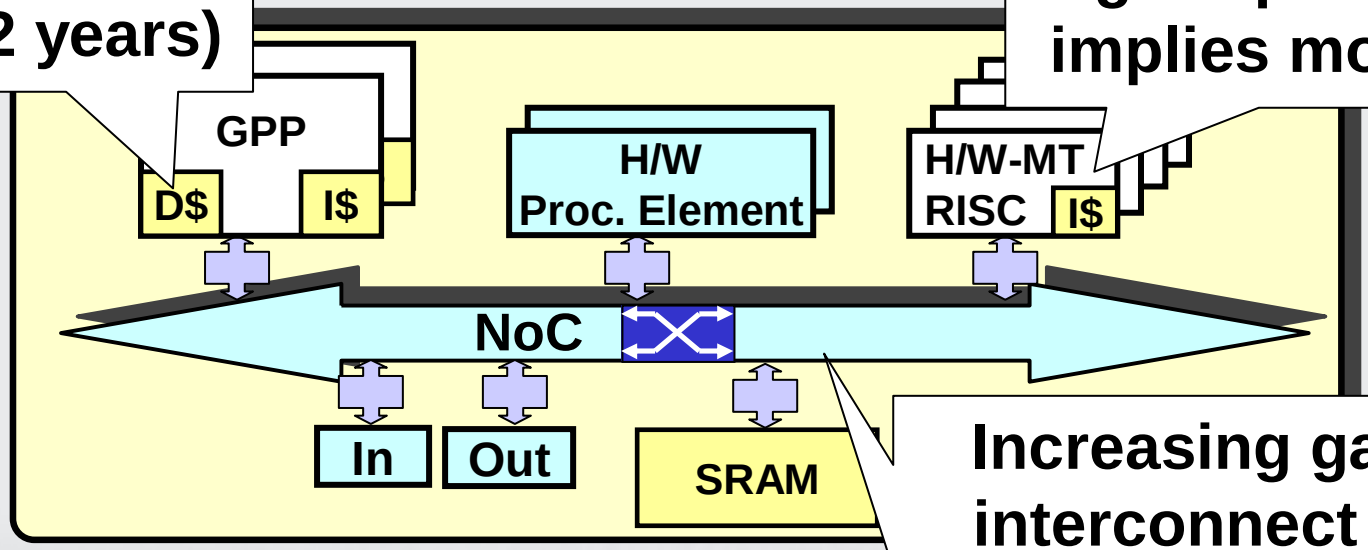


Source: ADI

Technology Trend: Latencies

Increasing gap memory & processor speeds (2x / 2 years)

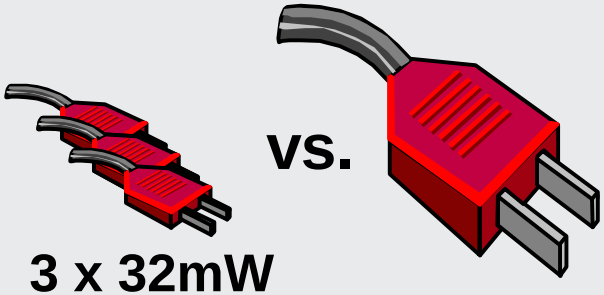
More parallel processing (lower-power, higher-perf./mm2) implies more IPC



Increasing gap interconnect & gate delays (multi-clock intra-chip delay)

Technology Trends Summary

- Embedded processor speed wall ~1GHz
  - More function requires more parallelism
- Parallelism favors lower power solutions
  - Single 625 MHZ MIPS processor consumes 4x more power than 3x 225 MHz processors
  - Need to efficiently program these parallel cores though …



- Three types of rising latency
  - Growing gap in interconnect v.s logic delays
  - Growing gap in memory v.s. logic delays
  - MP implies inter-processor communication

Outline

- MP-SoC Trends
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- ***MP-SoC Technology Objectives***
- ST's MP-SoC Technologies
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- R&D Outlook

What is Next SoC Paradigm Shift?

System function

- Algm./system expert
- S/W developers
- Platform programming

Prog. Models

H/W-S/W architecture

- Domain-specific platform expertise
- Fast platform derivatives

RTL to Layout

- Component expertise
- Process differentiators (BiCMOS, eDRAM, eFlash, eFPGA)

System Applications

- Audio codecs
- Video codecs
- Still image processing
- Communication stacks

months

2005: Platform "Insulation"

Architecture Platforms

- Hard-disk drive platform
- Set-top box, DVD, HDTV
- Mobile multimedia
- Image processing platform

2 yrs

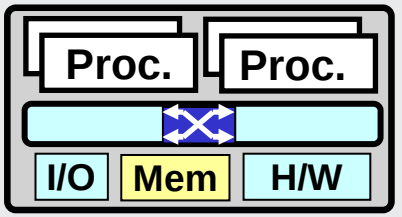
1995: RTL, ISA "Insulation"

Component IP

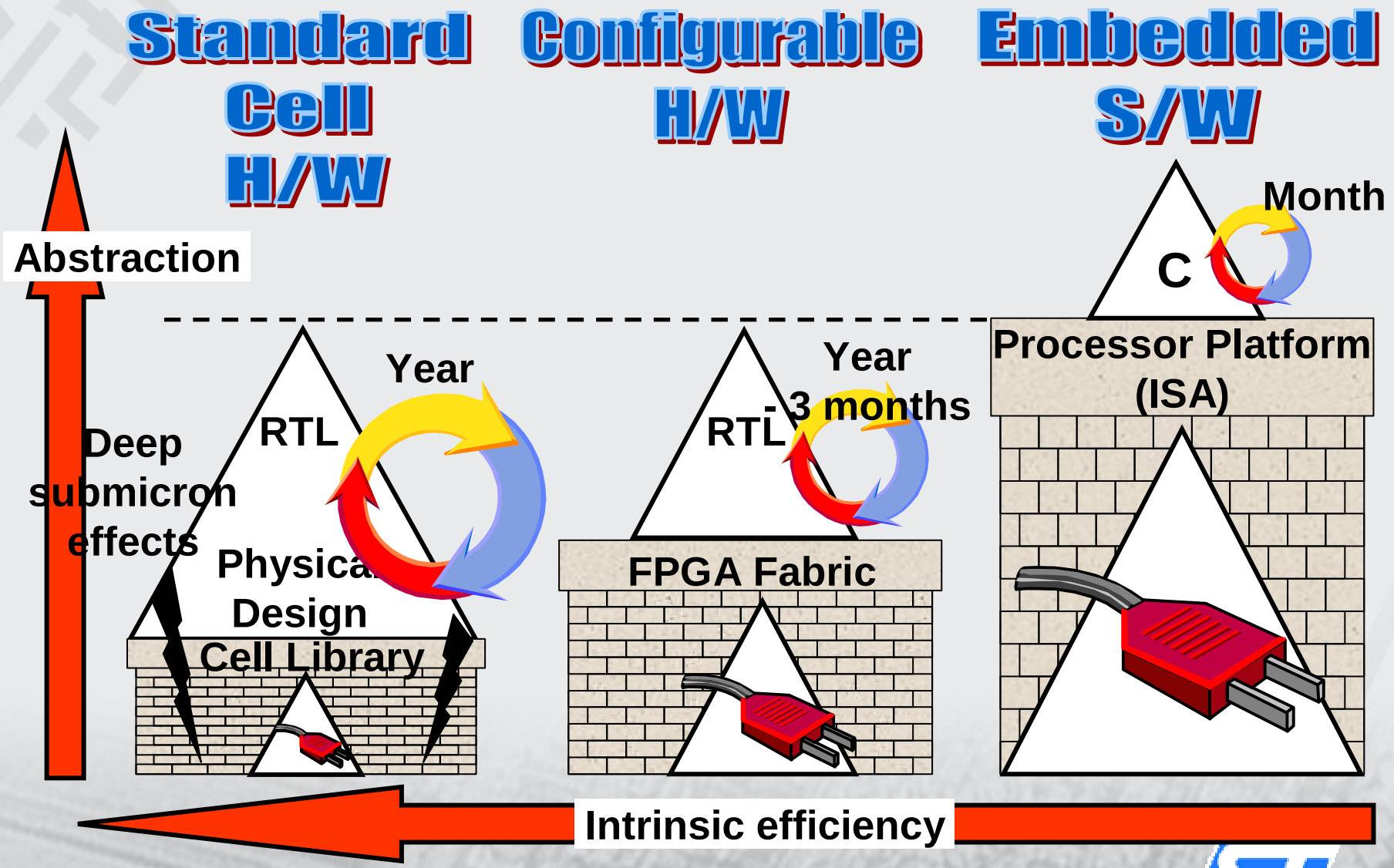
- Value-add cores, IP
- Commodity cores: GPP, DSP, MCU, Bus
- Libraries: Cells, memories, I/O

year

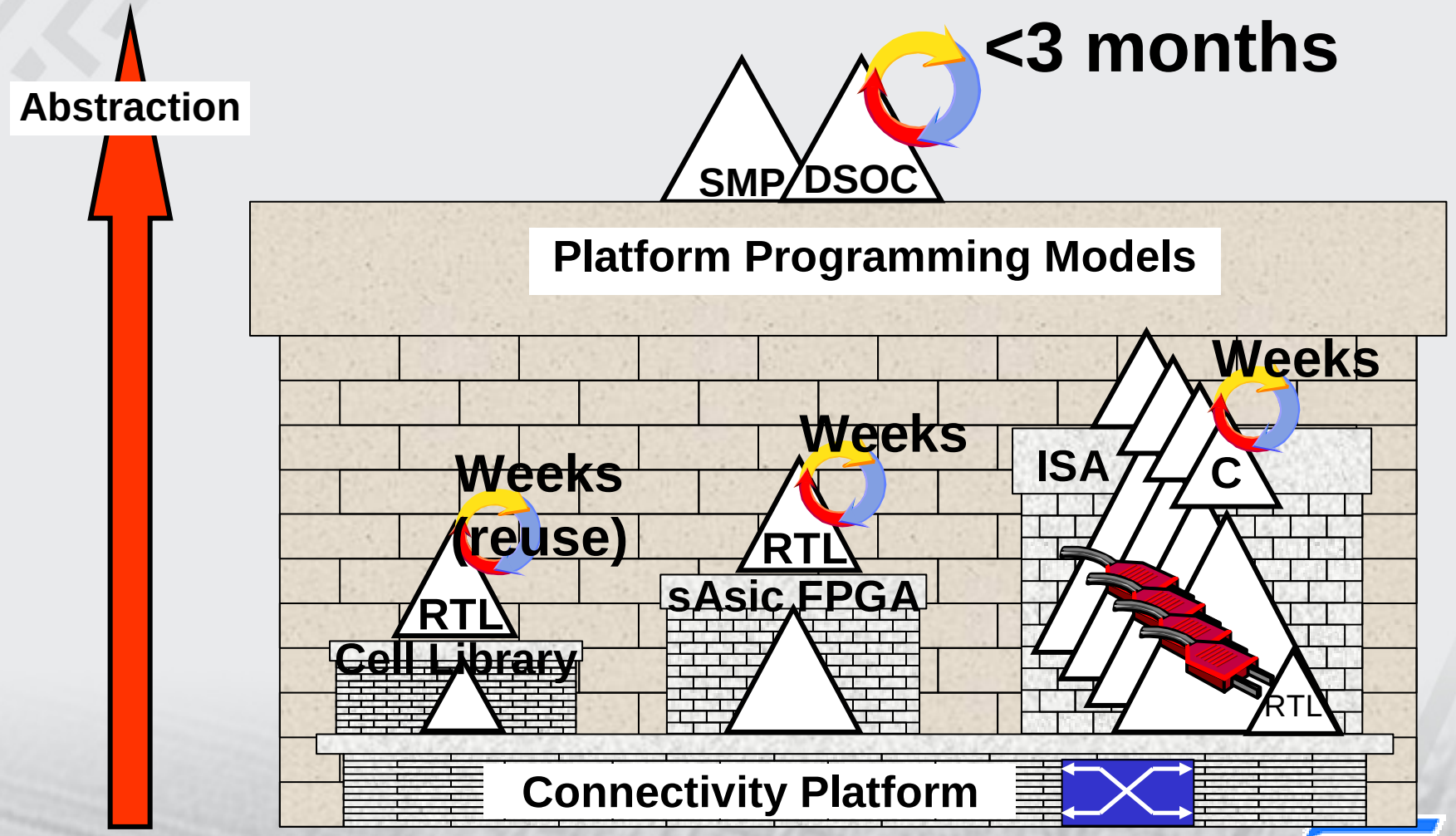
1985: Cell Library "Insulation"



Configurability Trade-offs



Flexible SoC Platform Objectives



Outline

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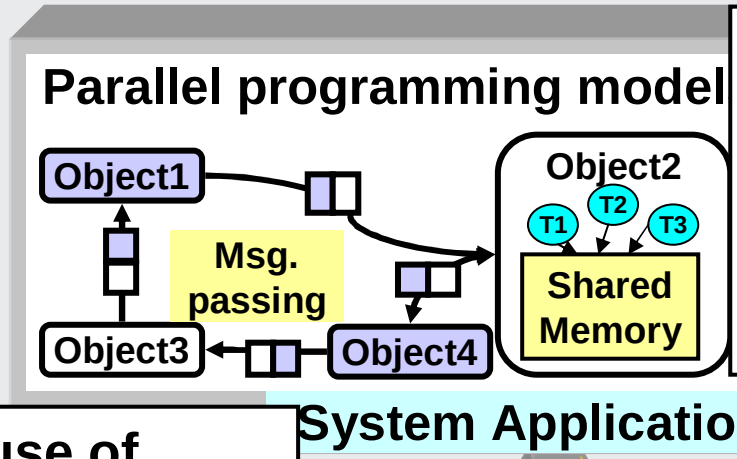
  - Application to platform mapping
- Applications
- R&D Outlook

System-on-Chip Platform Automation Ottawa, Canada

- Focus on use of flexible SoC platforms
  - Multi-processor, Network-on-Chip, Configurable H/W
- Applications
  - Multimedia (A/V/I), Networking, 3G basestation
- Leverage ST's other system design technologies

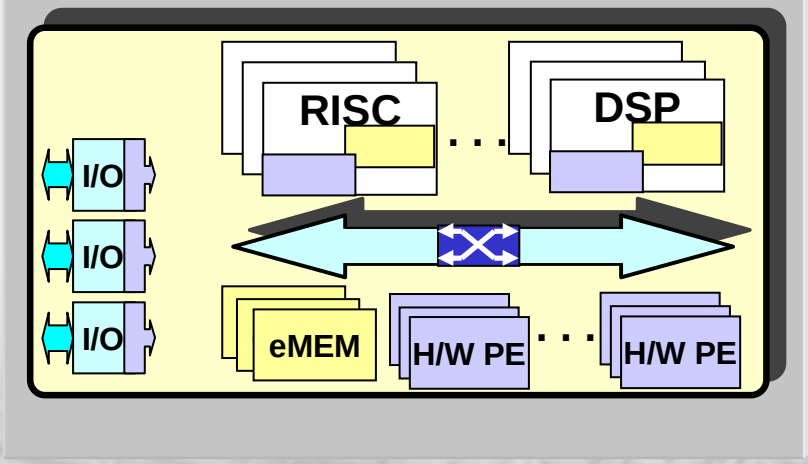
- Info:
  pierre.paulin@st.com
  +1 (613) 768-9069

MultiFlex MP-SoC Tools

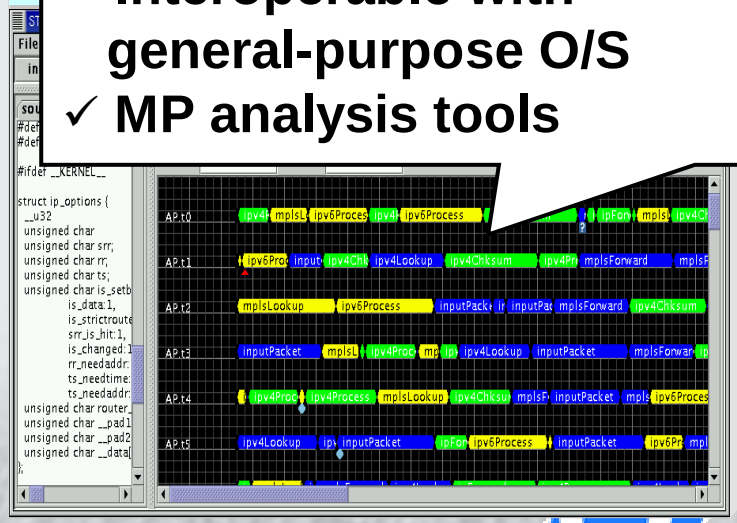


- ✓ Proven, established programming models (msg. passing, SMP)
- ✓ User-defined parallelism

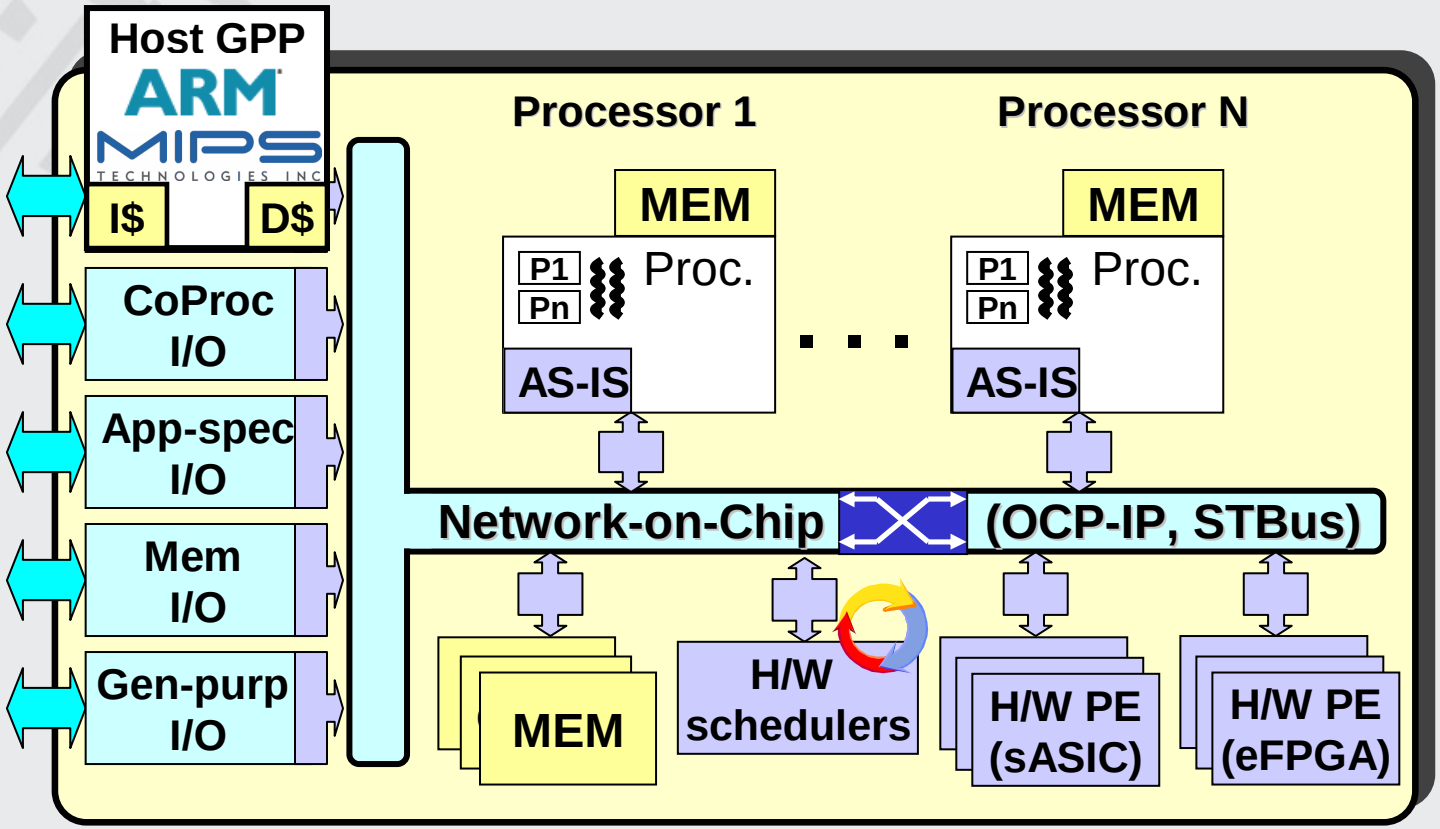
- ✓ Simplify the use of heterogeneous HW/SW MP-SoC architectures

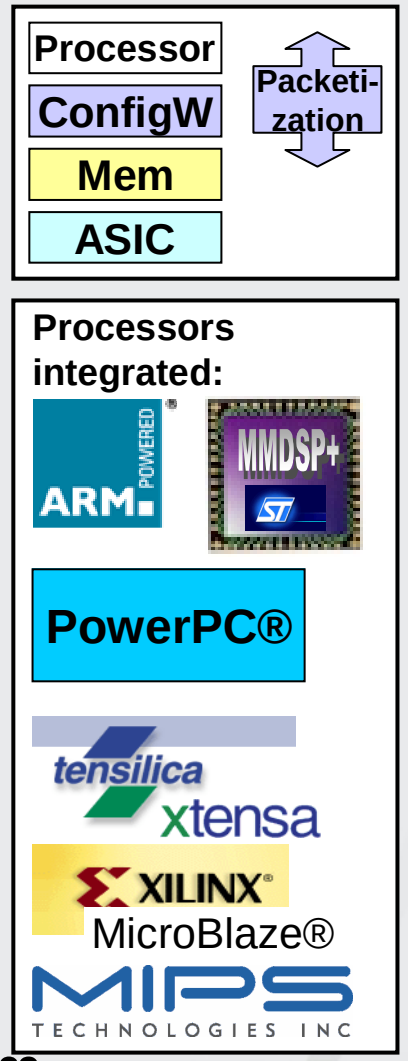


- ✓ Lightweight mapping tools
- ✓ Supported by H/W RTOS
  - thread-level parallelism
- ✓ Interoperable with general-purpose O/S
- ✓ MP analysis tools



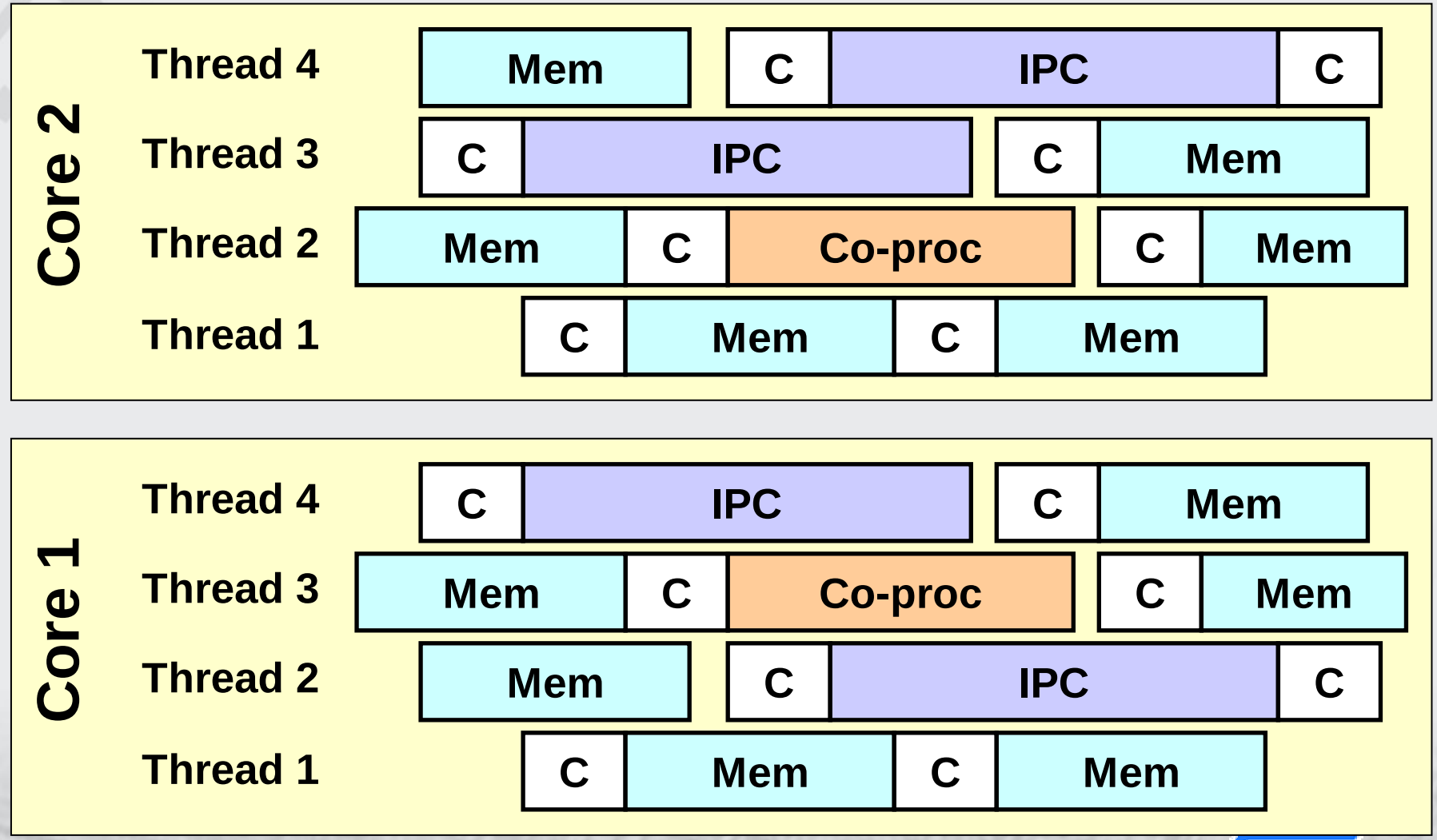
FlexMP Demo Virtual Platform



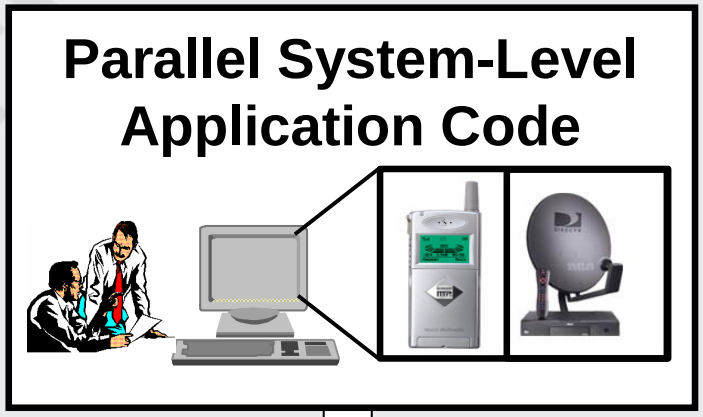


- Multi-threaded, multi-processor platform
- Popular processor models w. config. extensions: H/W multithreading and pipeline depth

Hiding latency with H/W MT

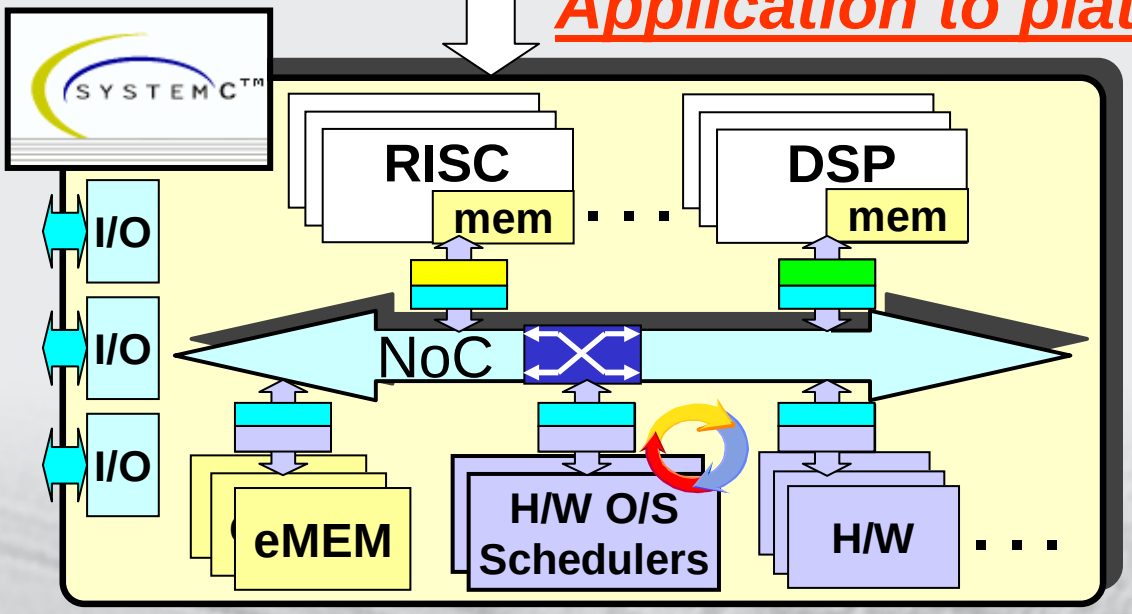


MultiFlex MP-SoC Platform Tools

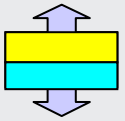


- Two parallel Programming Models
  - DSOC: Object-Oriented Message passing
  - SMP: Shared memory

Application to platform mapping



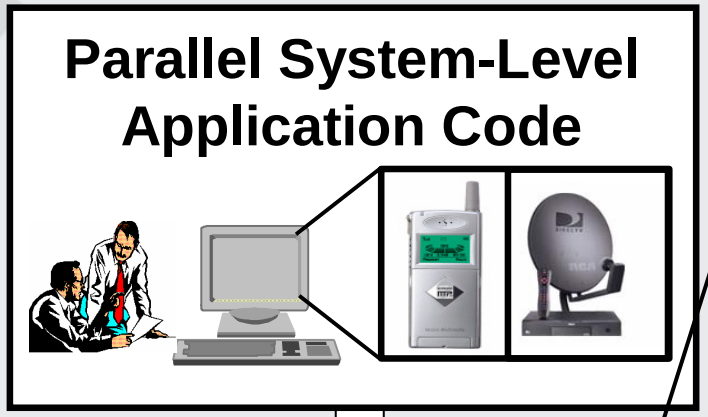
- Fine grain parallelism



H/W message passing, IP Plug and Play

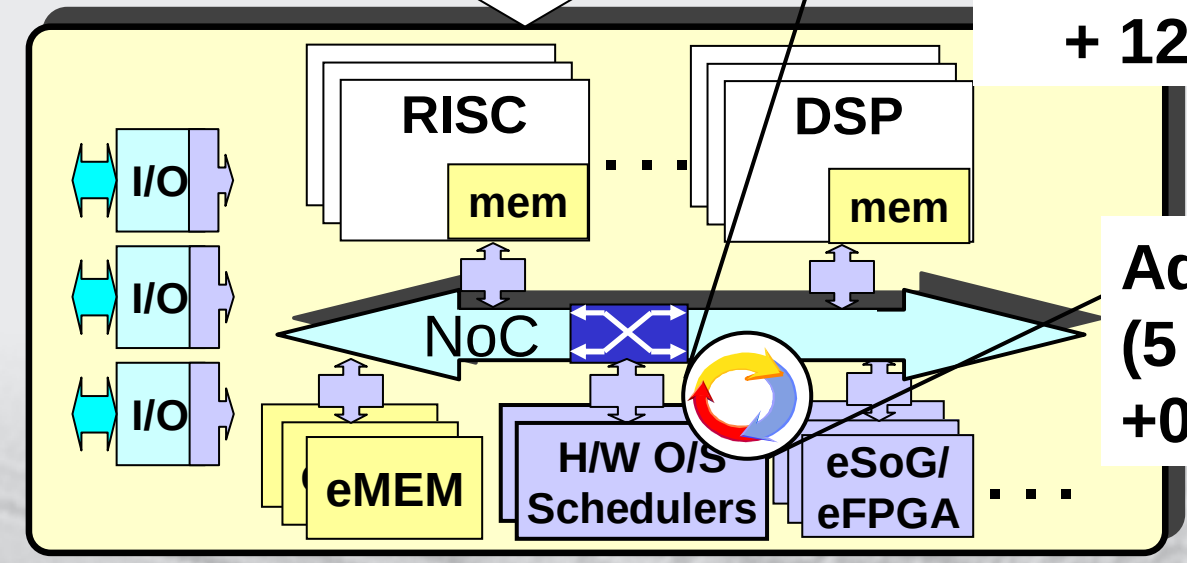
H/W MP-O/S scheduler accelerators

Impact of H/W Accellerators



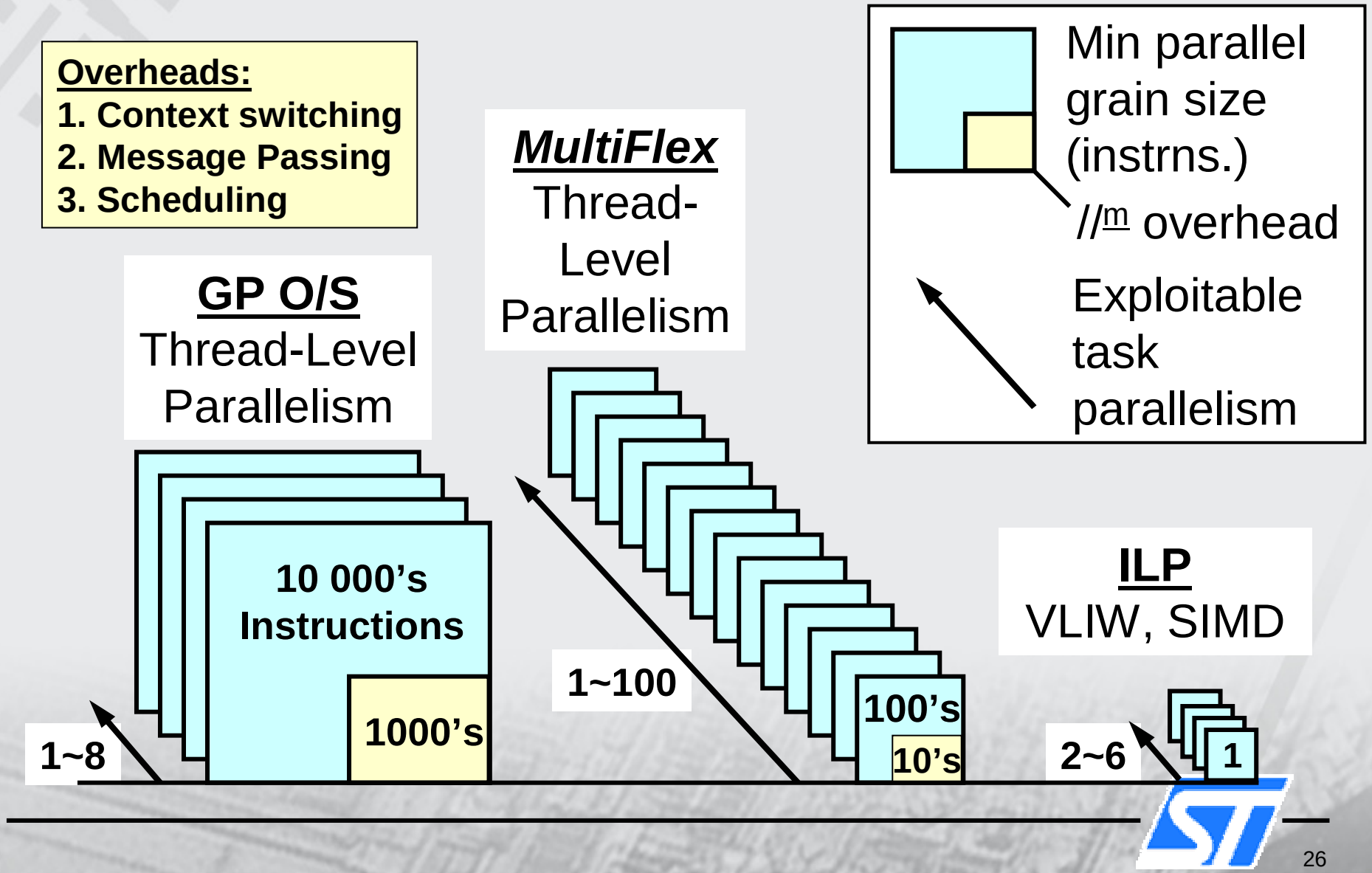
Msg passing rate:
<15 instructions
(15M msg/s @200 MHz)

Fork-join (for N forks):
10 instructions
+ 12 cycles/thread

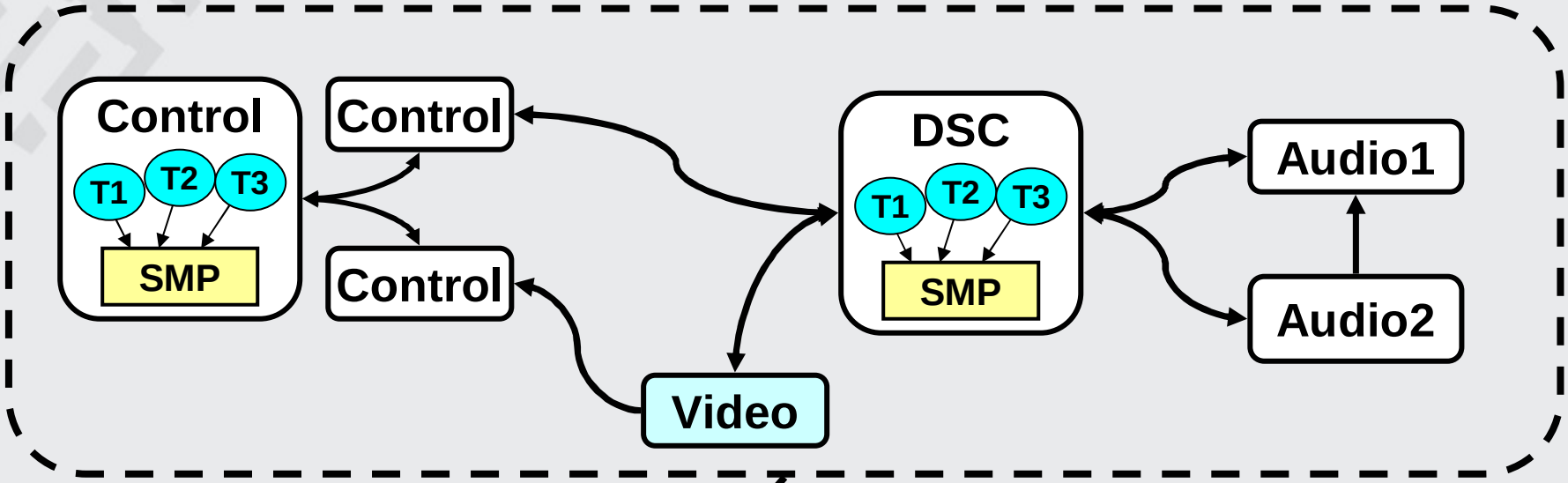


Additional cost
(5 processor system):
+0.3 mm2 (@90 nm)

Exploitable Parallelism



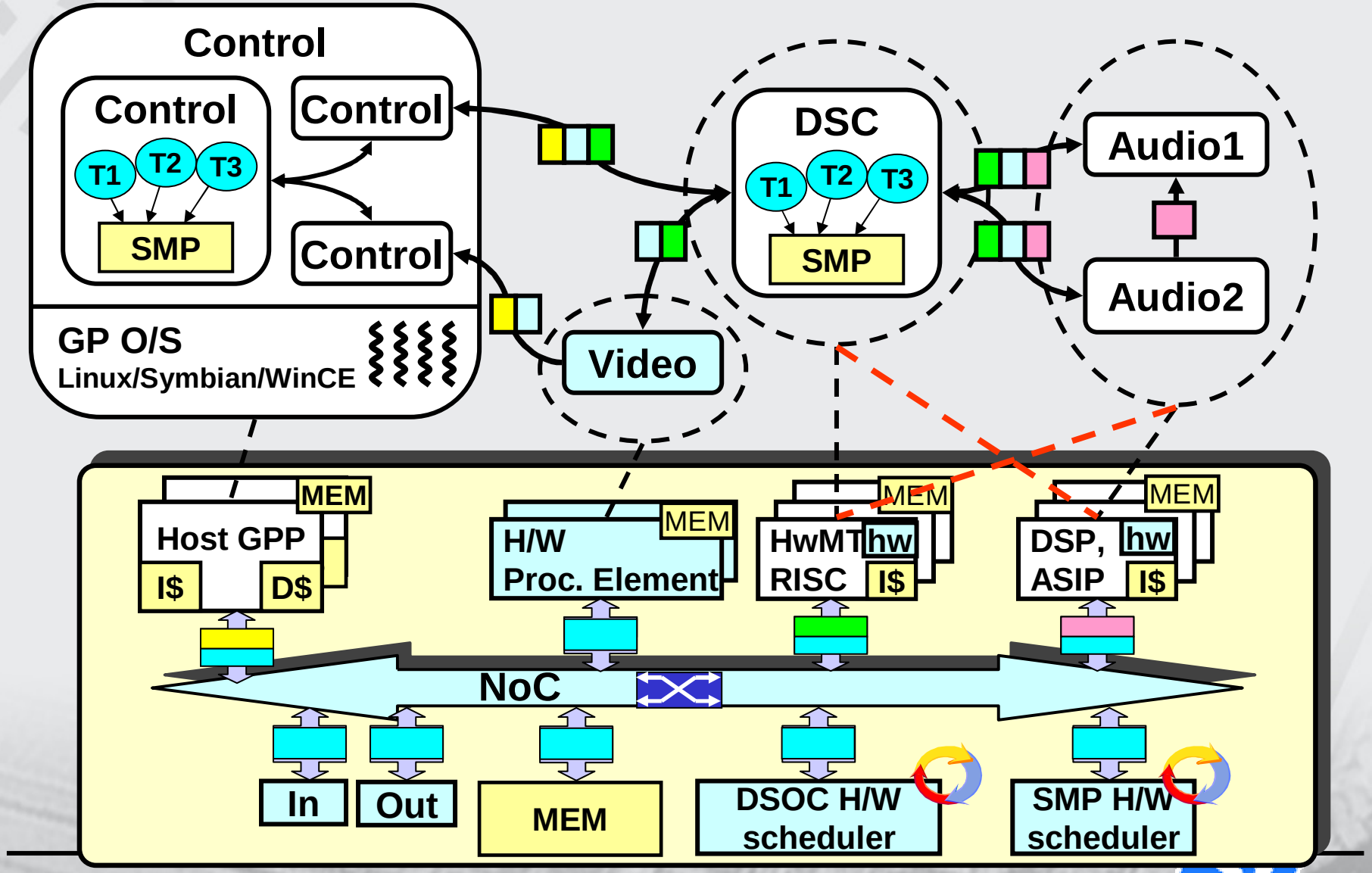
Application to Platform Mapping (1)



Host (Linux/Unix)

- High-level communicating parallel application objects
  - Platform independent
- Map onto host GP O/S to validate HL function and parallelism

Application to Platform Mapping (2)



Outline

- MP-SoC Trends
- MP-SoC Technology Objectives
- ST's MP-SoC Technologies
  - Application to platform mapping
- ***Applications***
  - Multimedia, Networking, 3G
- R&D Outlook

MultiFlex MP Applications

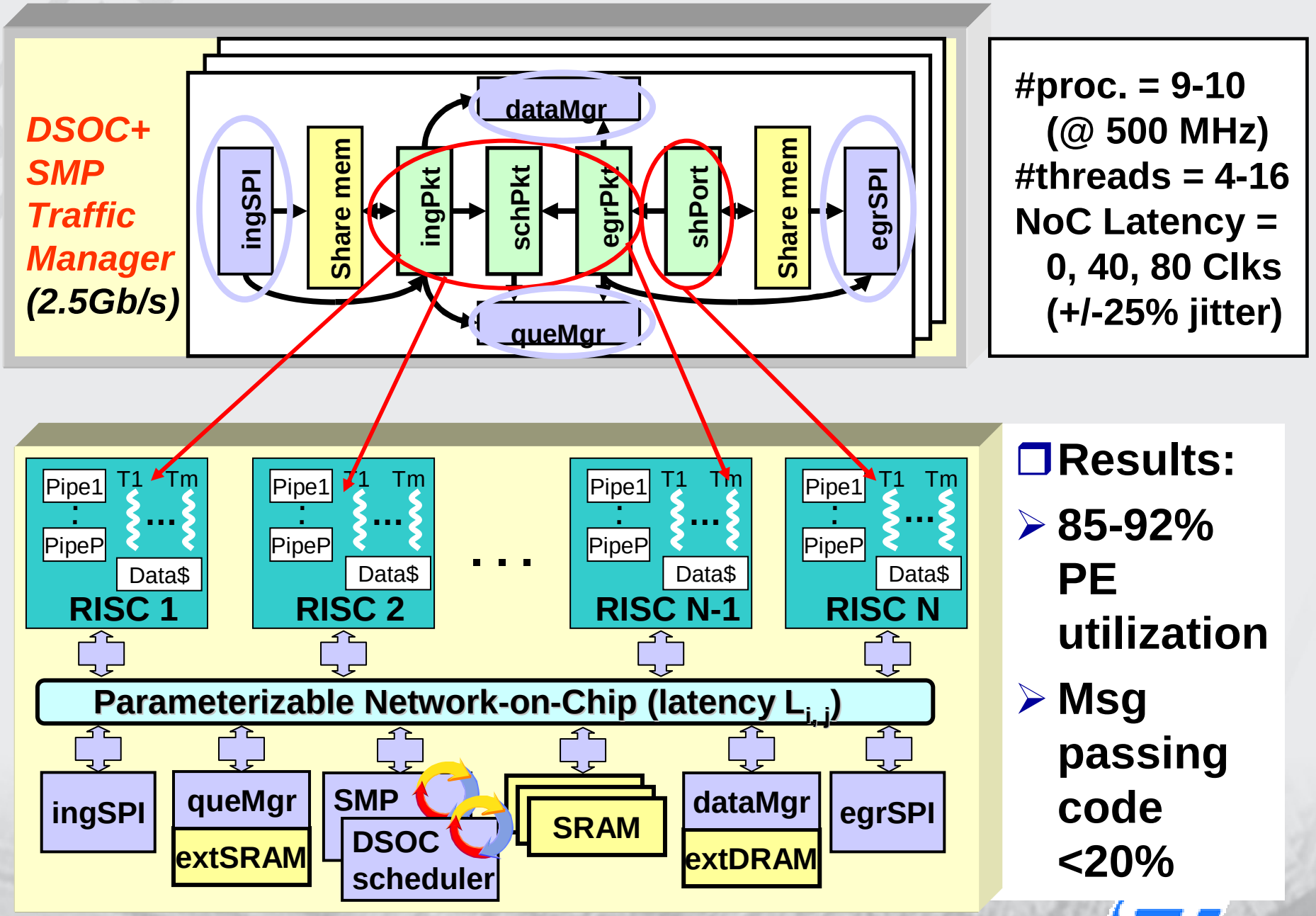
- Packet processing
  - 2.5/10 Gbps IPv4 forwarding, traffic manager
  - High-throughput platforms

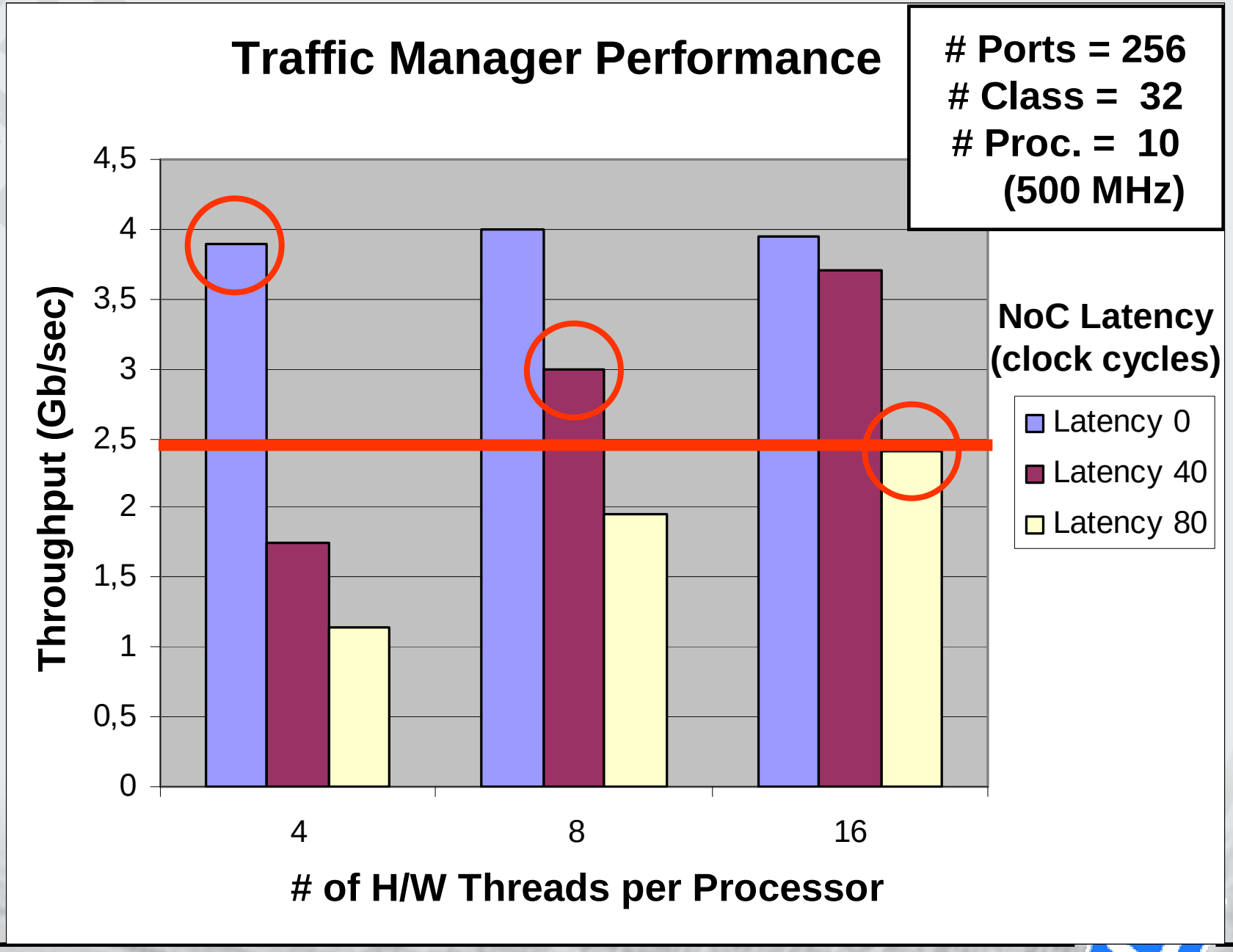
- Nomadik mobile multimedia
  - Heterogeneous platform, O/S interoperability
  - Impact: Hundreds of programmers

- Video codec exploration
  - VGA (30fps): Small grain, mixed SMP/DSOC

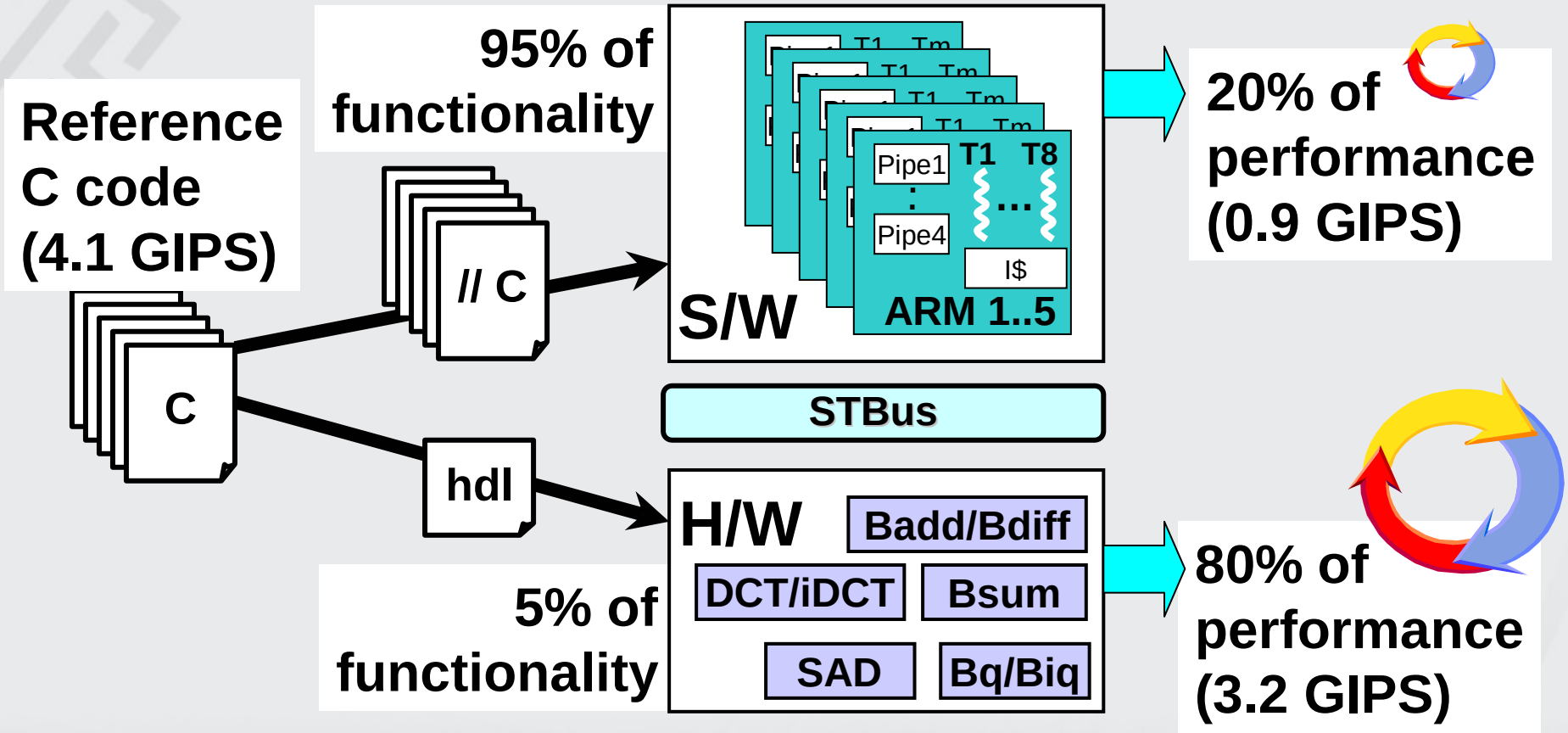
- Digital Still Camera
  - Array access optimization

- 3G basestation
  - Heterogeneous MP (ARM11, 3X DSP, 3X ASIP)


DSOC+
SMP
Traffic
Manager
(2.5Gb/s)
ingSPI
Share mem
ingPkt
schPkt
egrPkt
shPort
Share mem
egrSPI
dataMgr
queMgr
#proc. = 9-10
(@ 500 MHz)
#threads = 4-16
NoC Latency =
0, 40, 80 Clks
(+/-25% jitter)
Pipe1
T1
Tm
PipeP
Data$
RISC 1
RISC 2
RISC N-1
RISC N
Parameterizable Network-on-Chip (latency L i, j)
ingSPI
queMgr
extSRAM
SMP
DSOC
scheduler
SRAM
dataMgr
extDRAM
egrSPI
Results:
85-92%
PE
utilization
Msg
passing
code
<20%

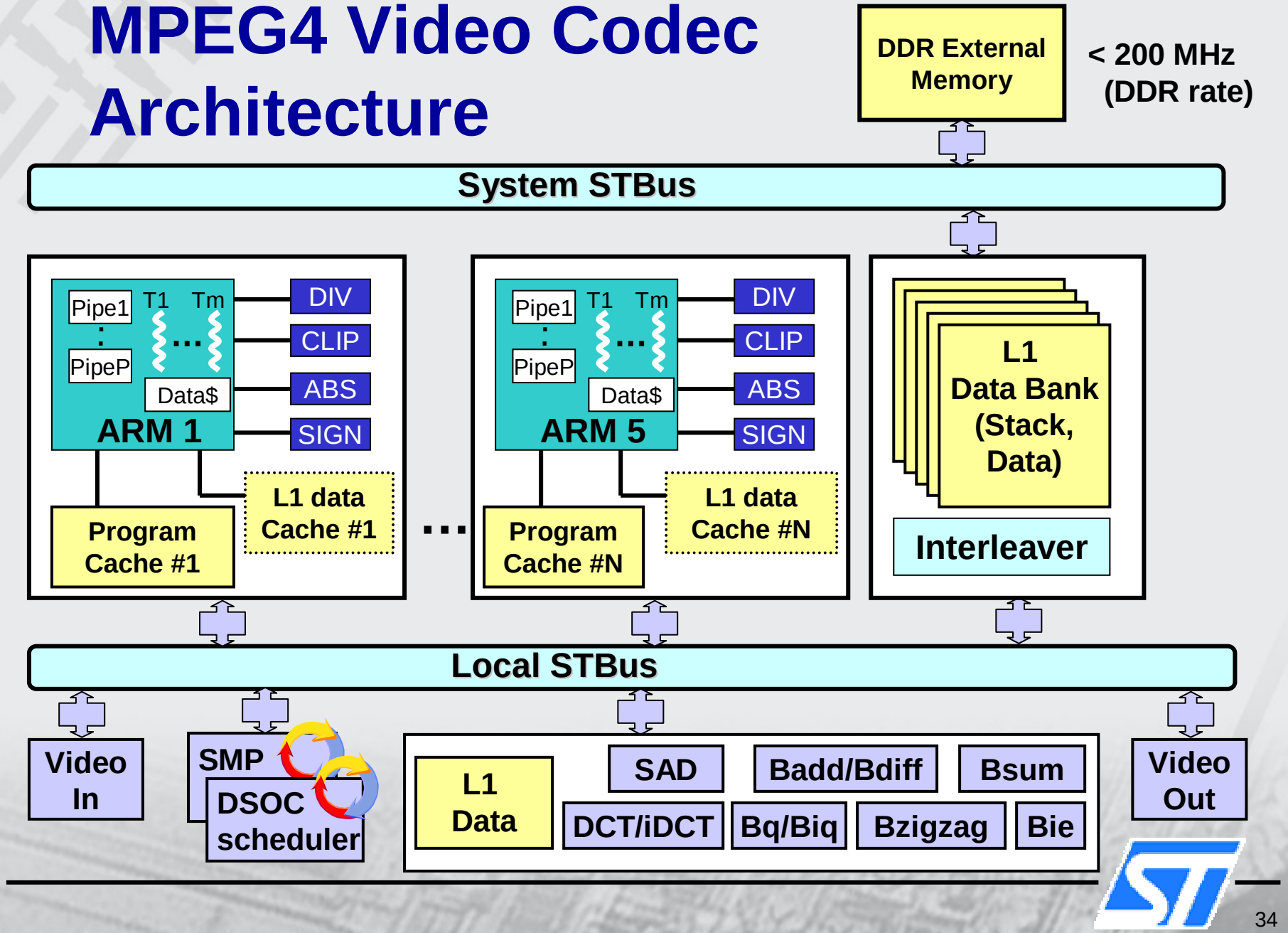

Traffic Manager Performance
Ports = 256
Class = 32
Proc. = 10
(500 MHz)
Throughput (Gb/sec)
4,5
4
3,5
3
2,5
2
1,5
1
0,5
0
4
8
16
# of H/W Threads per Processor
NoC Latency (clock cycles)
Latency 0
Latency 40
Latency 80

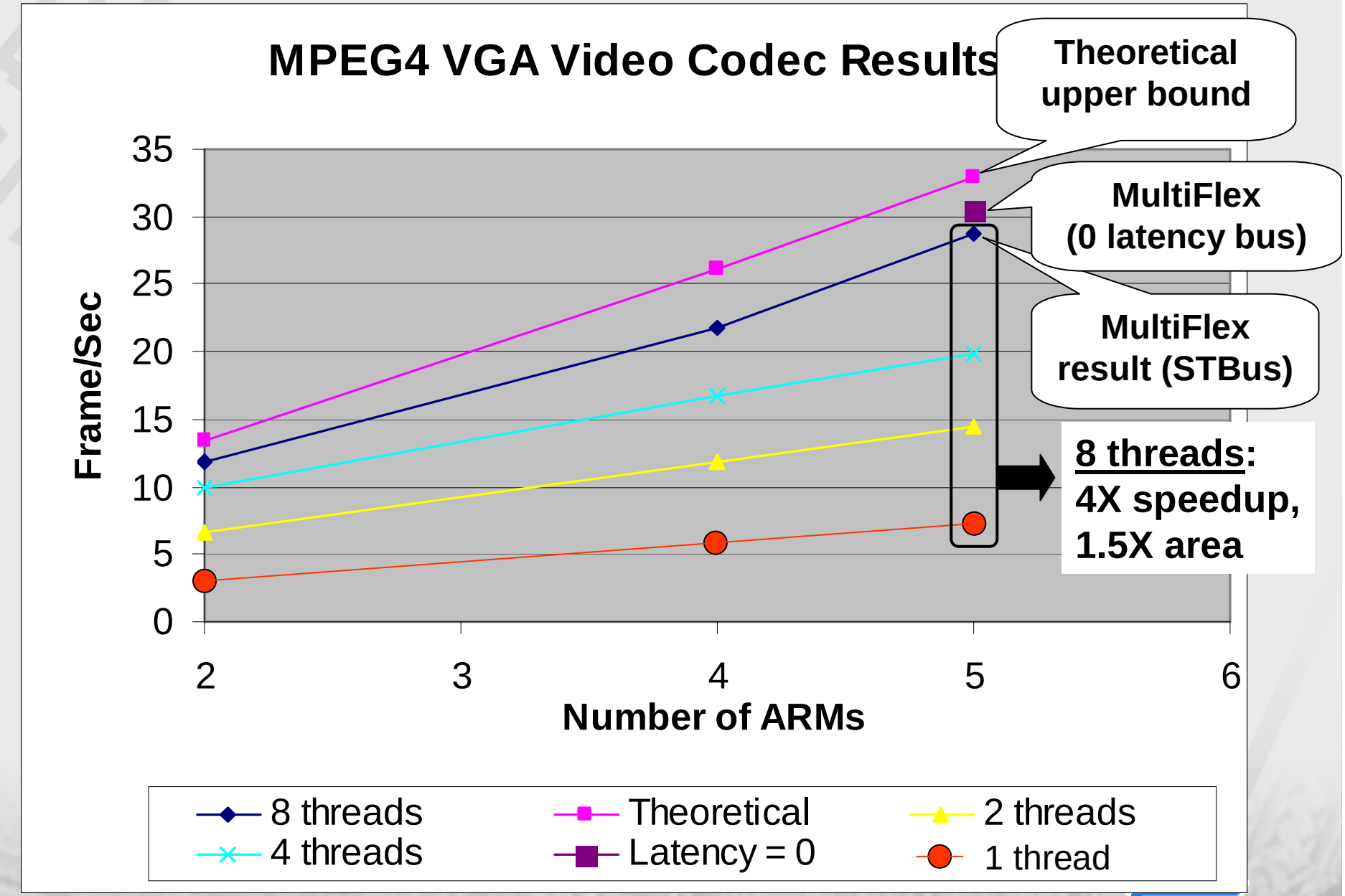
MPEG4 Video Codec (VGA, 30fps)



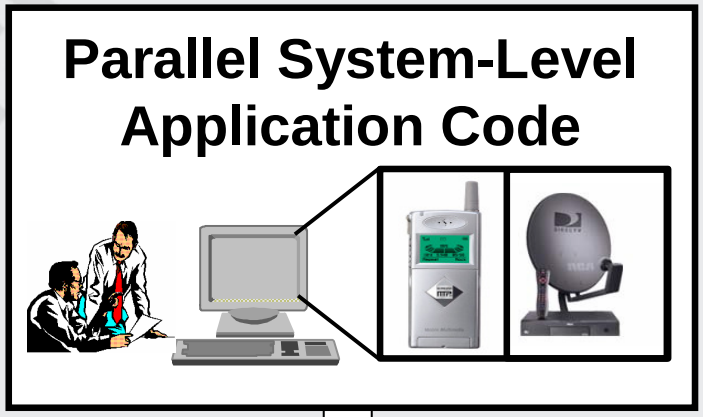
- Parallelization (SMP, DSOC), mapping in <2 months
- Flexibility in S/W, Performance in H/W

MPEG4 Video Codec Architecture




MPEG4 VGA Video Codec Results
Theoretical upper bound
MultiFlex (0 latency bus)
MultiFlex result (STBus)
8 threads: 4X speedup, 1.5X area
Frame/Sec
0
5
10
15
20
25
30
35
2
3
4
5
6
Number of ARMs
8 threads
Theoretical
2 threads
4 threads
Latency = 0
1 thread

MultiFlex Summary



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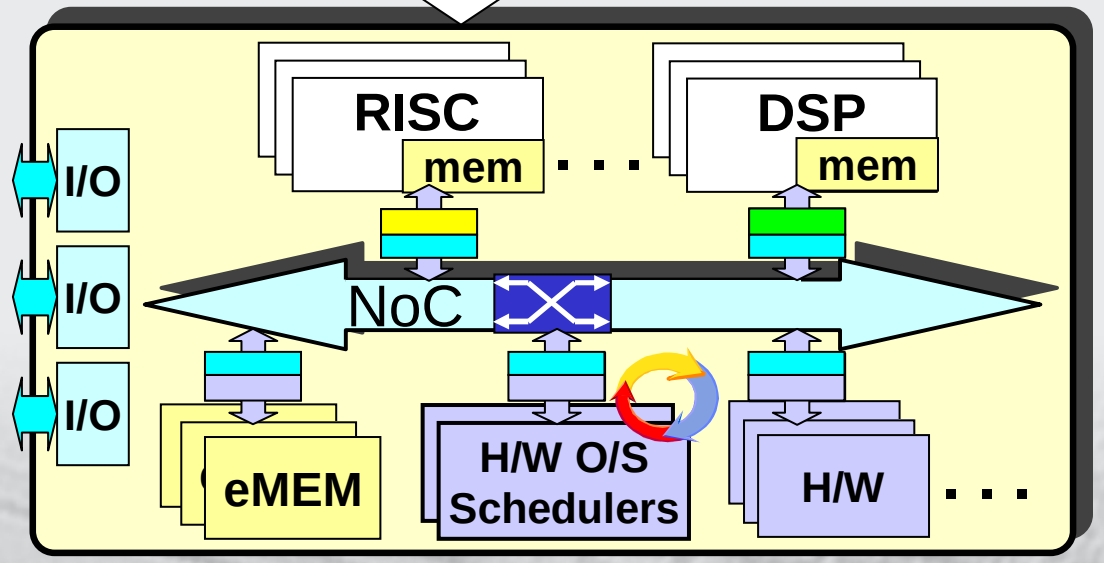
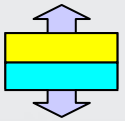
Application to platform mapping



- Programmability + High-performance

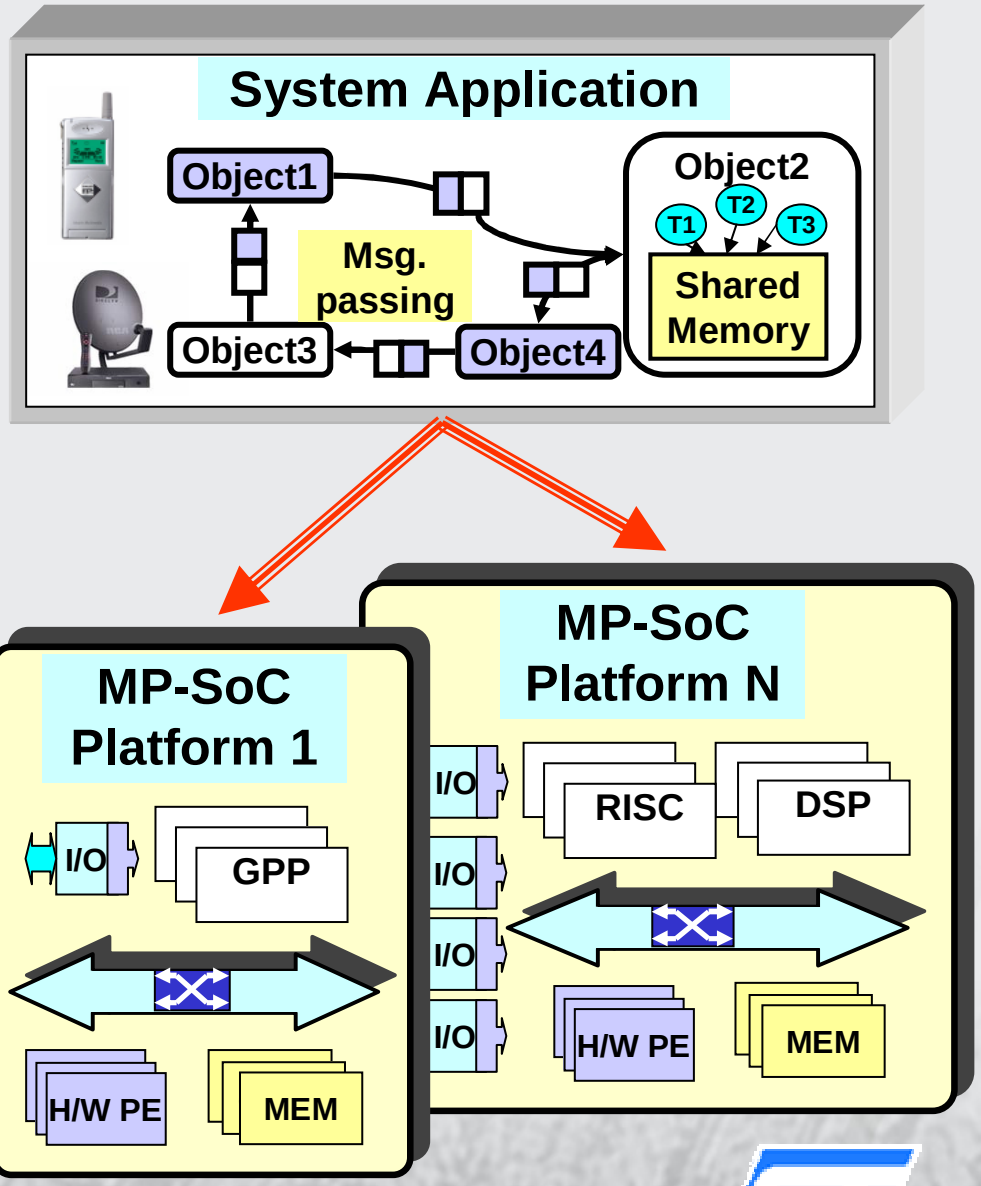


H/W message passing, IP Plug and Play

H/W MP-O/S scheduler accelerators

MultiFlex Value-add

- Platform independent S/W
  - S/W reuse across multiple products
- Platform scalability
- Exploit fine-grain parallelism
- Architecture exploration
- High-performance and flexibility
- Programming productivity



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- ***R&D Outlook***

Key Challenges

- Many architecture parameters to explore
  - HW-S/W partition
  - Number and specialization of processors
  - Memory architecture
- Virtual platform simulation
  - Good observability, controllability, debug
  - High level of abstraction
  - Too slow
- Verification, temporal correctness
  - Need formal parallelism analysis tools