

Test Generation and Fault Localization for Quantum Circuits

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Abstract

It is believed that quantum computing will begin to have a practical impact in industry around year 2010. We propose an approach to test generation and fault localization for a wide category of fault models. While in general we follow the methods used in test of standard circuits, there are two significant differences: (1) we use both deterministic and probabilistic tests to detect faults, (2) we use special measurement gates to determine the internal states. A Fault Table is created that includes probabilistic information. "Probabilistic set covering" and "probabilistic adaptive trees" that generalize those known in standard circuits, are next used.

1. Introduction

Quantum computers will reach a lower limit as to how much heat the computing device can generate. They will solve some problems never possible with standard computers and they will be super-fast and super-small in size for standard applications. Quantum logic gate [1,3,4,5,6,8,9,10,11,14,15,30] is a device which performs an operation described by a unitary matrix on selected qubits (quantum bits, [10]). Binary quantum gates process qubits which can have either a $|0\rangle$ or $|1\rangle$ or both $|0\rangle$ and $|1\rangle$ at the same time to varying extents and hence exhibit a superposition state $\alpha|0\rangle + \beta|1\rangle$ where $|\alpha|^2 + |\beta|^2 = 1$, α and β are complex numbers such that measurement probability of $|0\rangle$ is $|\alpha|^2$ and measurement probability of $|1\rangle$ is $|\beta|^2$. $|X|^2$ is a result of multiplication of complex number X and its conjugate. When the qubit state is observed or measured, it becomes invariably either $|0\rangle$ or $|1\rangle$. Quantum gates and circuits exhibit the additional property of reversibility as their mechanism of action is through Schrödinger's evolution. Thus, test methods developed for permutative (reversible) circuits [11,24] are to some extent helpful for quantum circuits as well. Matrices of all quantum operations are unitary (and usually have complex numbers as entries). Matrix X is unitary when $X * X^+ = I$, where I is an identity matrix and X^+ is a adjoint matrix of X . Adjoint matrix of X is conjugate transpose matrix of X .

Permutative circuits have only basis states and their unitary matrices are permutative [10].

The Test Generation Problem is to find a sequence of input vectors (tests) that applied to the circuit will either confirm that the circuit is correct or will determine that it has one or more faults from certain library of faults. When only a single fault in a circuit is assumed, we use a single-fault model [11]. In a multiple-fault model there is more than one fault (error) in the circuit. Fault localization problem is to locate the faults that are distinguishable, it means show the type of fault and where it is located in the netlist.

The basic quantum gates that are used in quantum circuits in this paper are Inverter (NOT, Pauli X rotation), Hadamard, Toffoli, Feynman, CV (controlled square root of NOT) and CV^+ (controlled square root of NOT Adjoint gate). These gates are selected for explanation only, since they are truly quantum and universal. Their subset $\{NOT, CV, CV^+\}$ allows creating all permutative binary quantum gates by compositions. However, our test generation and fault localization methods (see also [16,17,18,24,26,27] for more details) are for arbitrary (binary, ternary or quaternary) quantum gates and for broad category of fault models. Our software can be applied for both binary and multiple-valued quantum circuits and also for standard CMOS reversible circuits. We allow to use many fault models (including stuck-at basis states, stuck-at superposition states, bridging-AND, bridging-OR, shift of value, phase shift, gate change, gate removal, local measurement, and many others), some of which are only for non-quantum realization of reversible logic, such as CMOS. In principle, from our software point of view any fault model can be used to any type of circuit realization technology, but in practice we just do not use stuck-at models for quantum circuits, or phase fault models for CMOS reversible circuits. In addition, when we test quantum circuits, we can insert additional gates that change the measurement base. This way, probabilistic testing can be changed to deterministic testing, at the price of measurement gate modification (these additional gates are inserted just before the measurement gates).

Pioneering work in the area of testability of reversible logic [11] showed that such circuits are much better testable than irreversible circuits. This is because every test covers half of the faults and every fault is covered by half of the tests [11]. The reversible circuits are then more “transparent” to faults than standard circuits, making the reversible circuits well observable and controllable [24]. It was also shown [24] that fault localization in reversible circuits is easier. The reversibility property notably simplifies all testing-related problems for reversible circuits compared to irreversible circuits [11,24]. Because permutative matrices are a special case of unitary matrices of quantum circuits, one may expect similar properties for quantum circuits. This is partially true (for some fault types the fault tables are dense) but some special properties of reversible logic for stuck-at model [11,24] do not hold anymore.

The preliminary results on testing binary quantum circuits are in [16,17,18] and on fault localization of quantum circuits in [26,27]. The fundamental idea of test generation is straightforward and similar to classical test theory. Test generation is done using a quantum circuit simulator. First, the good circuit is simulated with basis binary input signals (tests). Next every possible quantum fault is inserted (our fault model is inserting arbitrary matrix in place of fault, this allows to simulate many different types of faults) and the circuit with fault is simulated in Hilbert space (no measurement). A local entanglement or local measurement can be inserted as a fault model. A gate can be also removed as a fault model. From the simulator, all possible complex amplitude values before measurement are calculated for all inserted faults. Superposed input bits (as through a vector of Hadamard gates – Hadamard Transform – used in quantum algorithms such as Deutsch-Jozsa [10] can be also used [18]. Additional gates can be inserted just before the measurement gates to change the measurement base. Next, all the measurement values corresponding to complex amplitude values are calculated with their probabilities. The comparison of a measurement from the unitary matrix of a correct circuit and measurement(s) from a circuit with fault determines those input combinations (tests) that produce different measurement values. Observe that in contrast to standard testing and reversible circuits testing, there are four types of faults in quantum domain: (1) faults that can be detected deterministically by standard measurement, (2) faults that cannot be detected (like global phase faults), (3) faults that can be detected by repeated application of tests; these faults can be detected only with certain probability, (4) faults that can be detected deterministically by using special measuring gates. These categories are not necessarily disjoint. Thus, in general, quantum testing is probabilistic testing, but there is a trade-off between the

ratio of probabilistic to deterministic tests and the number of measurement bases.

The paper is organized as follows. Section 2 discusses basic concepts. Section 3 discusses fault models. Section 4 presents testing of binary quantum circuits. We present briefly the software to generate minimum quantum test set and the adaptive tree for fault localization in quantum circuits in section 5. Section 6 concludes the paper. It is assumed that the reader is familiar with classical testing fundamentals, basic quantum gates, unitary matrix calculus of quantum mechanics and simulation. Information about test generation and fault localization can be found in [7] and quantum textbooks like [10], as well as papers [14,15] are recommended.

2. Preliminaries.

By V we denote the “square root of NOT” gate. This is not a permutative gate, but a truly quantum gate. It means, applied to basis states it creates superposition states on its output. The conjugated transpose of a unitary matrix X is called the adjoint of matrix X and denoted by X^+ . By V^+ we denote a gate that has a unitary matrix which is an adjoint of V . Therefore, the adjoint of V is called “square root of NOT adjoint” and has the unitary matrix U_{V^+} of gate V^+ . Design of many permutative gates is based on (controlled) cascading of V and V^+ gates. Cascading two square root of NOT gates acts as a basic inverter gate (see Figure 1a). The operation of the circuit from Figure 1a can be explained by the matrix multiplication. Multiplying the unitary matrix U_V by the input state we obtain the vector $\frac{1}{2} [1+i \ 1-i]^T = V_0$, Figure 2a. By multiplying V by this vector we obtain vector $[0 \ 1]^T = |1\rangle$.

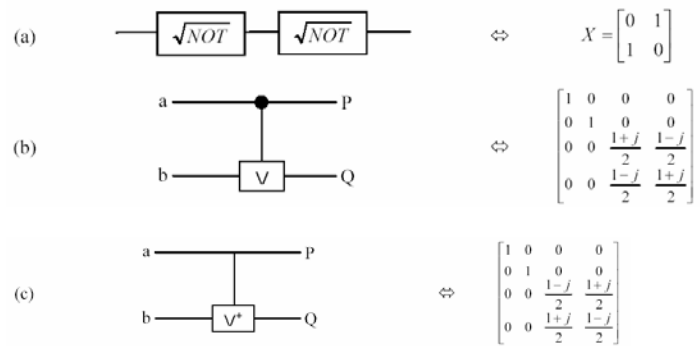


Figure 1 (a) Cascading V gates creates an inverter. Measurement of intermediate state would give $|0\rangle$ and $|1\rangle$ with equal probabilities, (b) Controlled- V gate, (c) its unitary matrix, (c) Controlled- V^+ gate and its unitary matrix.

Let us now try to find, by matrix/vector multiplication, all possible states that can be created by applying all possible serial combinations of gates V and V^+ to states $|0\rangle$, $|1\rangle$ and all states created from these basis states (Figure 2). A qubit $|0\rangle$, given to a “square root of NOT” gate (Figure 2a) gives a state denoted by $|V_0\rangle$. After measurement this state gives $|0\rangle$ and $|1\rangle$ with equal probabilities $\frac{1}{2}$. Similarly all other possible cases are calculated in Figure 2b – h. As we see, after obtaining states $|0\rangle$, $|1\rangle$, $|V_0\rangle$ and $|V_1\rangle$ the system is closed and no more states are generated. Therefore the subset of (complex, continuous) quantum space of states is restricted with these gates to a set of states that can be described by a four-valued algebra with values $\{|0\rangle, |1\rangle, |V_0\rangle, |V_1\rangle\}$.

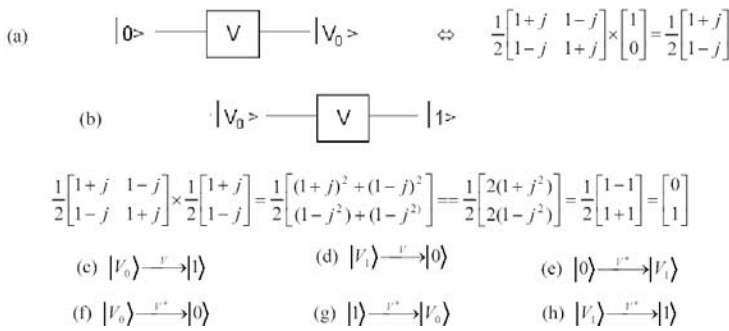


Figure 2. Calculating all possible superposition states that can be obtained from basis states $|0\rangle$ and $|1\rangle$ using V and V^+ gates.

Figure 1b shows a Controlled- V gate (Controlled-Square-Root-of-Not, denoted also by CV) and its unitary matrix. The gate operates as follows. Control signal a goes through the gate unaffected, i.e. $P = a$. If the control signal has value 0 then the qubit b goes through the controlled part unaffected, i.e. $Q = b$. If $a = 1$ then the unitary operation that is inside the box is applied to the input signal b , it means $Q = V$ (b) in our case. This operation is general for all binary controlled gates, for instance the Controlled- V -adjoint (Controlled-Square-root-of-Not-adjoint, denoted also by CV^+). This gate and its unitary matrix are shown in Figure 1c.

3. Fault Models used in our Methodology

We will present below two fault models, in sections 3.1, and 3.2. The first fault model is for the binary permutative quantum circuits that internally use quaternary logic. This model was introduced in [20] for exact synthesis. They are interesting since systematic methodologies of their synthesis can be created that are not based on binary reversible logic methods and can allow synthesis of larger circuits than other methods of quantum circuit design. The second model is general: every kind of quantum gate,

including the truly quantum entanglement producing gates such as Hadamard, can be used in this model. They can appear in any quantum wire and any type of fault can occur in any location in any quantum wire. In this model there is no expected determined set of values that are measured. This makes testing and localization more difficult.

3.1. Multiple-Valued Fault Model (simplified)

In [20] synthesis of binary permutative quantum circuits with NOT, Feynman, CV and CV^+ gates is discussed. Each quantum wire in this model is either a control wire and is binary $\{|0\rangle, |1\rangle\}$ or a data wire and is quaternary $\{|0\rangle, |1\rangle, |V_0\rangle, |V_1\rangle\}$. **Note that a data wire cannot be used as a control wire!** (For instance, in Figure 4, lines a and b are control lines and line c is a data line. It is not possible to use line c to control lines a or b .) The input-output behavior of a correct circuit is however always binary. In this model it is assumed that as a result of a fault (gate removal or insertion) the binary wire remains binary and the quaternary wire remains quaternary. Thus, in binary wires the faults are observed as output values $\{|0\rangle, |1\rangle\}$ and in quaternary wires the faults are observed as values $\{|0\rangle, |1\rangle, |V_0\rangle, |V_1\rangle\}$. This fault model will be presented here for ease of the presentation and to illustrate simplifications that are possible when certain additional assumption can be made about the quantum circuit. In this type of model the set of all possible complex amplitudes that are measurable is limited to a finite set of values of some multiple-valued algebra. This simplifies the testing procedure and also the selection of special measurement gates.

Observe that in bulk technology such as NMR [10] the measurement process can distinguish not only between basis values $|0\rangle, |1\rangle$ but also between values $|0\rangle, |1\rangle$ and the measured values the superposed states such as $|V_0\rangle$ and $|V_1\rangle$. This property is also used in the first model.

3.2. General Fault Models for arbitrary quantum circuits

In contrast to the model from section 3.1, the general fault model does not assume a finite set of internal quantum states that are measurable/observable. There are no special types of quantum wires and the fault can be an insertion or removal of single programmable pulses that correspond to parts of permutative gates. For instance, if a Feynman gate is composed by serial connection of two CV gates, the model from section 3.1 above would assume that both wires are binary, but if only one of the CV gates is removed, the binary controlled wire changes to a quaternary wire – this shows the limitation of the model from sec. 3.1.

For further simplification of explanation, we present here two special variants of the general quantum fault model: (1) gate insertion, (2) gate removal. We assume that Pauli X, Y and Z rotation gates, Hadamard gates and phase gates are inserted in the location of fault. Pauli gates are a standard model known from quantum error correction. The removal gate model is that any single gate is removed from the circuit - it has also certain technological substantiation [29]. We selected these types of faults because they have been selected for quantum correction circuits or for quantum testing, but our basic methodology and software are independent on particular fault model selection.

$$\begin{array}{ccccc}
 \begin{bmatrix} 1 & 1 \\ 0 & 0 \end{bmatrix} & \begin{bmatrix} 0 & 0 \\ 1 & 1 \end{bmatrix} & \begin{bmatrix} 0 & 1 \\ 1 & 0 \end{bmatrix} & \frac{1}{\sqrt{2}} \begin{bmatrix} 1 & 1 \\ 1 & -1 \end{bmatrix} & \begin{bmatrix} 1 & 0 \\ 0 & i \end{bmatrix} \\
 \text{(a)} & \text{(b)} & \text{(c)} & \text{(d)} & \text{(e)} \\
 \hline
 \begin{bmatrix} 0 & 0 & 0 \\ 0 & 0 & 0 \\ 1 & 1 & 1 \end{bmatrix} & \begin{bmatrix} 0 & 0 & 0 \\ 1 & 0 & 0 \\ 0 & 1 & 1 \end{bmatrix} & \begin{bmatrix} 1 & 1 & 1 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 \end{bmatrix} & \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 1 & 1 & 1 & 1 \end{bmatrix} & \\
 \text{(f)} & \text{(g)} & \text{(h)} & \text{(i)} &
 \end{array}$$

Figure 3 Matrices of faults. (a) stuck-at-0 in binary reversible circuit, (b) stuck-at-1 in binary reversible circuit, (c) inverter in binary quantum circuit, (d) Hadamard in binary quantum circuit, (e) phase fault in binary quantum circuit, (f) stuck-at-2 in ternary reversible circuit, (g) truncated plus 1 in ternary quantum circuit, (h) AND-bridging fault in binary reversible circuit, (i) stuck-at-3 of quaternary reversible circuit.

Figure 3 shows some selected examples of fault matrices (these matrices are square and in general complex non-unitary). In general they are complex matrices, depending on the assumed faults' nature. The "insertion" fault model in our system is that a fault matrix is inserted in place of the fault. More formally, the fault matrix is inserted in the netlist of parallel-serial connections of unitary matrices of gates. Pauli rotations have unitary matrices, but the general model of our software allows non-unitary matrices as well [17]. The matrices of stuck-at faults are not unitary, but some other fault matrices may be unitary, like for instance changing phase (by a small angle) or inserting a Pauli rotation.

The gate removal general fault model can be treated as a special case of the gate insertion model. This means that to remove a gate G (represented by a unitary hermitian matrix G), one just inserts its own inverse matrix (G⁻¹) and thus transforms the gate G into identity operation. Examples of using these models are shown later.

4. Principles of Test Generation for Binary Quantum Circuits

4.1. Explanation of the gate removal model for Multiple-Valued Fault Model

Assume a permutative binary quantum circuit. We assume that the first from left gate CV (Figure 4a) is removed. Assume first that standard measurement gates are used. The output measurements of this circuit in a presence of fault are in general probabilistic, because the circuit uses non-permutative quantum gates such as Controlled-V. To illustrate the test generation method, the fault-free output is calculated and is represented by a K-map of function f from Figure 4a, as shown in Figure 4b. Similarly, the K-map of the faulty outputs are calculated in four-valued algebra in quantum wire c of the circuit from Fig. 4a. By comparing the faulty output (in general, a vector of complex numbers) with the faultless output (a binary vector), it can be observed whether the test for this fault is deterministic or probabilistic. As seen from Kmaps in Figure 4b-e the tests $a'b'c'$, $a'b'c$, $a'bc'$, $a'bc$, $ab'c'$, and $ab'c$, are deterministic and tests abc' and abc are probabilistic (by b' we denote a negation of b). The Kmap can be drawn for each output separately (Figure 4b,c) or for all outputs together (Figure 4d,e). All outputs are measured (observed) together (Figure 4e). Obviously, the internal signals (in general, complex numbers) of the quantum world cannot be observed by the tester equipment that operates on the measured signals (as in a classical physics world). Therefore, only the externally measured classical signals $|0\rangle$, $|1\rangle$ are observed and measured at the input to the Tester Program. We know, however, from the symbolic (in general complex) output value what are the binary vector values that can occur on the circuit output and with what probabilities they are occurring there. Therefore, all possible measurement vectors with their probabilities can be known in advance before the measurement. If these measurement values include the correct output vector (of a non-faulty circuit) the corresponding test vectors (inputs) are called the probabilistic tests, otherwise the input vectors are called the deterministic tests. If the output vectors are the same in the faulty and non-faulty circuits then their corresponding input vector cannot be used as a test for this fault. This is represented by a zero or a blank cell in the Fault Table. Fault table is created as in [7] but it has also probabilistic (fractional) values in its cells.

If the outputs are "deterministic", we apply test vectors and detect the fault using standard deterministic approach to testing. If the outputs are "probabilistic" (complex numbers denoted by symbolic values like V_0 and V_1 in this example), we calculate the probability of occurrence of the observed output as explained in the following sections. While solving the "probabilistic set covering

problem” we give priority to deterministic tests. The same is true while creating the probabilistic adaptive tree. Observe that a deterministic fault in quantum circuit can be observed on the output probabilistically.

4.2. Probability calculation of the random output

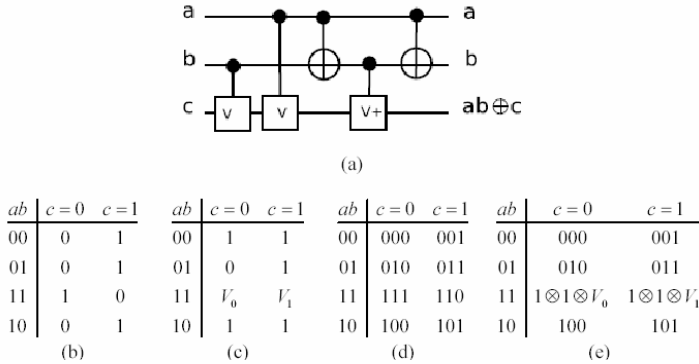


Figure 4. (a) Realization of a Toffoli gate from Controlled V, Controlled V⁺ and Feynman gates. (b) Kmap of the fault free output f for circuit from Figure 6, (c) the Kmap of the same output f when there is a gate CV removal fault of the first gate from left, (d) binary output signals of a correct circuit, (e) symbolic faulty outputs with probabilistic tests for the same fault.

By iteratively applying the same input test vector (a probabilistic test) we are calculating the probability of getting the observed output. The input vectors are always vectors of basis states. Each of the successive iterations of applying the probabilistic test reduces the probability of obtaining a correct measurement for a faulty circuit. For five iterations the probability of obtaining a correct measurement in presence of a given fault is reduced to 1/32. We say that the *test accuracy* of 1/32 requires 5 repetitions of test 110. Similarly for six iterations it is 1/64 and for eight iterations it is 1/256 (See Figure 5a). Hence, the greater the number of iterations the lesser is the probability of getting the correct measurement for faulty circuit. Suppose that we use test 110 for fault of gate removal as in Figure 4a. According to Fig. 4d the correct output should be 111 and according to Figure 4e the faulty output is 11V₀, which means 110 or 111 with equal probabilities of 1/2 are measured. If we tested eight times and we get |1> in bit f each time, we have the probability 255/256 that there is no fault of removing the first CV gate. Of course, in this particular case we should apply deterministic tests such as a'b'c' or ab'c' because they are possible. The setup from Figure 5b is used. In general, depending on a circuit, fault types, and their location, probabilistic tests may not exist, or all tests may be probabilistic as special cases. Usually, part of tests is

deterministic and part is probabilistic. The number of iterations should depend on the expected accuracy and cost of testing. This will lead to the generalized probabilistic “quantum covering problem” [17,18].

4.3. Repeated measurements in different bases.

When one knows what are all the possible faulty values, the probabilistic test can be replaced with a deterministic test in a different measurement base. As we remember from Figure 2, gate V⁺ converts the probabilistically measurable values |V₀> and |V₁> to the deterministically measurable values |0> and |1>, respectively. Similarly for gate V (see Figure 2). Thus if the bulk technology measurement is “value other than |0> or |1>” and we know that the faulty value in quantum wire just before the measurement can be only in set {|V₀>, |V₁>} we apply an additional measurement base in which gate V⁺ precedes the standard measurement gate. The first gate converts thus values |V₀>, |V₁> to |0> and |1>. This is done in a second measurement (see Figure 5c). The entire measurement procedure is then the following. (1) Set the input signals to the test value. (2) do the standard measurement (Fig. 5b) (3) if the measured value is |0> or |1>, terminate, else (3) insert gate V⁺ before the measurement gate to the circuit, (4) set the input values to the same test value for the second time, (5) do the measurement in the new measurement base with gate V⁺ inserted (Fig. 5c), (6) From the second measurement, determine if the complex amplitude value was |V₀> or |V₁>.

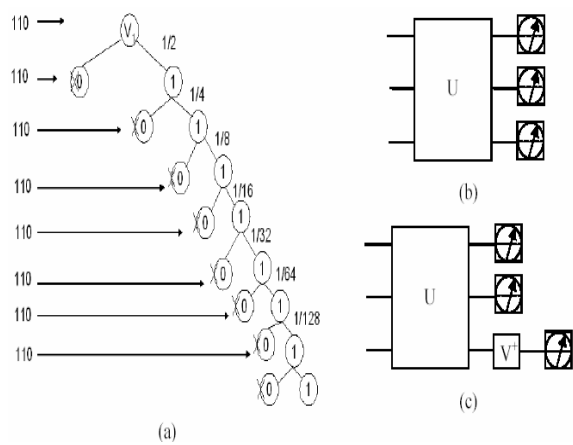


Figure 5. (a) Probabilistic Supernode – a tree for calculating the probability of obtaining a sequence of n signals “1” from gate which has probability 1/2 of output “1”, (b) Measurement in normal measurement base, (c) Measurement in modified base in which gate V⁺ is inserted before the measurement gate in the lowest bit.

As we see, the repeated probabilistic test in standard measurement base can be in this case replaced with two deterministic tests in a modified measurement base. This trade-off property is fundamental to all kinds of test generation and fault localization procedures for quantum circuits.

5. Generation of Test Sets and Adaptive Trees for Quantum Circuits

For binary quantum circuits our approach is very efficient since we use a technique for gate-level simulation of quantum circuits that uses new data structure called Quantum Information Decision Diagrams (QuiDDs), Viamontes et al [14,15,25]. Program QuiDPro that we use is based on QuiDDs, which are generalizations of Algebraic Decision Diagrams which in turn generalize the Binary Decision Diagrams, well-known for their ability to efficiently represent many problems.

With respective fault model the approach can be used to arbitrary multiple-valued quantum circuits and multiple-valued reversible (non-quantum) circuits [8,28,24]. Because we do not know yet how to convert QuiDPro to ternary logic, we wrote another software package for ternary quantum circuits [16] in which the basis states are $|0\rangle$, $|1\rangle$ and $|2\rangle$. We used there standard realization of matrix operations to implement matrix and Kronecker multiplications on unitary and non-unitary matrices [10]. Because these operations are repeated many times, the speed of this program variant suffers and we can handle only 3-qutrit (ternary) circuits.

Quaternary quantum logic circuits are realized in Hilbert space [8] using the model with values $\{|0\rangle, |1\rangle, |V_0\rangle, |V_1\rangle\}$ similar to the one presented above. In this model two measurements (as in sec. 4.3) are necessary to read any standard logic value in 4-valued logic [8], and the same is true for testing faulty circuits. The methods presented here can be adapted for test generation and fault localization also for this logic. *In all these variants, if possible, deterministic tests are first selected, while covering faults with tests, in order to shorten the total length of the test sequence. The solution (test set or a tree) is found, for any type of measurement gates, with arbitrary assumed accuracy. The system allows in principle to generate test sequences and adaptive fault localization trees for medium-size binary quantum (~ 20 qubits) and 3-qubit ternary quantum circuits.*

6. Conclusion

This paper presents a new approach to test generation and fault localization for quantum binary circuits.

Although all our examples were permutative circuits, the presented method can be applied with no difference to non-permutative (truly quantum) circuits, such as those used by a quantum source emitting entangled pairs on a quantum channel. We use in a uniform way the gate removal/gate insertion model with repeated initializations and measurements of various types, and in various bases. Our preliminary results are very promising – we showed on several reversible benchmark functions that they can be tested with smaller number of tests in quantum than in classical realization.

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