On Universality of General Reversible Multiple-Valued Logic Gates

Pawel Kerntopf
Institute of Computer Science
Department of Electronics
and Information Technology
Warsaw Univ. of Technology
Nowowiejska 15/19
00-665 Warsaw, Poland
pke@ii.pw.edu.pl

Marek A. Perkowski
Department of Electrical
and Computer Engineering
Portland State University
1900 SW 4th Avenue
Portland, OR 97201, USA
mperkows@ee.pdx.edu

Mozammel H. A. Khan
Department of Computer
Science and Engineering
East West University
45 Mohakhali, Dhaka 1212
Bangladesh
mhakhan@ewubd.edu,

Abstract

A set of p-valued logic gates (primitives) is called universal if an arbitrary p-valued logic function can be realized by a logic circuit built up from a finite number of gates belonging to this set. In the paper, we consider the problem of determining the number of universal single-gate libraries of p-valued reversible logic gates with two inputs and two outputs under the assumption that constant signals can be applied to arbitrary number of inputs. We have proved some properties of such gates and established that over 97% of ternary gates are universal.

1. Introduction

The *universality* (or *completeness*) of sets of binary and multiple-valued functions and related problems have been studied for many years and by many researchers (the survey [26] published in 1977 contains 464 references). The research has been conducted in three areas: propositional calculus of logics, universal algebras and logic (switching) circuits.

The universality of logic gates (primitives) depends on the technology because it has to take into account some additional constraints. It may differ from the notion of functional completeness studied by mathematicians and for this reason sometimes is called elemental universality [11]. This area has been gradually evolving. Initially, it dealt exclusively with delay-less combinational circuits [18]. Later, delays have also been taken into account as well as universality of sequential primitives was considered (including asynchronous behavior) [21, 11]. With technological changes new types of universality have been introduced, e.g. corresponding to double-rail circuits [12].

Although studies of reversible computing were initiated in the 1960s [17, 2] and a number of universal reversible logic gates have been proposed, general problems of universality of such gates have attracted the attention of researchers only very recently. Few papers have been devoted so far to universality of reversible gates and they consider almost exclusively binary gates [28, 7, 13]. In this paper, we are concerned entirely with universality of general multiple-valued reversible gates. Such MV gates are experimentally feasible in the context of the ion trap scheme for quantum computing [19].

A gate (or a circuit) is called *reversible* if there is a one-to-one correspondence between its input and output assignments, i.e. not only the outputs can be uniquely determined from the inputs, but also the inputs can be recovered from the outputs. In other words, a gate is reversible if it is information-lossless (or invertible). Using reversible logic circuits enables avoiding energy losses in digital devices [17, 10, 2, 5, 6, 9]. It is a fast developing area of research due to its increasing importance to future computer technologies, especially quantum ones [8] because of possibility to solve some exponentially hard problems in polynomial time [3]. During the last four years over 40 papers have been published on reversible computing, some of them proposing new multiple-valued gates [25, 23, 7, 1, 22, 24, 14, 15]. To solve the important practical problem of designing circuits built from such gates we should first establish which multiple-valued gates are universal.

Let us call a gate with n inputs and m outputs an $n*m$-gate. Some of the binary reversible gates considered in the literature have different number of inputs and outputs, e.g. 2*3 "switch gate" and 2*4 "interaction gate" [10] (also considered earlier as magnetic bubble logic gates [16, 27]). However, usually it is assumed that a reversible gate has the same number of inputs and outputs.

Proceedings of the 34th International Symposium on Multiple-Valued Logic (ISMVL'04)
0195-623X/04 $20.00 © 2004 **IEEE**

The output rows of the truth table of a reversible gate can be obtained by permutation of the input rows. Thus, there are equal numbers of all values in the function vector (the column in the truth table of a gate) for each output function of a reversible gate. Functions having this property are called *balanced* [4].

Universality of general reversible gates differs from classical elemental universality because in reversible case

(1) most gates are multi-output instead of only one-output gates,
(2) a constant signal may be applied to an arbitrary number of inputs,
(3) fan-out of each output of reversible gates is equal to 1.

Thus we have to consider

(1) universality of sets of functions instead of single functions,
(2) weak completeness instead of strong completeness,
(3) gates having the property of replicating input signals at the gate outputs.

Compositional properties of binary and multiple-valued reversible gates are different. There exist single universal binary reversible $k*k$ gates only for $k \geq 3$ [29]. It is so because the set of 2-variable balanced Boolean functions is equal to {EXCLUSIVE-OR, EQUIVALENCE} and that set is not weak complete. Over 97% of binary reversible 3*3 gates and almost 100% of reversible 4*4 gates are universal [13] in spite of the reversibility constraint. However, in contrast to binary logic, there exist ternary 2*2 gates that are universal. The number of ternary reversible 2*2 gates is 9 times greater than the number of binary reversible 3*3 gates (9! in comparison with 8!). Thus, one could expect that the percentage of universal gates among all ternary 2*2 gates is smaller than in the binary case for 3*3 gates. For establishing universality of a binary reversible gate it is sufficient to check weak completeness of the set of the gate output functions. Namely, it has been proved in [13] that all gates with this property can duplicate input signals. This result does not hold for multiple-valued reversible gates. For this reason we have introduced a new property of gates called quasi-replicating. Using this notion it was possible to obtain results allowing experimental estimation of the number of universal ternary reversible 2*2 gates. We have established that over 97% of such gates are universal.

The rest of the paper is organized as follows. In Section 2, basic notions of reversible gates are defined. Section 3 introduces the notion of universality of p-valued reversible gates (called *r-universality*, in short) and presents results of counting the number of r-universal ternary reversible 2*2 gates. Finally, in Section 4, conclusions are made.

2. Preliminaries

Let $P = \{0,1, \dots, p-1\}$. A mapping $f: P^n \rightarrow P$ will be called an *n-variable p-valued function*. If p=3, then f is called *ternary*. To represent a ternary function $f(x)$ we use the vector of the function values written as a string. For example, a 1-variable function will be represented by $a_0\ a_1\ a_2$, where $a_i = f(i)$, and the identity function $f(x) = x$ by the string 012. Similarly, to represent a 2-variable ternary function $f(x_1,x_2)$ the string $a_0\ a_1\ a_2\ a_3\ a_4\ a_5\ a_6\ a_7\ a_8$ will be used, where $f(j,k) = a_{3j+k}$. For example, the function $f(x_1,x_2) = x_1+x_2$ (mod 3) will be represented by 012120201.

Definition 1 A set F of p-valued functions is

- *complete* (strong complete, Sheffer) if an arbitrary p-valued function $f(x_1,\dots,x_n)$ can be realized by a loop-free combinational circuit built up of logic gates realizing functions from F and using $x_1, \dots, x_n$ as primary inputs,
- *weak complete* (complete with constants, pseudo-Sheffer) if an arbitrary p-valued function $f(x_1,\dots,x_n)$ can be realized by a loop-free combinational circuit built up of logic gates realizing functions from F and using 0, 1, … , p-1, $x_1, \dots, x_n$ as primary inputs.

Definition 2 Let $w_i(f)$ denote the number of input assignments X for which $f(X) = i$. An n-variable p-valued function f is called *balanced* iff $w_i(f) = p^{n-1}$ for each i, i.e. f is equal to each value belonging to the set $\{0,1, \dots, p-1\}$ the same number of times.

There are six 1-variable balanced ternary functions. They are represented by strings 012, 021, 102, 120, 201, 210 and corresponds to S_3, the symmetric group on three marks. The function $f(x_1,x_2) = x_1+x_2$ (mod 3) is one of 1,680 2-variable balanced ternary functions.

Definition 3 A p-valued gate (or a circuit) is *reversible* iff there is a one-to-one correspondence between the input and the output assignments, i.e. if in the truth table of the gate (or the circuit) there is a distinct output row for each input row.

Note that every output function of a reversible gate is balanced and that the reversibility property of gates is preserved under permutations of inputs and/or outputs. We will consider only the gates with the same number of inputs and outputs.

A gate with k inputs and k outputs will be called a $k*k$-gate. There exist six ternary reversible 1*1 gates (they have the same truth tables as 1-variable balanced ternary functions). As mentioned earlier, only 1,680 out of 3^9=19,683 2-variable ternary functions are balanced.

The number of pairs of balanced ternary functions is equal to $1{,}680^2 = 2{,}822{,}400$. However, not every pair of balanced functions may appear in a ternary reversible 2*2 gate (see Example 1). Namely, the number of ternary reversible 2*2 gates is equal to 9! = 362,880 (the number of permutations of nine rows in the truth table of a ternary reversible 2*2 gate).

Definition 4 Two balanced p-valued functions f, g are called *r-compatible* if for all input assignments $(a_1, \ldots, a_n)$ the pairs of their values $\langle f(a_1,\ldots,a_n), g(a_1,\ldots,a_n)\rangle$ are equal the same number of times to each of the pairs $\langle j.k\rangle$, $0 \le j,k \le p\text{-}1$.

Example 1 Let the capital letters A, B denote inputs, and P, Q denote outputs of a ternary reversible 2*2 gate. Table 1 shows an example of a pair of balanced functions that are not r-compatible. Namely, in the output rows of Table 1 each of the pairs <0,0>, <1,2> and <2,1> appears twice, each of the pairs <0,1>, <1,0> and <2,2> appears once, while the pairs <0,2>, <1,1> and <2,0> are missing.

Table 1. Pair of ternary balanced functions that are not r-compatible

A	B	P	Q
0	0	0	0
0	1	1	2
0	2	1	0
1	0	0	1
1	1	1	2
1	2	0	0
2	0	2	1
2	1	2	1
2	2	2	2

Lemma 1 Two functions belonging to the set of output functions of a p-valued reversible gate are r-compatible.
Proof. All p^n output rows in the truth table of a reversible $n*n$ gate are distinct. Thus for each pair of output functions f, g all pairs of values of these functions $\langle f(a_1,\ldots,a_n), g(a_1,\ldots,a_n)\rangle$ appear in the output part of the gate the same number of times. Hence, the pair f, g is r-compatible.

Lemma 2 All output functions of a p-valued reversible gate are distinct.
Proof. Let us assume that there exists a p-valued reversible gate with two identical output functions. In the two identical output columns corresponding to the functions only the following pairs of values appear: <0,0>, <1,1>, ... , <p-1,p-1>. Such two functions are not r-compatible. By Lemma 1 we obtain a contradiction. Hence, Lemma 2 holds.

3. Universality of multiple-valued reversible 2*2 gates

Definition 5 A p-valued reversible $n*n$ gate (or circuit) has *duplicating property* (*D-property*, in short) iff there exists a sequence of $n\text{-}1$ constants $a_1, \ldots, a_{i-1}, a_{i+1}, \ldots, a_n$ and two output functions of the gate (circuit) $f_j(x_1,x_2,\ldots,x_n)$ and $f_k(x_1,x_2,\ldots,x_n)$ such that

$f_j(a_1,\ldots,a_{i-1},x_i,a_{i+1},\ldots,a_n) = f_k(a_1,\ldots,a_{i-1},x_i,a_{i+1},\ldots,a_n) = x_i$.

Example 2 Table 2 shows the truth table of a ternary reversible 2*2 gate (circuit) having D-property. It is easy to notice that for $A = 0$ the values at both gate outputs P and Q are equal to the value at the input B:

$$P = B \qquad Q = B.$$

Table 2. Ternary reversible 2*2 gate having D-property

A	B	P	Q
0	0	0	0
0	1	1	1
0	2	2	2
1	0	0	1
1	1	1	2
1	2	0	2
2	0	2	1
2	1	1	0
2	2	2	0

Definition 6 A p-valued reversible $n*n$ gate (or circuit) has *quasi-duplicating property* (*qD-property*, in short) iff it does not have D-property and there exists a sequence of $n\text{-}1$ constants $a_1, \ldots, a_{i-1}, a_{i+1}, \ldots, a_n$ and two output functions of the gate $f_j(x_1,x_2,\ldots,x_n)$ and $f_k(x_1,x_2,\ldots,x_n)$ such that each of the 1-variable functions

$f_j(a_1,\ldots,a_{i-1},x_i,a_{i+1},\ldots,a_n)$ and $f_k(a_1,\ldots,a_{i-1},x_i,a_{i+1},\ldots,a_n)$

is balanced, i.e. takes all values 0,1, ... , p-1.
Example 3 Table 3 shows the truth table of a ternary reversible 2*2 gate (circuit) having qD-property. It is easy to notice that for $B = 0$ the output functions P and Q have the representations 012 and 201, respectively.

Table 3. Ternary reversible 2*2 gate having qD-property

A	B	P	Q
0	0	0	2
0	1	0	0
0	2	0	1
1	0	1	0
1	1	1	1
1	2	2	0
2	0	2	1
2	1	1	2
2	2	2	2

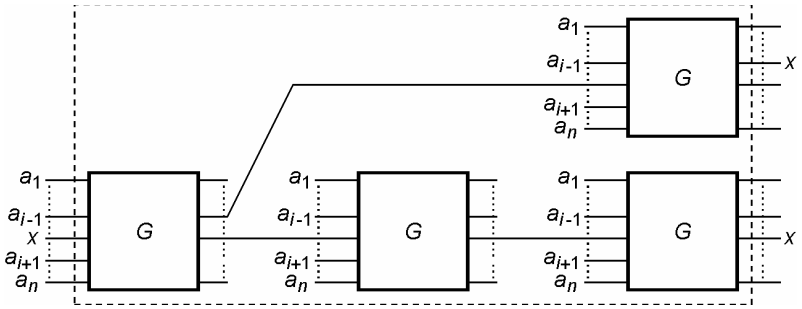

Fig. 1 Example of a circuit with D-property built using gates G with qD-property

Theorem 1 If G is a p-valued reversible $n*n$ gate with qD-property, then a p-valued circuit with D-property can be built from gates G.

Proof Let $p = 3$. If f is a 1-variable ternary function and $f^2(x) = f(f(x))$, $f^3(x) = f(f^2(x))$, then $f^2(x) = x$ for f belonging to A_1={021, 102, 210}, and $f^3(x) = x$ for f belonging to A_2={120, 201}. Assume that a ternary reversible $n*n$ gate G has qD-property. Then there exist $n-1$ constants $a_1, \ldots, a_{i-1}, a_{i+1}, \ldots, a_n$ and two output functions of the gate $f_j(x_1,x_2,\ldots,x_n)$ and $f_k(x_1,x_2,\ldots,x_n)$ such that each of the functions $f_j(a_1,\ldots,a_{i-1},x_i,a_{i+1},\ldots,a_n)$ and $f_k(a_1,\ldots,a_{i-1},x_i,a_{i+1},\ldots,a_n)$ takes all three values 0,1,2. First, we will consider an example. Let the representation of $f_j(a_1,\ldots,a_{i-1},x_i,a_{i+1},\ldots,a_n)$ belong to A_1 and the representation of $f_k(a_1,\ldots,a_{i-1},x_i,a_{i+1},\ldots,a_n)$ belong to A_2. Fig. 1 shows a circuit with D-property built using exclusively gates G. In general, if the representation of the function $f_m(a_1,\ldots,a_{i-1},x_i,a_{i+1},\ldots,a_n)$, where $m = j$ or k, belongs to A_1 (A_2), then we construct a sequence of two (three) gates in which the j-th output of the first gate is connected to the i-th input of the second gate (the k-th output of the first gate is connected to the i-th input of the second gate and k-th output of the second gate is connected to i-th input of third gate). When the first gate is common for the two sequences, then the signal at the j-th output of one sequence and the signal at the k-th output of the other sequence are both equal to the i-th input of the common gate. Thus Theorem 1 holds in ternary case. The proof for $p > 3$ is similar (based on properties of permutation groups). Let the orders of $f_j(a_1,\ldots,a_{i-1},x_i,a_{i+1},\ldots,a_n)$ and $f_k(a_1,\ldots,a_{i-1},x_i,a_{i+1},\ldots,a_n)$ be m_j and m_k, respectively, and let m be the least common multiple of m_j and m_k. Then $f_j^m(a_1,\ldots,a_{i-1},x_i,a_{i+1},\ldots,a_n)$ and $f_k^m(a_1,\ldots,a_{i-1},x_i,a_{i+1},\ldots,a_n)$ are both the identity on x_i.

It is also possible to build up a circuit with qD-property (and by Theorem 1 also a circuit with D-property) using multiple-valued gates not having qD-property as shown in the example below.

Example 4 Table 4 shows the truth table of a ternary reversible 2*2 gate G not having qD-property. Fig. 2 presents a circuit with qD-property built up using such gates. Thus it is also possible to build up a circuit with D-property using gates G.

Table 4. Ternary reversible 2*2 gate not having qD-property

A	B	P	Q
0	0	0	2
0	1	0	0
0	2	0	1
1	0	1	1
1	1	1	0
1	2	2	0
2	0	2	1
2	1	1	2
2	2	2	2

Definition 7 A p-valued reversible gate G is *r-universal* iff an arbitrary p-valued function $f(x_1,\ldots,x_n)$ can be realized by a loop-free combinational circuit built up of a finite number of copies of the gate G using constants an arbitrary number of times and using each signal $x_1, \ldots, x_n$ at most once as primary inputs.

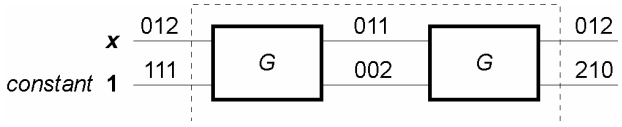

Fig. 2 Circuit with qD-property built up using gate G not having qD-property

Theorem 2 If the set of all output functions of a p-valued reversible gate G is weak complete and it is possible to built a p-valued circuit having qD-property built up of gates G, then G is r-universal.

Proof. Classical proofs of universality (e.g., see [18]) are based on the assumption that each signal may be used an arbitrary number of times as a primary input and that operations of a canonical form can be realized using primitives. It is sufficient to follow these arguments to prove Theorem 2. When it is possible to build up a circuit having qD-property from gates G, then by Theorem 1 it is also possible to build up a circuit with D-property from gates G. This is equivalent to the assumption that each signal may be used any number of times. When the set of output functions of the gate G is weak complete, then circuits realizing operations of a canonical form can be built up from gates G. Hence, Theorem 2 holds.

4. Experimental results

To find all ternary reversible 2*2 gates having a weak complete set of output functions we used the following result [20]. A ternary 2-variable function f is weak complete iff using f and the constants it is possible to generate:

a) two permutations that form a basis of the symmetric group S_3, and
b) a 1-variable function which assumes exactly two values

Let us remind that a basis of S_3 consists of one of: 120, 201; and one of: 021, 210, 102.

Let f denote the ternary function under examination and let us define the following sets:

- C_0 contains the variable 012 and the three constant functions 000, 111, 222,
- C_{s+1} contains all functions $f(g_1,g_2)$ not belonging to C_r, $r \leq s$, where one of the functions g_1, g_2 is an element of C_s and the other is an element of C_r, $r \leq s$.

The procedure for checking whether a ternary 2-variable function [20] is weak complete forms sets C_i until one of two stopping conditions is satisfied:

(i) for some k, a basis of S_3 and a 1-variable function which assumes exactly two values are included in the union of all sets C_i, $i \leq k$, in which case the given function is weak complete,
(ii) for some k, the set C_k is empty in which case the given function is not weak complete.

Example 5 Let us consider the output function P of the gate defined in Table 2: C_0 = {012, 000, 111, 222}, C_1 = {002, 010, 202, 212}, C_2 is empty. Thus the function P is not weak complete because it does not include a basis of S_3.

Now let us consider the output function Q of the gate defined in Table 2:
C_0 = {012, 000, 111, 222}
C_1 = {011, 020, 100, 120, 122, 220}
The function with two values (e.g., 011) and the generator 120 of S_3 are included in C_1. The second generator 021 belongs to C_2 as it can be obtained by the composition $f(g_1,g_2)$, where g_1 = 011, g_2 = 020. Thus Q is weak complete.

We have run a program based on the above procedure and have established that 1605 out of all 1680 balanced ternary 2-variable functions (i.e., 95.5%) are weak complete.

Let us note that it is easy to extend the above procedure for checking weak completeness of sets consisting of both output functions of a ternary reversible 2*2 gate as well as for checking weak completeness of output functions of sets of gates.

By exhaustive checking of all ternary reversible 2*2 gates we have found that 132,768 of them have D-property. Then we have checked how many of the rest of the gates has qD-property. From each such gate we have built cascade circuits (allowing wire crossing) to check whether the second condition of Theorem 2 has been fulfilled. Because the number of these cascade circuits grows exponentially with the number of levels we have limited the calculations of cascades with not more than 12 levels. On the basis of Theorem 2 we were able to establish that among 362,880 ternary reversible 2*2 gates at least 353,214 (97.34%) are r-universal. The rest of the gates either have the set of output functions which is not weak complete or have a weak complete set of output functions, but we were not able to find cascade circuits with qD-property built up from those gates.

5. Conclusions

We have proved some properties of multiple-valued reversible gates related to their universality. By exhaustive calculations we have established that over 97% of all ternary reversible 2*2 gates are r-universal. It is clear that for values of p greater than 3 such percentages will be even larger. As there are so many universal gates the circuit designers have a lot of freedom in finding gates with good physical implementations (e.g. minimum cost). Some multiple-valued reversible gates have already been proposed [19, 22, 24, 14, 15].

Theorem 2 gives a sufficient condition for r-universality. However, we do not know whether it is also a necessary condition. It is an interesting open problem.

6. References

[1] A. Al-Rabadi, *Novel Methods for Reversible Logic Synthesis and Their Application to Quantum Computing*, Ph.D. Thesis, Portland State University, Portland, Oregon, 2002.

[2] C. H. Bennett, "Notes on the History of Reversible Computation," *IBM J. Res. Dev.*, Vol. 30, pp.16-23, 1988.

[3] C. H. Bennett and D. P. DiVincenzo, "Quantum Information and Computation," *Nature*, Vol. 404, pp. 247, 2000.

[4] K. Chakrabarty and J. P. Hayes, "Balanced Boolean Functions," *IEE Proceedings – Computers and Digital Techniques*, Vol. 145, pp. 52-62, 1998.

[5] A. De Vos, "Towards Reversible Digital Computers," *Proc. European Conf. on Circuit Theory and Design*, Vol. 2, pp. 923-931, 1997.

[6] A. De Vos, "Reversible Computing," *Progress in Quantum Electronics*, Vol. 23, pp. 1-49, 1999.

[7] A. De Vos, B. Raa and L. Storme, "Generating the Group of Reversible Logic Gates," *Journal of Physics A: Mathematical & General*, Vol. 35, pp. 7063-7078, 2002.

[8] R. Feynman, "Quantum Mechanical Computers," *Optics News*, Vol. 11, pp. 11-20, 1985.

[9] M. P. Frank, *Reversibility for Efficient Computing*. Ph.D. Thesis, Massachusetts Institute of Technology (MIT), Cambridge, MA, 1999.

[10] E. Fredkin and T. Toffoli, "Conservative Logic," *Int. Journal of Theoretical Physics*, Vol. 21, pp. 219-253, 1982.

[11] K. Inagaki, "Elemental Universality of Sets of Logic Devices," *IEICE Trans. on Inf. & Syst.*, Vol. E81-D, pp. 767-772, 1998.

[12] S. Karunanithi and A. D. Friedman, "Some New Types of Logical Completeness," *IEEE Trans. on Computers*, Vol. C-27, pp. 998-1005, 1978.

[13] P. Kerntopf, "On Universality of Binary Reversible Logic Gates," *Proc. 5th Int. Workshop on Boolean Problems*, pp. 47-52, 2002.

[14] M. H. A. Khan, M. Perkowski and P. Kerntopf, "Multi-Output Galois Field Sum of Product (GFSOP) Synthesis with New Quantum Cascades," *Proc. 33rd IEEE Int. Symposium on Multiple-Valued Logic*, pp. 146-153, 2003.

[15] M. H. A. Khan, M. Perkowski, R. Khan and P. Kerntopf, "Ternary GFSOP Minimization using Kronecker Decision Diagrams and Their Synthesis with Quantum Cascades," submitted to *Journal of Multiple-Valued Logic and Soft Computing*, 2003.

[16] K. Kinoshita, T. Sasao and J. Matsuda, "On Magnetic Bubble Logic Circuits," *IEEE Trans. on Computers*, Vol. C-25, pp. 247-253, 1976.

[17] R. Landauer, "Irreversibility and Heat Generation in the Computing Process," *IBM J. Res. Develop.*, Vol. 3, pp. 183-191, 1961.

[18] A. Mukhopadhyay, "Complete Sets of Logic Primitives", in *Recent Developments in Switching Theory* (edited by A. Mukhopadhyay), Academic Press, pp. 1-26, 1971.

[19] A. Muthukrishnan and C. R. Stroud Jr., "Multivalued Logic Gates for Quantum Computation," *Physical Review A*, Vol. 62, pp. 052309.1-8, 2000.

[20] J. C. Muzio, „Ternary Two-Place Functions that are Complete with Constants," *Proc. 5th Int. Symposium on Multiple-Valued Logic,* pp. 27-33, 1975.

[21] A. Nozaki, "Complete Sets of Switching Elements and Related Topics," *Proc. 1st USA-JAPAN Computer Conf.,* pp. 12.5.1-4, 1972.

[22] M. Perkowski, A. Al-Rabadi and P. Kerntopf, "Multiple-Valued Quantum Logic Synthesis," *Proc. Int. Symp. on New Paradigms VLSI Computing*, Sendai, Japan, pp.41-47, 2002.

[23] M. Perkowski, A. Al.-Rabadi, P. Kerntopf, A. Mishchenko and M. Chrzanowska-Jeske, "Three-Dimensional Realization of Multi-Valued Functions using Reversible Logic," *Proc. 10th Int. Workshop on Post-Binary Ultra-Large-Scale Integration Systems*, pp. 47-53, 2001.

[24] M. Perkowski, P. Kerntopf, A. Al.-Rabadi, M. H. A. Khan, "Multiple-Valued Quantum Computing. Issues, Open Problems, Solutions," *Technical Report*, Korea Advanced Institute of Science and Technology (KAIST), Taejeon, Korea, 2002.

[25] P. Picton, "A Universal Architecture for Multiple-Valued Reversible Logic," *Multiple-Valued Logic Journal*, Vol. 5, pp. 27-37, 2000.

[26] I. G. Rosenberg, „Completeness Properties of Multiple-Valued Logic Algebras," in *Computer Science and Multiple-Valued Logic. Theory and Applications* (edited by D. C. Rine), North-Holland Publishing Co., pp. 144-186, 1977.

[27] T. Sasao and K. Kinoshita, "Conservative Logic Elements and Their Universality," *IEEE Trans. on Computers*, Vol. C-28, pp. 682-685, 1979.

[28] L. Storme, A. De Vos, and G. Jacobs, "Group Theoretical Aspects of Reversible Logic Gates," *Journal of Universal Computer Science*, Vol. 5, pp. 307-321, 1999.

[29] T. Toffoli, „Reversible Computing", in *Automata, Languages and Programming* (edited by de J. W. Bakker and J. van Leeuwen), Springer Verlag, pp. 632-644, 1980.