On Universality of Ternary Reversible Logic Gates

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Abstract

A set of *p*-valued logic gates (primitives) is called universal if an arbitrary *p*-valued logic function can be realized by a logic circuit built up from a finite number of gates belonging to this set. In the paper, we consider the problem of determining the number of universal ternary reversible logic gates with two inputs and two outputs. We have established that over 97% of such gates are universal. Some of the theoretical results are also valid for arbitrary *p*-valued reversible logic gates.

1. Introduction

The *universality* (or completeness) of sets of binary and multiple-valued functions and related problems have been studied for many years and by many researchers in three areas: propositional calculus of logics, universal algebras and logic (switching) circuits ([49] contains 464 references). The universality of logic gates (primitives) depends on the technology because it has to take into account also some constraints. It may differ from the notion of functional completeness studied by mathematicians and for this reason sometimes is called elemental universality [19]. This area has been gradually evolving. Initially, it dealt with delay-less combinational circuits exclusively [37]. Later, delays have also been taken into account as well as universality of sequential primitives was considered (including asynchronous behavior) [19, 40]. With technological changes new types of universality have been developed, e.g. corresponding to double-rail signals [21].

Although studies of reversible computing were initiated in the 1960s [31, 6] and a number of universal reversible logic gates have been proposed, general problems of universality of such gates have attracted the attention of researchers only very recently. Few papers have been devoted so far to universality of reversible gates and they consider almost exclusively binary gates [52, 14, 26]. In this paper, we are concerned entirely with universality of general ternary reversible gates.

A gate (or a circuit) is called *reversible* if there is a one-to-one correspondence between its input and output assignments, i.e. not only the outputs can be uniquely determined from the inputs, but also the inputs can be recovered from the outputs. In other words, a gate is reversible if it is invertible or information-lossless. Using reversible logic circuits enables avoiding energy losses in digital devices [31, 18, 6, 10, 11, 17]. It is a fast developing area of research due to its increasing importance to future computer technologies, especially quantum ones [16] because of possibility to solve some exponentially hard problems in polynomial time [7]. For example, during the last three years many papers have been written on reversible computing [1-5, 8, 12-15, 20, 22-26, 28-30, 32-36, 41-48, 51, 54, 55], some of them proposing new multiple-valued gates [48, 42, 5, 14, 1-3, 41, 44, 30]. In designing circuits built from such gates it is important to know which of the gates have the least cost. Solving this practical problem we should first establish how many multiple-valued gates are universal.

Let us call a gate with *n* inputs and *m* outputs an *n*m*-gate. Some of the binary reversible gates considered in the literature have different number of inputs and outputs, e.g. 2*3 “switch gate” and 2*4 “interaction gate” [18] (also called I_B and II_B elements, respectively, in [27, 50]). However, usually it is assumed that a reversible gate has the same number of inputs and outputs. In this case, the output rows of the truth table of a reversible gate can be obtained by permutation of the input rows. Thus, there are equal numbers of all values in the function vector for each output function of a reversible gate (such functions are called *balanced* [9]).

Universality of reversible gates differs from classical elemental universality because in reversible circuits

(1) usually multi-output gates are considered instead of only one-output gates,
(2) a constant signal may be applied to an arbitrary number of inputs,
(3) reversible gates have fan-out of each output equal to 1.

Thus we have to consider

(1) universality of sets of functions instead of single functions,
(2) weak completeness instead of strong completeness,
(3) the property of replicating input signals at the gate outputs.

Compositional properties of binary and ternary reversible gates are different. Universal binary reversible $k*k$ gates exist only for $k \geq 3$ [53] (the set of 2-variable balanced Boolean functions is equal to {EXCLUSIVE-OR, EQUIVALENCE} and it is known that this set is not weak complete). Over 97% of binary reversible 3*3 gates and almost all reversible 4*4 gates are universal [26] in spite of the reversibility constraint. However, there exist ternary 2*2 gates that are universal. Moreover, the number of ternary reversible 2*2 gates is 9 times greater than the number of binary reversible 3*3 gates (9! in comparison with 8!). In binary case, for establishing universality of a gate it is sufficient to check weak completeness of the set of the gate output functions as it has been proved in [26] that all gates with this property are duplicating input signals. This result does not hold for ternary reversible gates. For this reason we have introduced a new property of gates called quasi-replicating. Using this notion it was possible to obtain experimental results allowing estimation of the number of universal ternary reversible 2*2 gates. Namely, also over 97% of such gates are universal.

The rest of the paper is organized as follows. In Section 2, we define basic notions of reversible gates. Section 3 introduces the notion of universality of reversible gates (called *r-universality*, in short). Section 4 presents results of counting the number of r-universal ternary reversible 2*2 gates. Finally, in Section 5, conclusions are made.

2. Preliminaries

Let $P = \{0,1, \dots, p\text{-}1\}$. A mapping $f: P^n \rightarrow P$ will be called an *n-variable p-valued function*. If p=3 then the function f is called *ternary*. To represent a 1-variable ternary function $f(x)$ we use the vector of the function values written as a string $a_0\ a_1\ a_2$, where $a_i = f(i)$. For example, the identity function $f(x) = x$ is represented by the vector 012. Similarly, to represent a 2-variable ternary function $f(x_1,x_2)$ the vector $a_0\ a_1\ a_2\ a_3\ a_4\ a_5\ a_6\ a_7\ a_8$ will be used, where $f(j,k) = a_{3j+k.}$ For example, the function $f(x_1,x_2) = x_1+x_2$ (mod 3) will be represented by the vector 012120201.

Definition 1 A set of p-valued functions F is

- *complete* (strong complete, Sheffer) if an arbitrary p-valued function $f(x_1,\dots,x_n)$ can be realized by a loop-free combinational circuit built up of logic gates realizing functions from F and using $x_1, \dots, x_n$ as primary inputs,
- *weak complete* (complete with constants, pseudo-Sheffer) if an arbitrary p-valued function $f(x_1,\dots,x_n)$ can be realized by a loop-free combinational circuit built up of logic gates realizing functions from F and using $0, 1, \dots, p\text{-}1, x_1, \dots, x_n$ as primary inputs.

Definition 2 Let $w_i(f)$ denotes the number of input assignments X for which $f(X) = i$. An n-variable p-valued function f is called *balanced* if $w_i(f) = p^{n-1}$ for each i, i.e. f is equal to each value belonging to the set $\{0,1, \dots, p\text{-}1\}$ the same number of times.

There are six 1-variable balanced ternary functions. They are represented by the vectors 012, 021, 102, 120, 201, 210 and corresponds to S_3, the symmetric group on three marks. The function $f(x_1,x_2) = x_1+x_2$ (mod 3) is one of 1,680 2-variable balanced ternary functions.

Definition 3 A p-valued gate (or a circuit) is *reversible* if there is a one-to-one correspondence between the input and the output assignments, i.e. if in the truth table of the gate or circuit there is a distinct output row for each input row.

Note that every output function of a reversible gate is balanced and that the reversibility property of gates is preserved under permutations of inputs and/or outputs. We will consider only the gates with the same number of inputs and outputs. A gate with k inputs and k outputs will be called a $k*k$-gate. There exist six ternary reversible 1*1 gates (they have the same truth tables as 1-variable balanced ternary functions). As mentioned earlier only 1,680 out of 3^9 =19,683 2-variable ternary functions are balanced. The number of pairs of balanced ternary functions is equal to $1{,}680^2$ = 2,822,400. However, the number of ternary reversible 2*2 gates is smaller: 9! = 362,880 (it is equal to the number of permutations of 9 rows in the truth table of a ternary reversible 2*2 gate) as not every pair of balanced functions may appear in a ternary reversible 2*2-gate (see Example 1).

Definition 4 Two balanced p-valued functions f, g are called *r-compatible* if for all input assignments $(a_1, \dots, a_n)$ the pairs of their values $\langle f(a_1,\dots,a_n), g(a_1,\dots,a_n)\rangle$ are equal the same number of times to each of the pairs $\langle j.k\rangle$, $0 \le j,k \le p$-1.

Example 1 Let the capital letters A, B denote inputs, and P, Q denote outputs of a ternary reversible 2*2 gate. Table 1 shows an example of a pair of balanced functions that is not r-compatible. Namely, in the output rows of Table 1 each of the pairs <0,0>, <1,2> and <2,1> appears twice, while the combinations <0,2>, <1,1> and <2,0> are missing.

TABLE 1
PAIR OF TERNARY BALANCED FUNCTIONS THAT IS NOT r-COMPATIBLE

A	B	P	Q
0	0	0	0
0	1	1	2
0	2	1	0
1	0	0	1
1	1	1	2
1	2	0	0
2	0	2	1
2	1	2	1
2	2	2	2

Lemma 1 Each pair of functions belonging to the set of output functions of a p-valued reversible gate is r-compatible.

Proof. All p^n output rows in the truth table of a reversible $n*n$ gate are distinct. Thus for each pair of output functions f, g all pairs of values of these functions $\langle f(a_1,\dots,a_n), g(a_1,\dots,a_n)\rangle$ appear in the output part of the gate the same number of times. Hence the pair f, g is r-compatible.

Lemma 2 All output functions of every p-valued reversible gate are distinct.

Proof. Let us assume that there exists a p-valued reversible gate with two identical output functions. In a pair of identical output columns only the following pairs of values appear: <0,0>, <1,1>, ... , <p-1,p-1>. Such a pair of functions is not r-compatible. By Lemma 1 we obtain a contradiction. Hence, Lemma 2 holds.

3. Universality of ternary reversible 2*2 gates

Definition 5 A p-valued reversible $n*n$ gate (or circuit) has *duplicating property* (*D-property*, in short) if there exist a sequence of n-1 constants $a_1, \dots, a_{i-1}, a_{i+1}, \dots, a_n$ and two output functions of the gate (circuit) $f_j(x_1,x_2,\dots,x_n)$ and $f_k(x_1,x_2,\dots,x_n)$ such that

$$f_j(a_1,\dots,a_{i-1},x_i,a_{i+1},\dots,a_n) = f_k(a_1,\dots,a_{i-1},x_i,a_{i+1},\dots,a_n) = x_i.$$

Example 2 Table 2 shows the truth table of a ternary reversible 2*2 gate (circuit) having D-property. It is easy to notice that for $A = 0$ we always obtain the same value at both gate outputs P and Q as at the input B:

$$P = B \qquad Q = B.$$

TABLE 2
TERNARY REVERSIBLE 2*2 GATE HAVING D-PROPERTY

A	*B*	*P*	*Q*
0	0	0	0
0	1	1	1
0	2	2	2
1	0	0	1
1	1	1	2
1	2	0	2
2	0	2	1
2	1	1	0
2	2	2	0

Definition 6 A *p*-valued reversible *n*n* gate (or circuit) has *quasi-duplicating property* (*qD-property*, in short) if it is has not D-property and there exist a sequence of *n-1* constants $a_1, \dots, a_{i-1}, a_{i+1}, \dots, a_n$ and two output functions of this gate $f_j(x_1,x_2,\dots,x_n)$ and $f_k(x_1,x_2,\dots,x_n)$ such that each of the functions

$$f_j(a_1,\dots,a_{i-1},x_i,a_{i+1},\dots,a_n) \quad \text{and} \quad f_k(a_1,\dots,a_{i-1},x_i,a_{i+1},\dots,a_n)$$

takes all values 0,1, ... , *p*-1.

Example 3 Table 3 shows the truth table of a ternary reversible 2*2 gate (circuit) having qD-property. It is easy to notice that for $B = 0$ the output functions *P* and *Q* have the representations 012 and 201, respectively.

TABLE 3
TERNARY REVERSIBLE 2*2 GATE HAVING qD-PROPERTY

A	*B*	*P*	*Q*
0	0	0	2
0	1	0	0
0	2	0	1
1	0	1	0
1	1	1	1
1	2	2	0
2	0	2	1
2	1	1	2
2	2	2	2

Theorem 1 If *G* is a *p*-valued reversible *n*n* gate with qD-property then a circuit with D-property can be built using exclusively gates *G*.

Proof Let us consider ternary case. If *f* is a 1-variable ternary function and $f^2(x) = f(f(x))$, $f^3(x) = f(f^2(x))$ then $f^2=f$ for *f* belonging to $A_1=\{021, 102, 210\}$, and $f^3=f$ for *f* belonging to $A_2=\{120, 201\}$. Assume that a ternary reversible *n*n* gate *G* has qD-property. Then there exists a sequence of *n-1* constants $a_1, \dots, a_{i-1}, a_{i+1}, \dots, a_n$ and two output functions of this gate $f_j(x_1,x_2,\dots,x_n)$ and $f_k(x_1,x_2,\dots,x_n)$ such that each of the functions $f_j(a_1,\dots,a_{i-1},x_i,a_{i+1},\dots,a_n)$ and $f_k(a_1,\dots,a_{i-1},x_i,a_{i+1},\dots,a_n)$ takes all three values 0,1,2. First, we will consider an example. Let the representation of $f_j(a_1,\dots,a_{i-1},x_i,a_{i+1},\dots,a_n)$ belongs to A_1 and the representation of $f_k(a_1,\dots,a_{i-1},x_i,a_{i+1},\dots,a_n)$ belongs to A_2. Fig. 1 shows a circuit with D-property built using exclusively gates G. In general, if the representation of the function $f_m(a_1,\dots,a_{i-1},x_i,a_{i+1},\dots,a_n)$, where $m = j$ or *k*, belongs to A_1 (A_2) then we construct a sequence of two (three) gates in which the *j*-th output of the first gate is connected to the *i*-th input of the second gate (the *k*-th outputs of the first and second gate are connected to the *i*-th input of the second and third gate, respectively). When the first gate is common for the two sequences then the signal at the *j*-th output of one sequence and the signal at the *k*-th output of the other sequence are both equal to the *i*-th input of the common gate. Thus Theorem 1 holds in ternary case. The proof for *p*-valued case is similar (based on properties of permutation groups). We are not including it due to the lack of space.

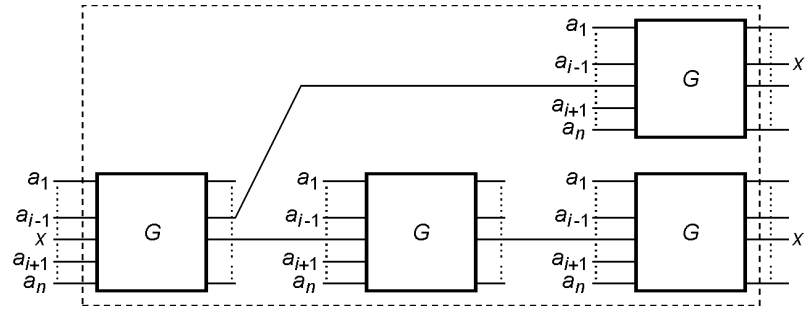

Fig. 1 Example of a circuit with D-property built using gates G with qD-property

It is possible to build up a circuit with qD-property (and by Theorem 1 also a circuit with D-property) using gates not having qD-property as shown in the example below.

Example 4 Table 4 shows the truth table of a ternary reversible 2*2 gate not having qD-property. Fig. 2 presents a circuit with qD-property built using such gates. Thus it is also possible to build up a circuit with D-property using circuits from Fig. 2.

TABLE 4
TERNARY REVERSIBLE 2*2 GATE NOT HAVING qD-PROPERTY

A	*B*	*P*	*Q*
0	0	0	2
0	1	0	0
0	2	0	1
1	0	1	1
1	1	1	0
1	2	2	0
2	0	2	1
2	1	1	2
2	2	2	2

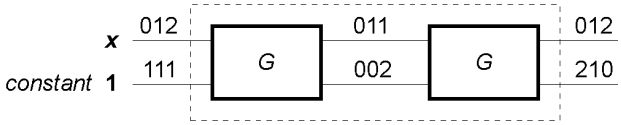

Fig. 2 Circuit with qD-property built up using gate G not having qD-property

Definition 7 A *p*-valued reversible gate *G* is *r-universal* if an arbitrary *p*-valued function $f(x_1,\ldots,x_n)$ can be realized by a loop-free combinational circuit built up of a finite number of copies of the gate *G* using constants an arbitrary number of times and using each signal $x_1, \ldots, x_n$ at most once as primary inputs.

Theorem 2 If for a *p*-valued reversible gate *G* it is possible to built a circuit having qD-property using gates *G* and the set of output functions of *G* is weak complete then *G* is *r-universal*.

Proof. Proofs of universality in classical case (see e.g. [37]) are based on the assumption that each input signal may be used an arbitrary number of times (i.e., arbitrary number of copies of primary inputs can be used). Then from a canonical form of a function it follows that a circuit realizing any function can be built. Thus it is sufficient to follow these arguments to prove Theorem 2. As it is possible to built a circuit having qD-property using gates *G* then by Theorem 1 it is possible to build a circuit with D-property using gates *G*. However, this is equivalent to the assumption that each signal may be used any number of times. Hence, Theorem 2 holds.

4. Experimental results

First we have run a program based on the procedure from [39] to find all ternary reversible 2*2 gates that are weak complete. Then for each such gate we have constructed cascade circuits (allowing wire crossing) to check whether conditions of Theorem 2 have been fulfilled. Because the number of these cascade circuits grows exponentially with the number of levels we have limited the calculations to 12 levels.

On the basis of Theorem 2 we were able to establish that among 362,880 ternary reversible 2*2 gates:

a) 353,214 (**97.34%**) **are r-universal**,

b) 1,934 (**0,53%**) are not weak complete, thus **are not r-universal**,

c) 7,732 (**2.13%**) are weak complete, but **it is not known whether they are r-universal** (circuits with qD-property built up of gates *G* have not been found)..

5. Conclusions

By exhaustive calculations we have established that over 97% of all ternary reversible 2*2 gates are r-universal. As there are so many universal gates the circuit designers have a lot of freedom in finding gates with good physical implementations (e.g. minimum cost). Some such multivalued gates have been proposed for quantum logic [38] and generalized in [41, 44, 30]. However, nobody has done such research for CMOS, DNA and nanotechnologies where a number of binary gates have been proposed.

Theorem 2 gives a sufficient condition for r-universality. However, we do not know whether it is also a necessary condition. It is an interesting open problem.

6. References

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