Current-Mode Amplifier/Integrator for a Field-Programmable Analog Array

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Outline

1. Introduction
2. The FPAA
3. Programmable Amplifier/Integrator
4. Conclusions

"Analog VLSI is strikingly superior to digital technology in terms of cost, power and computational density."

– BYTE Magazine, 1992

But ...

design of analog circuits is much more difficult and computer design aids for analog are far behind those for digital.

"It is not uncommon to design a digital VLSI containing more than 100,000 transistors in a few weeks.

"It is not unusual for an analog designer to spend several months on an analog cell with fewer than 30 transistors."

–L. Richard Carley, 1994
Carnegie Mellon University

FPGAs are revolutionizing **digital** design.

But they currently do not handle **continuous-time** (c-t) signals.

Attaining full programmability of c-t circuits requires:

- providing a flexible architecture (scheme of interconnections) between programmable circuit blocks (cells),
- designing a multi-function cell.

Long (global) signal connections could be used to attain flexible architectures.

But they introduce signal delays (excess phase) and increase undesired signal coupling (cross talk).

Switches could be used to attain programmability (EPAC, Electronically Programmable Analog Circuit, based on switched-capacitor (SC) technique).

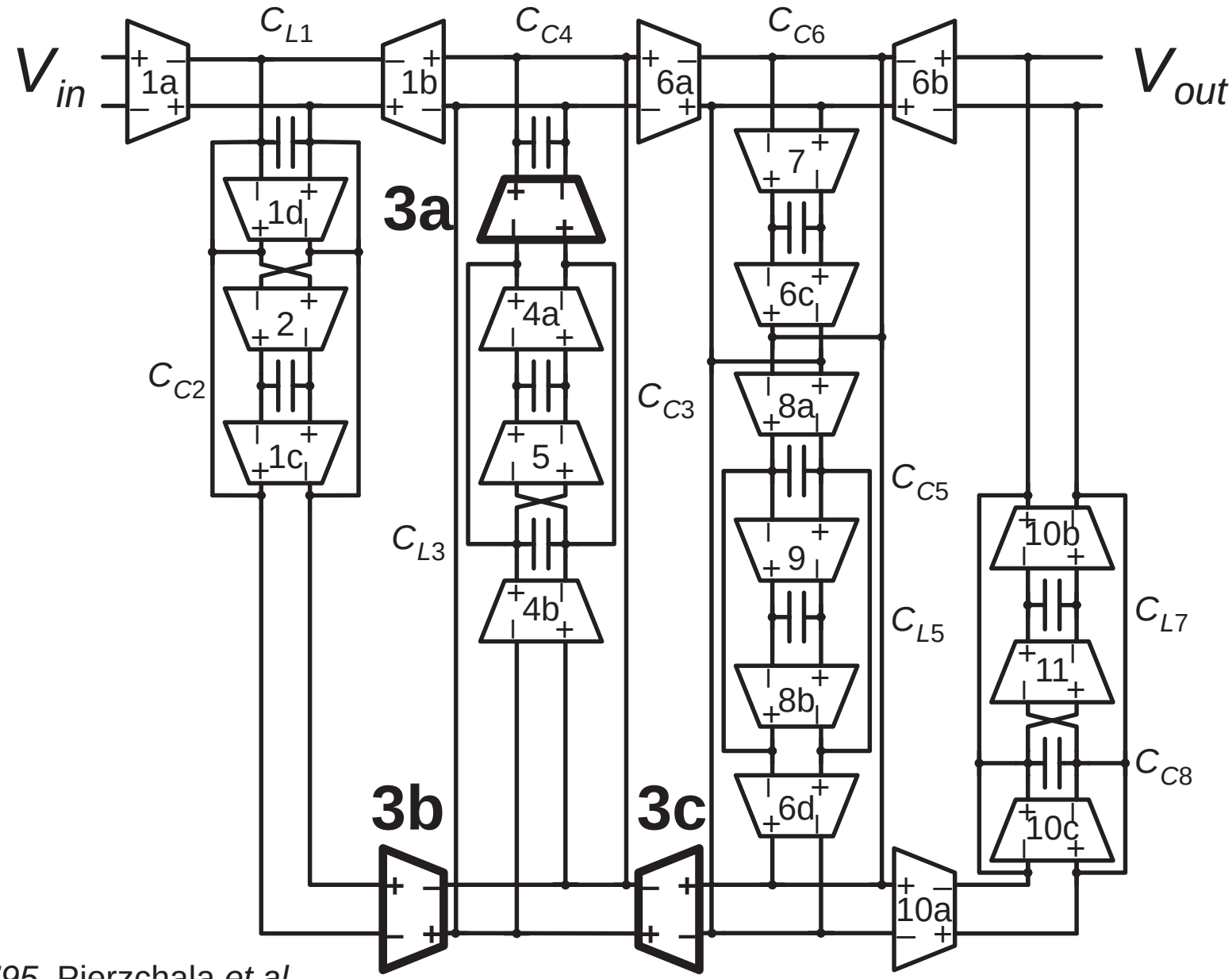
But switches have parasitics which limit the bandwidth of c-t circuits and introduce excess phase.

In HF c-t programmable circuits there is no place for long signal connections or switches in the signal path.

But then how to attain programmability?

No programmable circuit—digital or analog—should be expected to target all possible applications.

We have selected linear c-t filters to demonstrate our approach to FPAA design.


V_{in}
V_{out}
C_{L1}
C_{C4}
C_{C6}
1a
1b
6a
6b
1d
2
1c
4a
5
4b
7
6c
8a
9
8b
6d
10b
11
10c
10a
3a
3b
3c
C_{C2}
C_{L3}
C_{C3}
C_{C5}
C_{L5}
C_{L7}
C_{C8}

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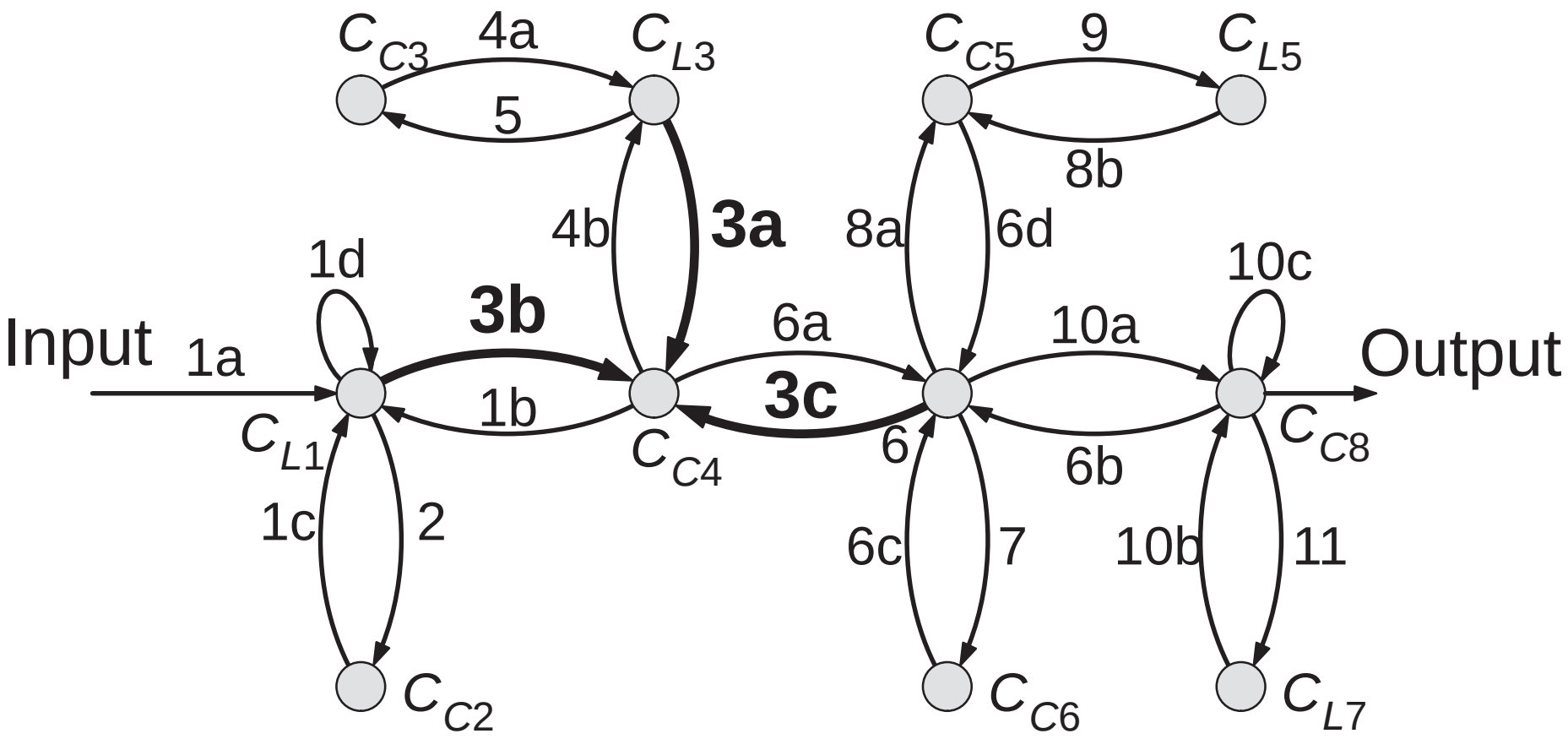
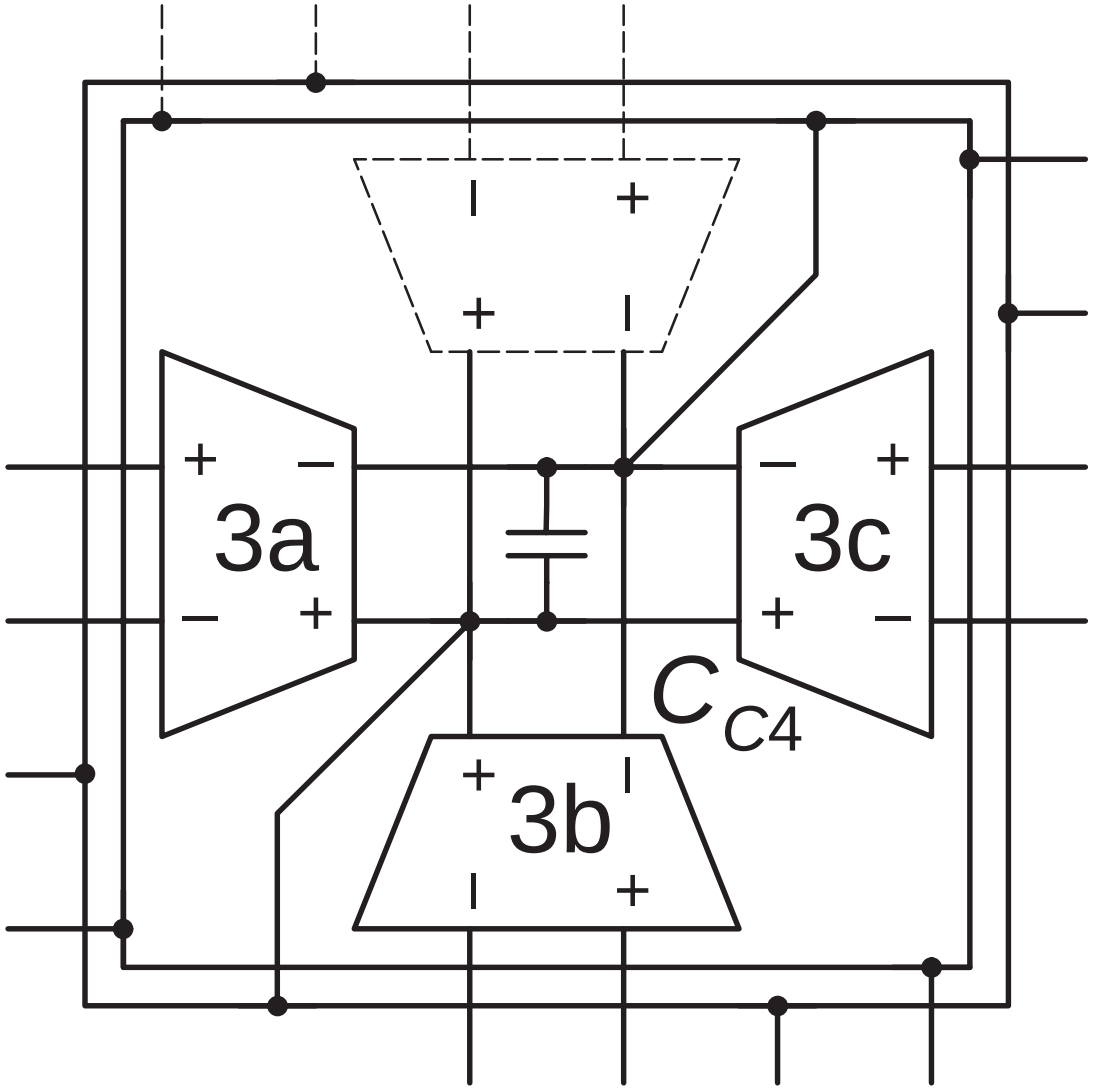
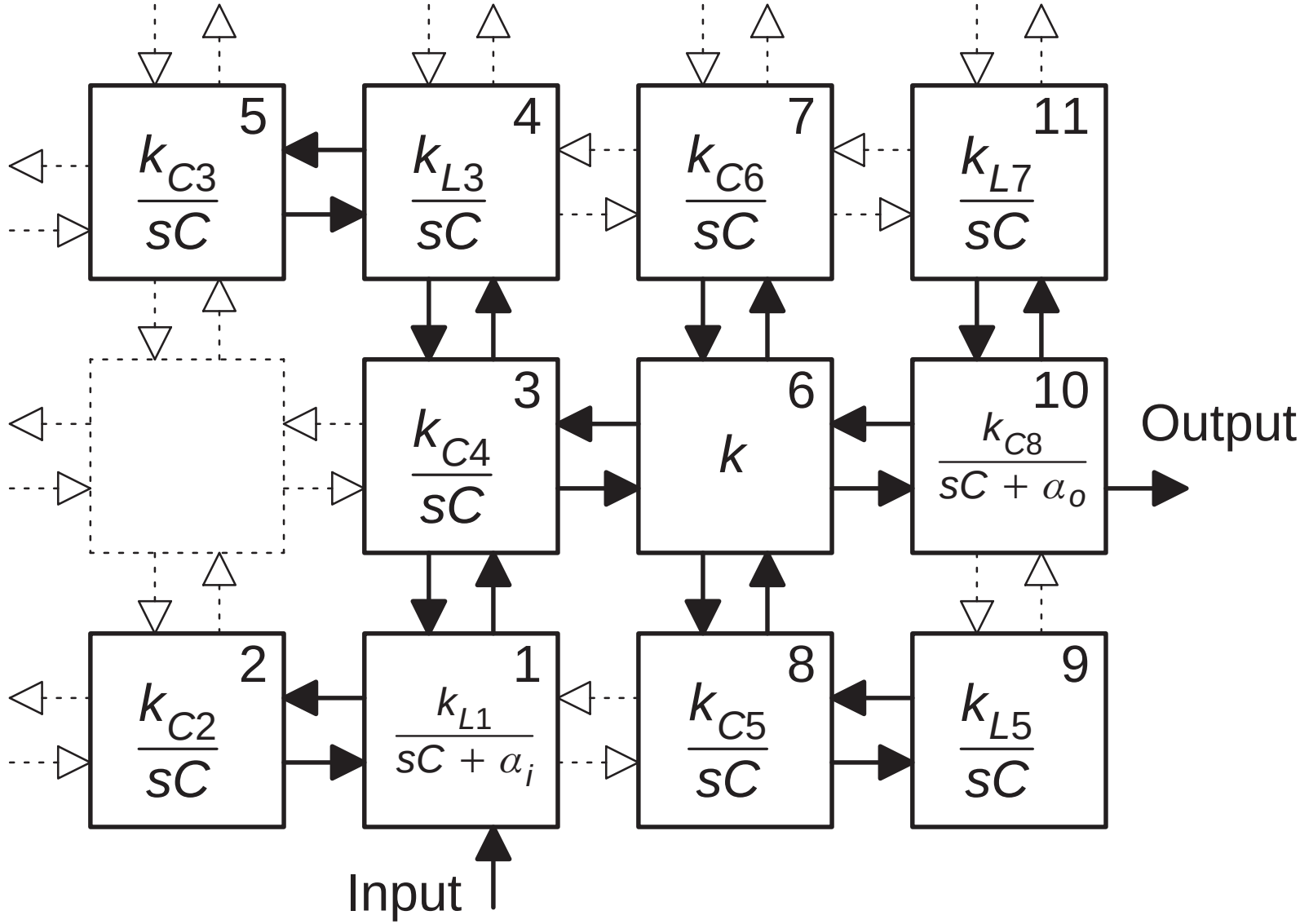
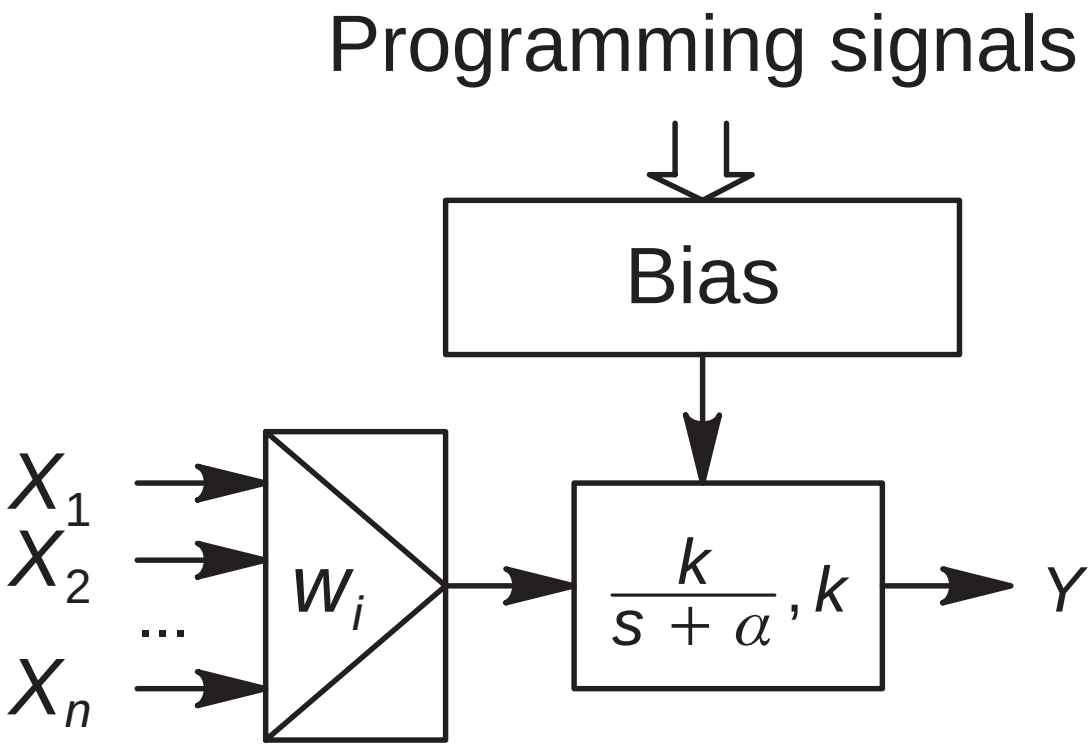
The architecture of the FPAA emerges from the observed regularity of the pattern of connections of ladder filters, a specific application.


C_{C3}
4a
C_{L3}
5
C_{C5}
9
C_{L5}
8b
4b
3a
8a
6d
1d
10c
3b
Input
1a
6a
10a
Output
1b
3c
C_{L1}
C_{C4}
6
6b
C_{C8}
1c
2
6c
7
10b
11
C_{C2}
C_{C6}
C_{L7}

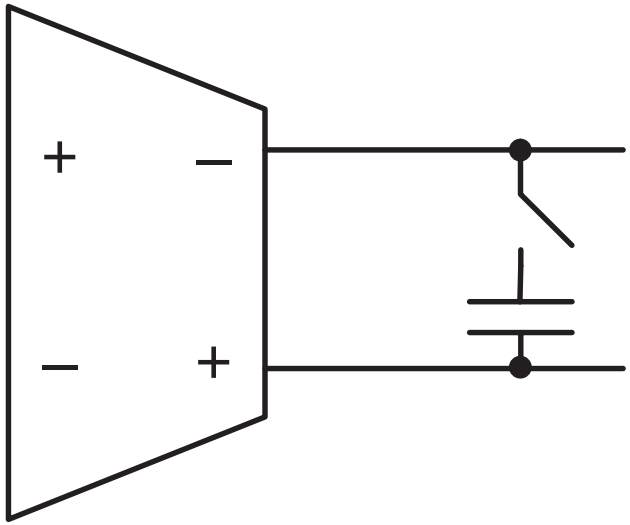

3a
3c
3b
C_{C4}


5
$\frac{k_{C3}}{sC}$
4
$\frac{k_{L3}}{sC}$
7
$\frac{k_{C6}}{sC}$
11
$\frac{k_{L7}}{sC}$
3
$\frac{k_{C4}}{sC}$
6
k
10
$\frac{k_{C8}}{sC + \alpha_o}$
Output
2
$\frac{k_{C2}}{sC}$
1
$\frac{k_{L1}}{sC + \alpha_i}$
8
$\frac{k_{C5}}{sC}$
9
$\frac{k_{L5}}{sC}$
Input

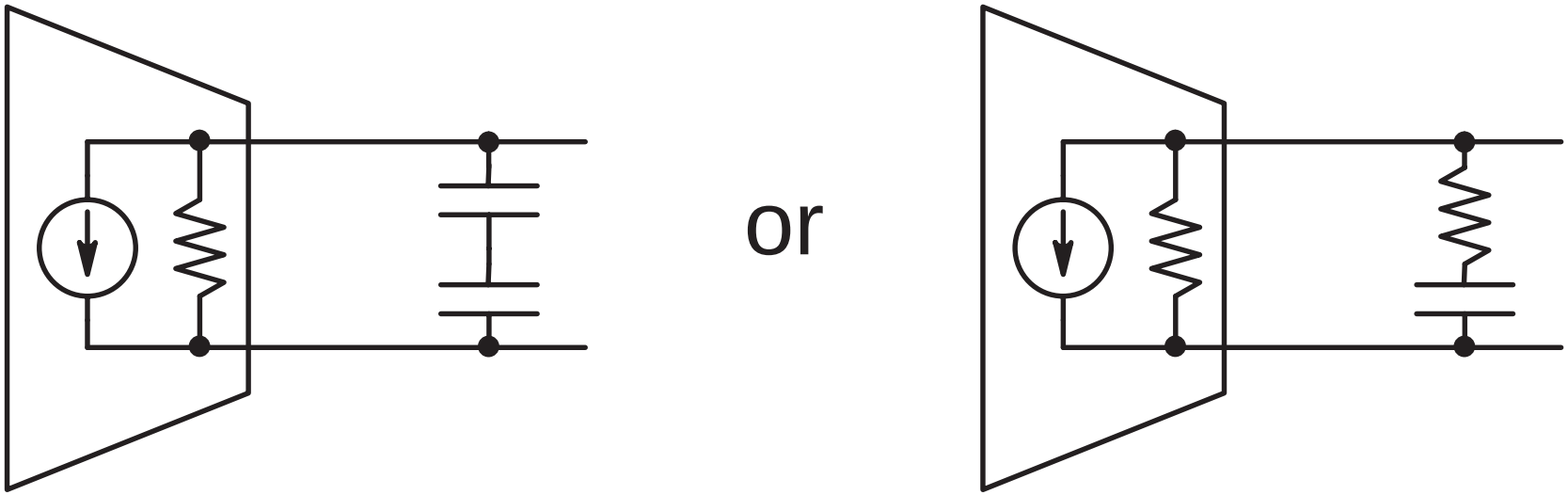
Functions of the cell:



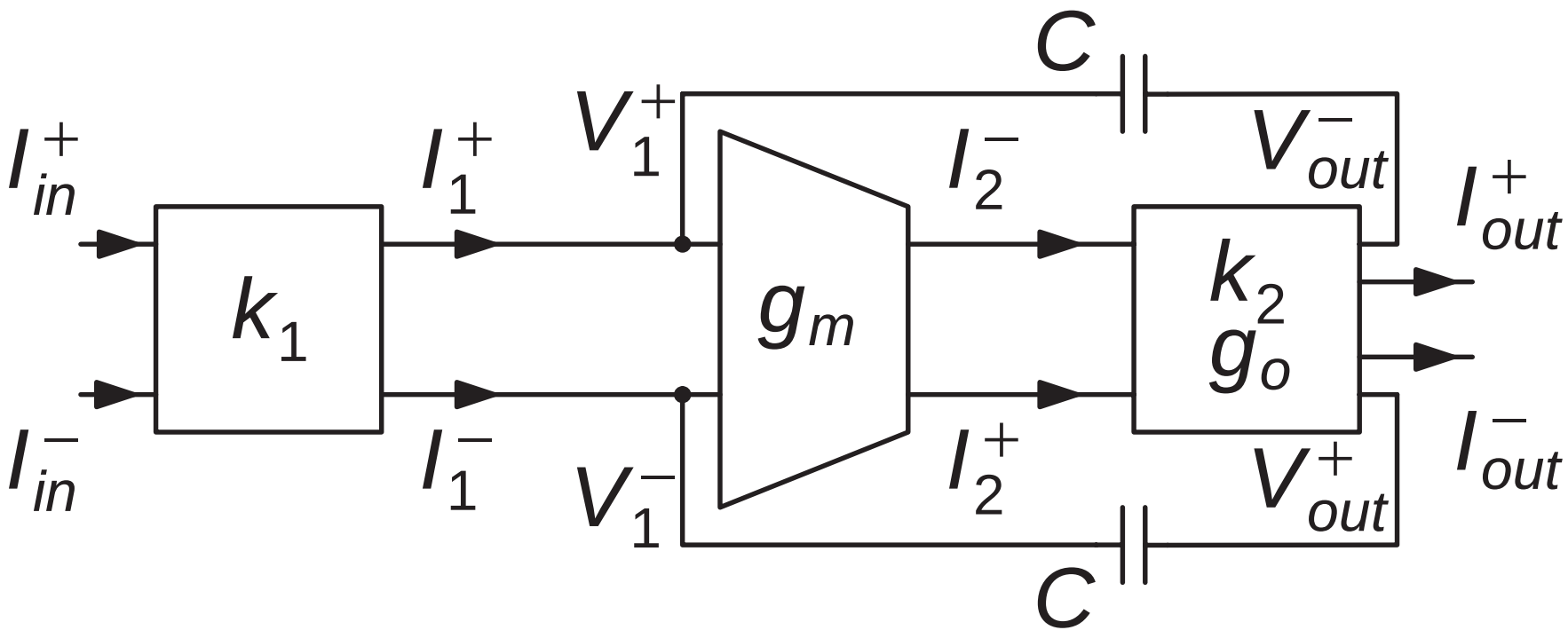
A straightforward implementation of the programmable integrator in OTA-C technique would lead to a switch in the signal path:



Which would lead to ...



Instead we propose a current-mode implementation of a Miller integrator.



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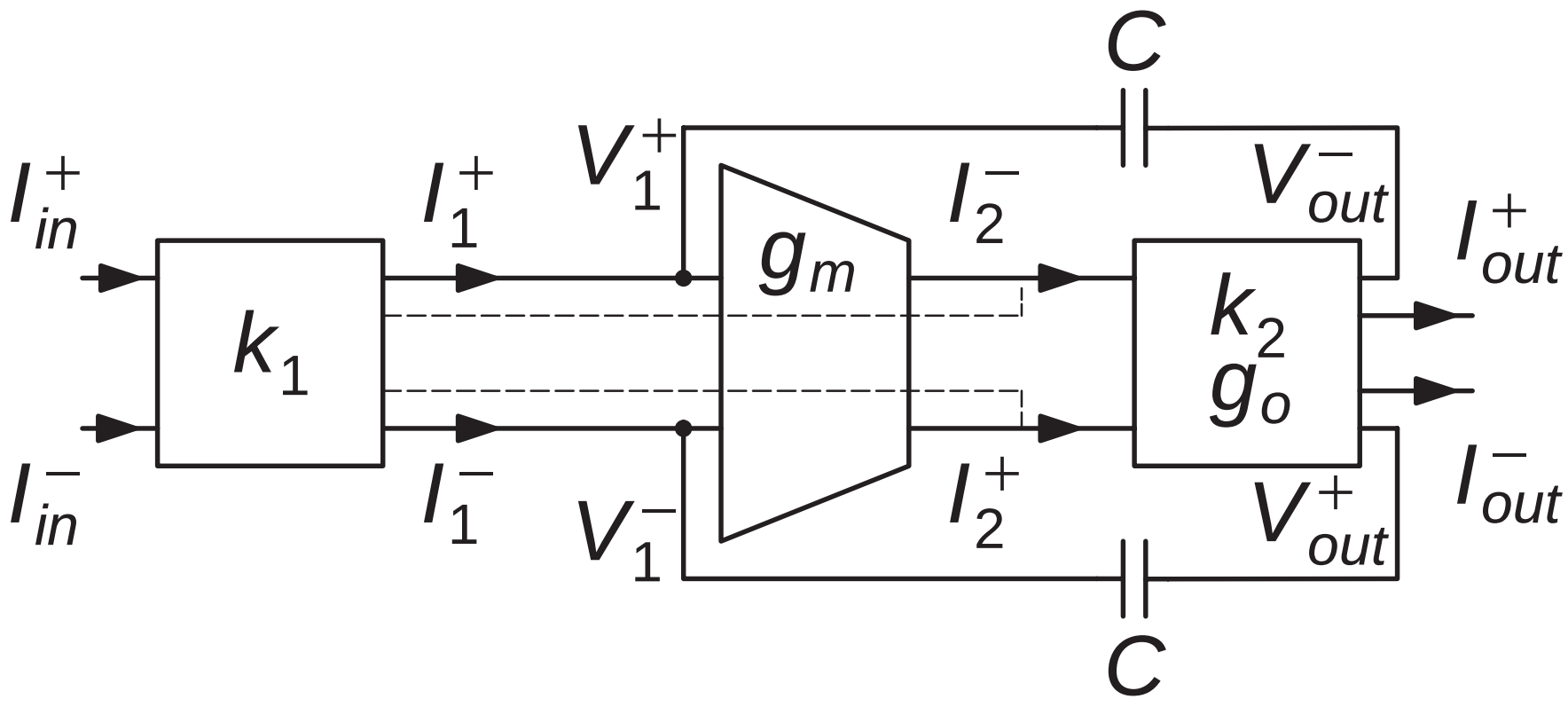
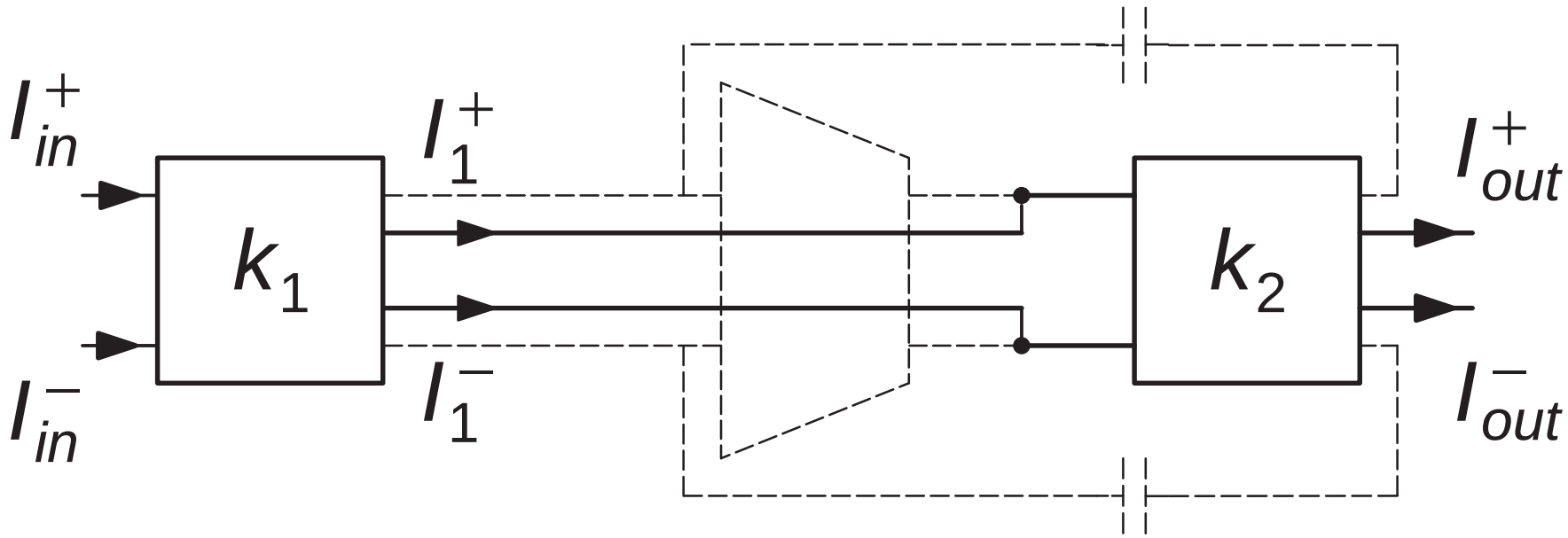
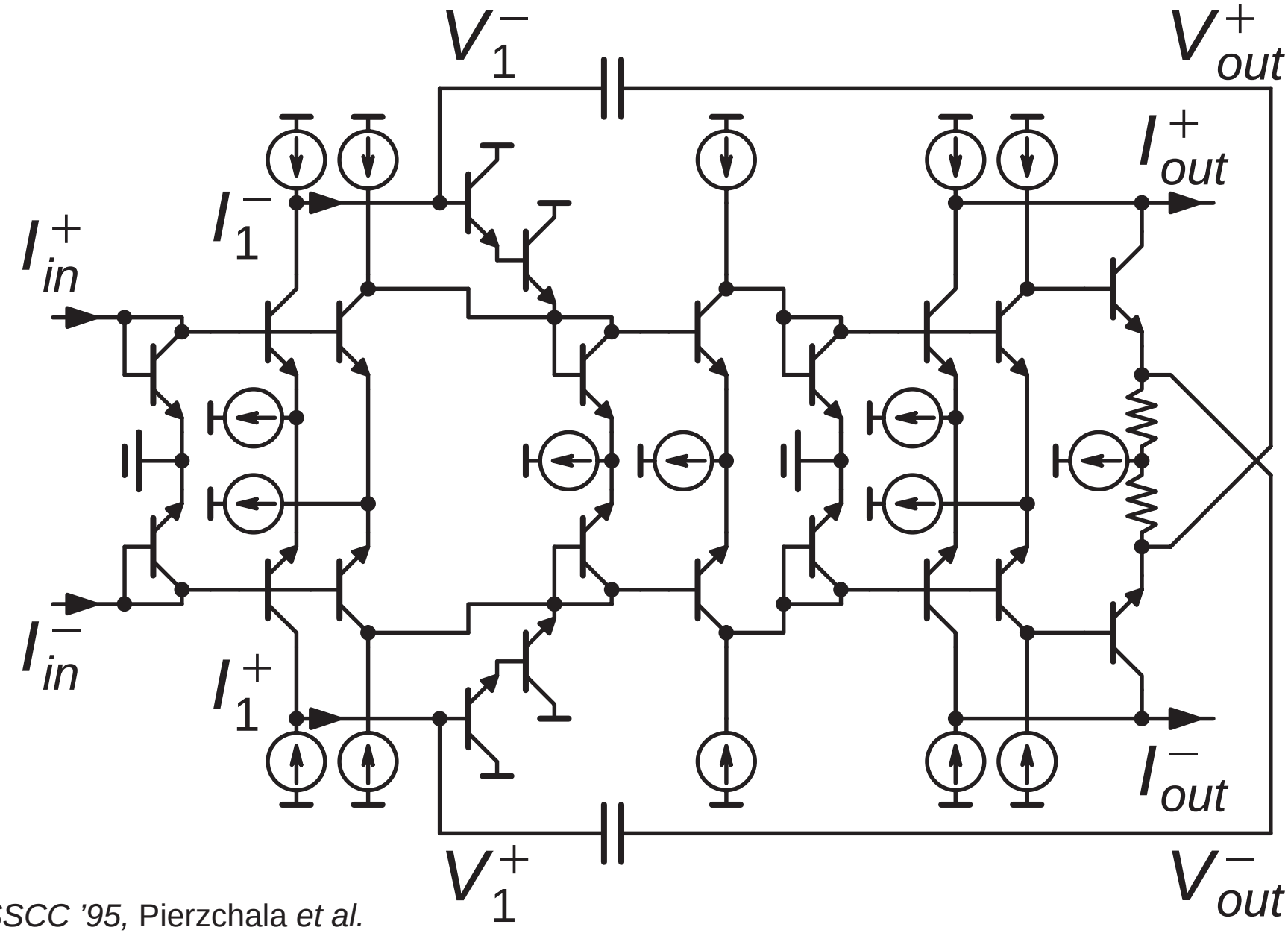

C
I_{in}^{+}
I_1^{+}
V_1^{+}
I_2^{-}
V_{out}^{-}
I_{out}^{+}
k_1
g_m
k_2
g_o
I_{in}^{-}
I_1^{-}
V_1^{-}
I_2^{+}
V_{out}^{+}
I_{out}^{-}
C


I_{in}^{+}
I_{in}^{-}
k_1
I_1^{+}
I_1^{-}
k_2
I_{out}^{+}
I_{out}^{-}



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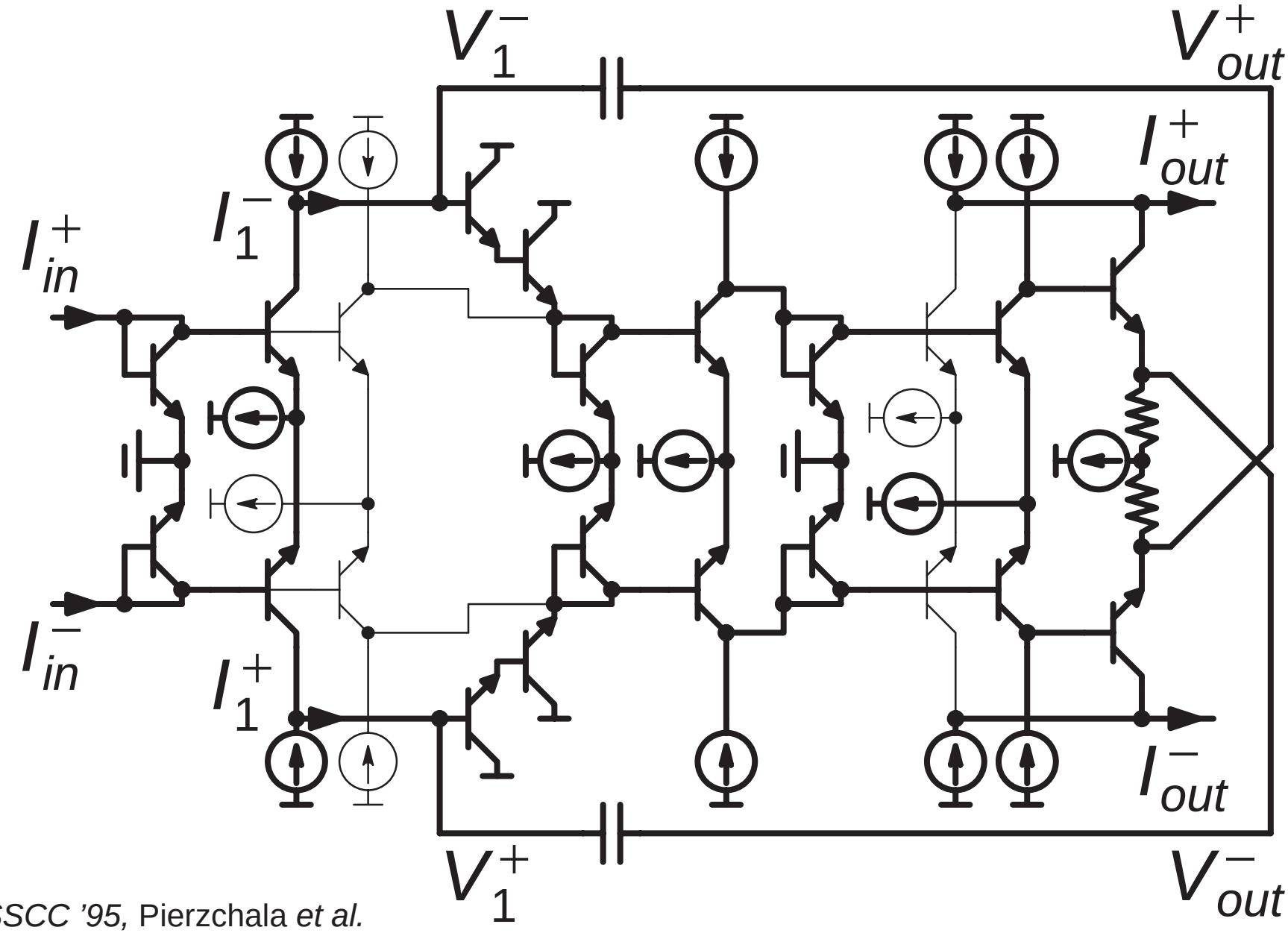

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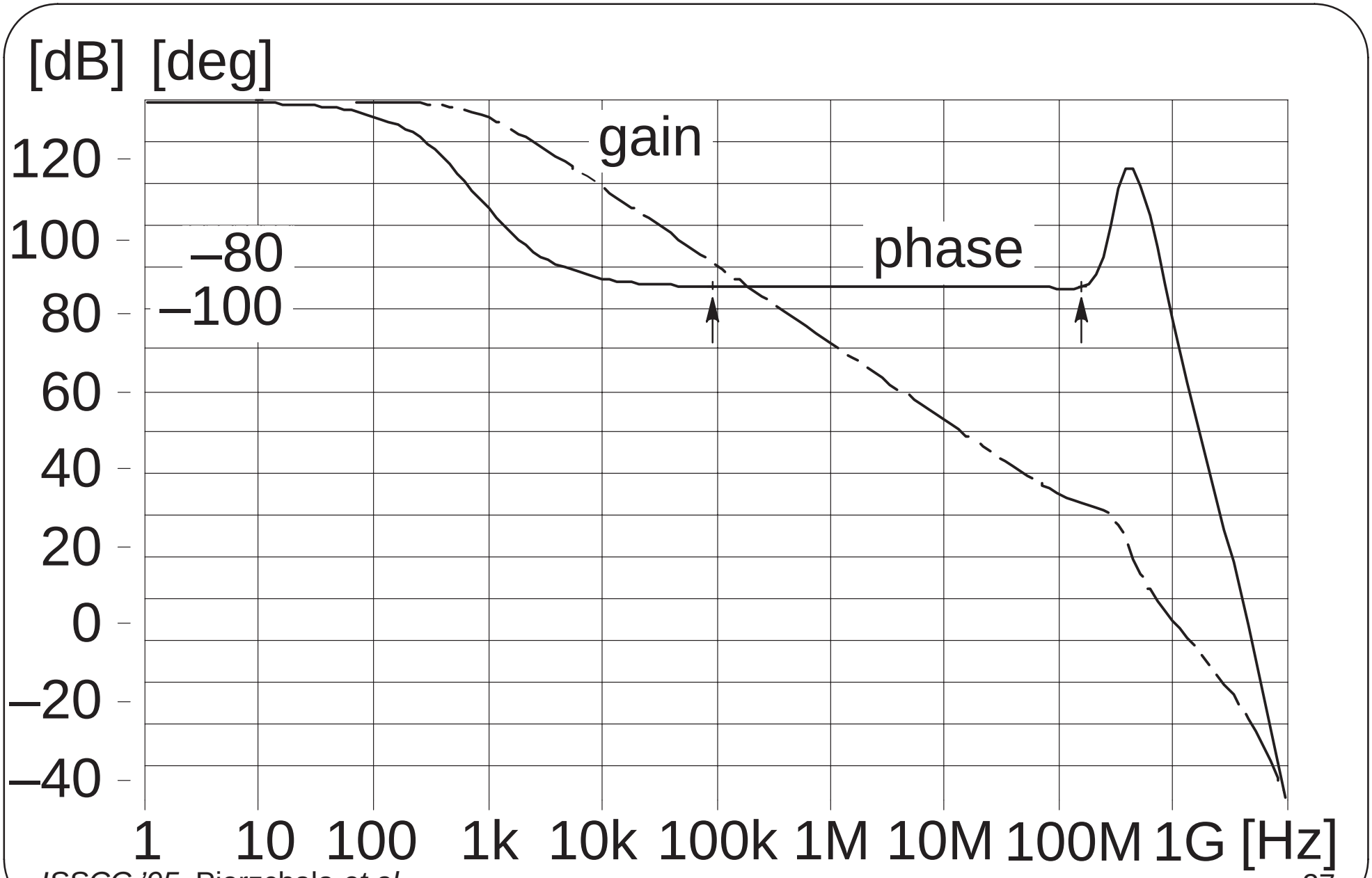
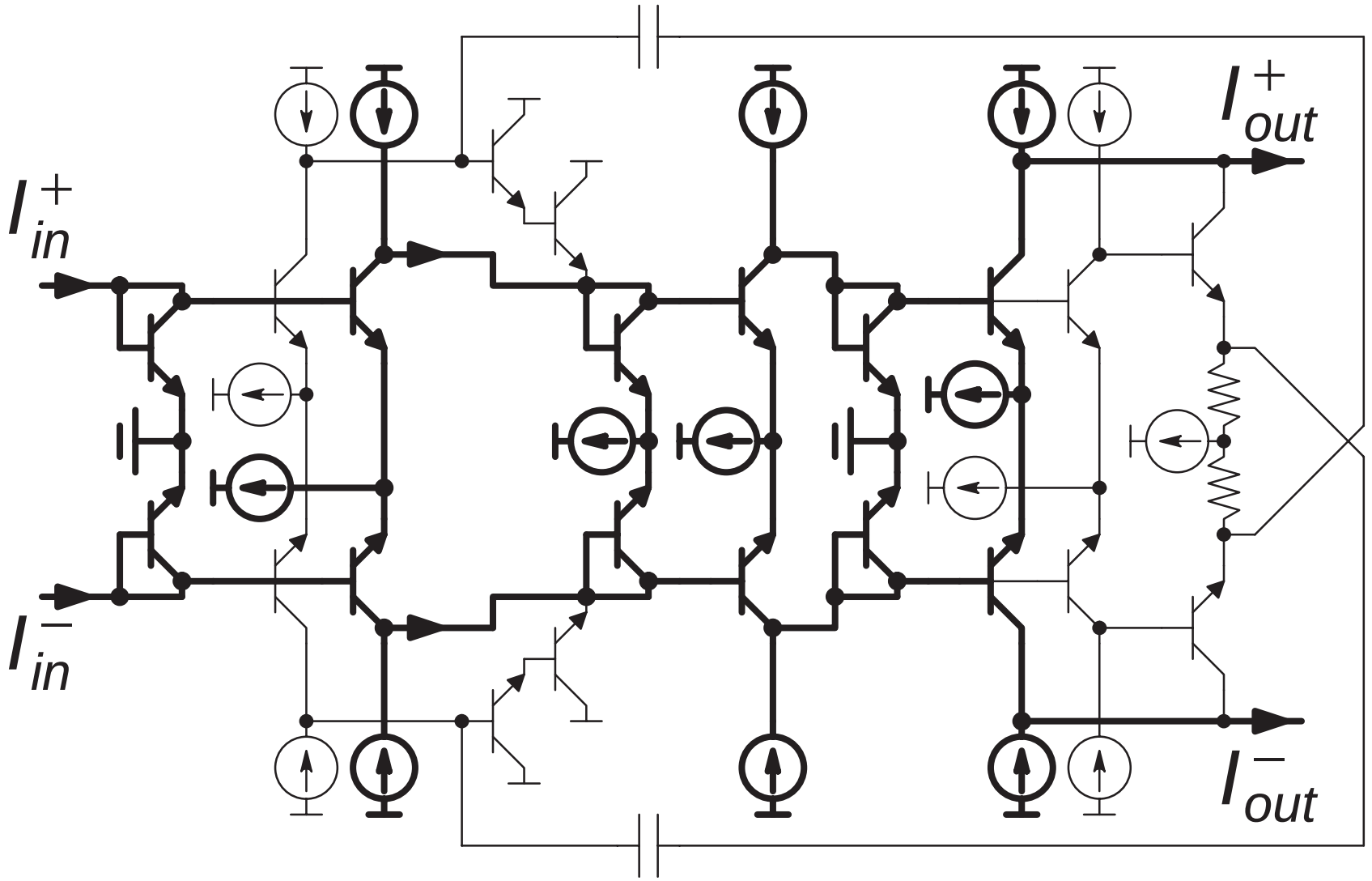

[dB]
[deg]
120
100
80
60
40
20
0
–20
–40
–80
–100
gain
phase
1
10
100
1k
10k
100k
1M
10M
100M
1G
[Hz]



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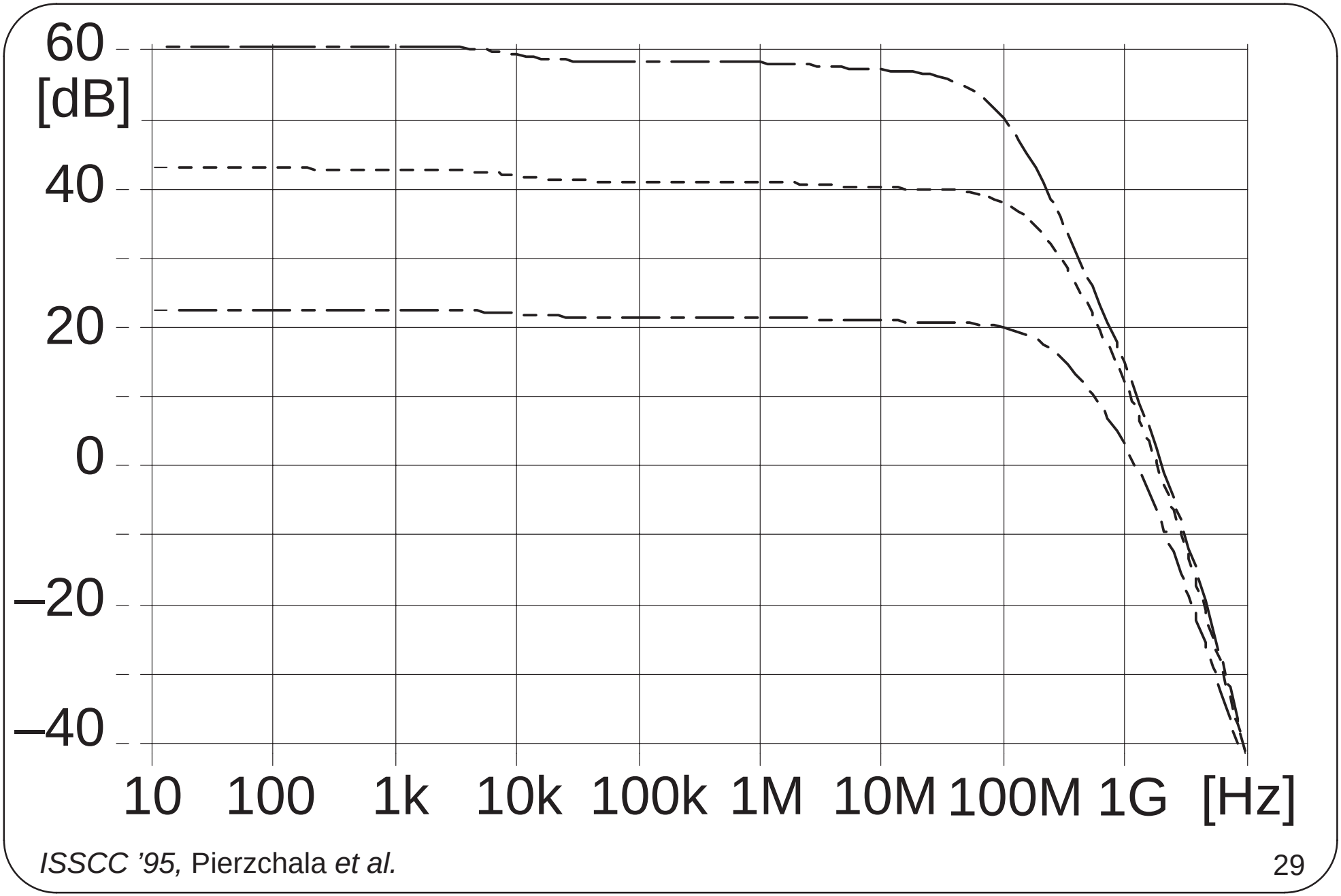

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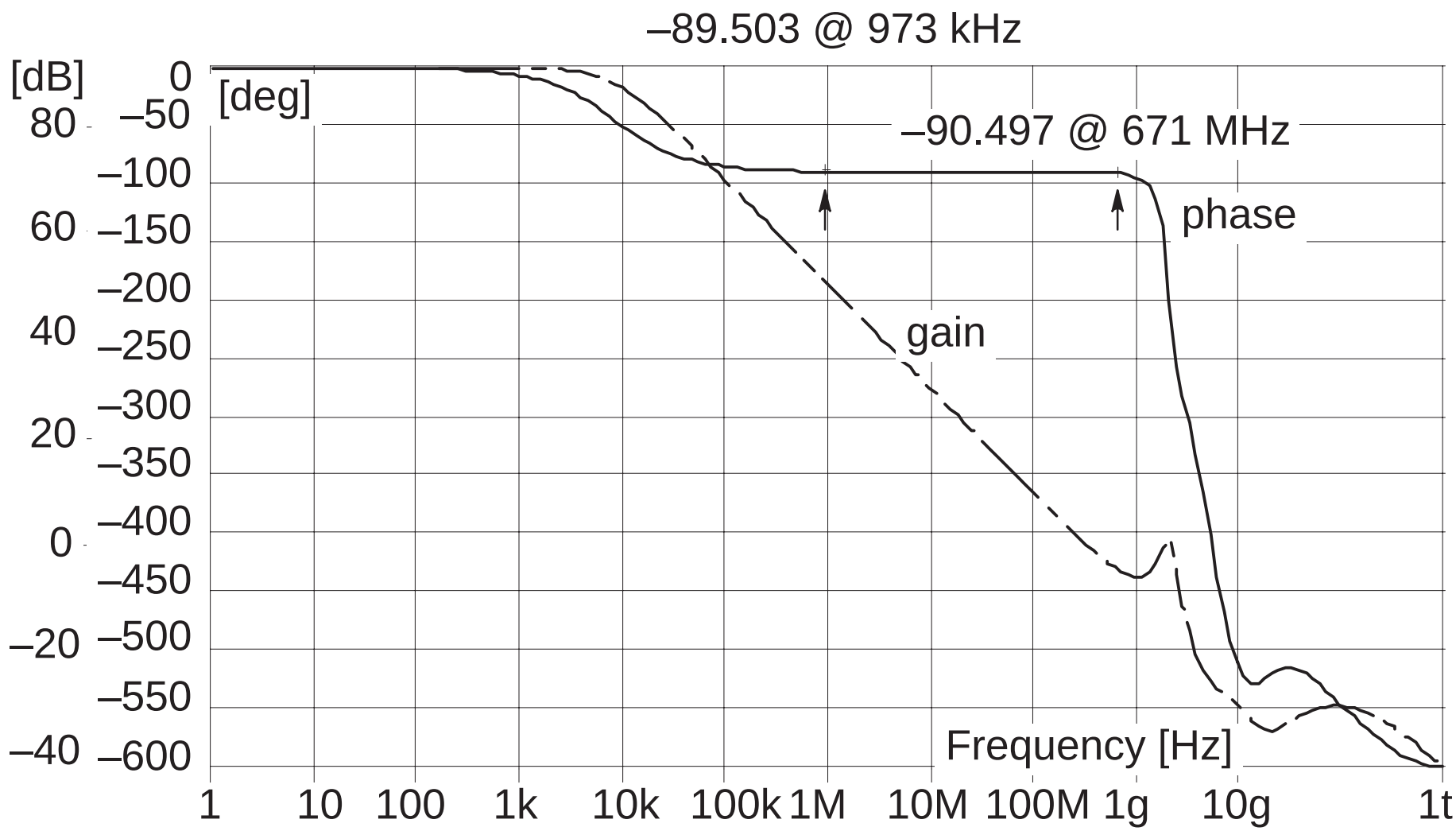
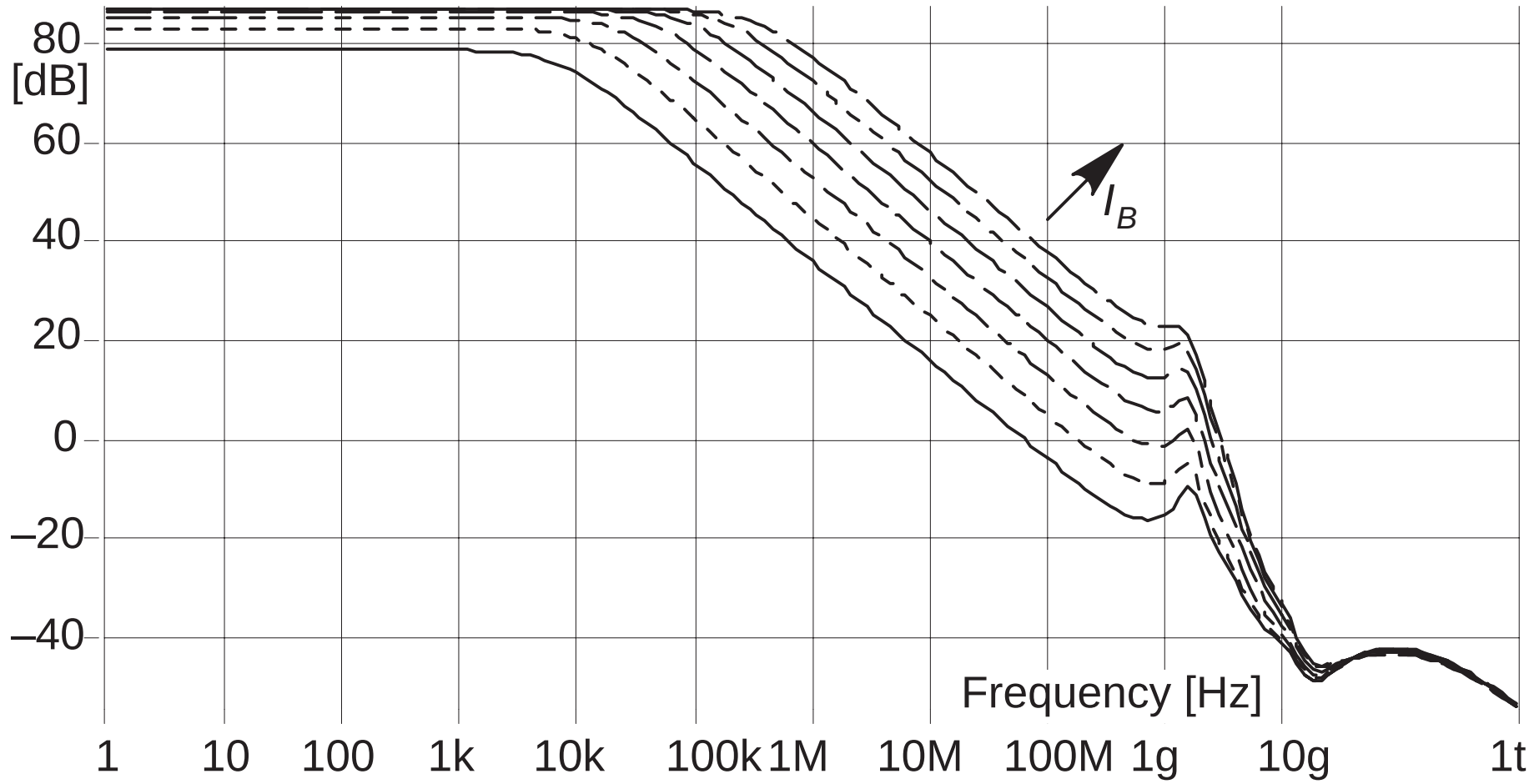

–89.503 @ 973 kHz
[dB]
[deg]
–90.497 @ 671 MHz
phase
gain
Frequency [Hz]
80
60
40
20
0
–20
–40
0
–50
–100
–150
–200
–250
–300
–350
–400
–450
–500
–550
–600
1
10
100
1k
10k
100k
1M
10M
100M
1g
10g
1t


80
[dB]
60
40
20
0
–20
–40
I_B
Frequency [Hz]
1
10
100
1k
10k
100k
1M
10M
100M
1g
10g
1t

Power supplies	± 3V	± 5V
Power consumption	< 12 mW	< 20 mW
Design Tool	ADS	
Technology	Tektronix/Maxim CPI transistor array, f_T = 8 GHz	
Programming method	by changing bias, with no switches in the signal path	

Integrator

Phase response

with tuning	90°±0.5° for 370 Hz to 160 MHz
without tuning	90°±0.5° for 92 kHz to 160 MHz

DC gain 130 dB

Amplifier

Max gain 60 dB

Unity gain bandwidth 855 MHz

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- Programmability (of both parameters and functions) of selected classes of analog circuits can be attained without substantially sacrificing the performance.
- Pre-designed array of cells makes the design of analog applications easier.
- Presented FPAA can be generalized for other classes of circuits.
- Speed-critical applications are a natural target of the emerging fast FPAA technology.