# Final Solutions <br> December 6 and 8, 1999 

## ECE 171: Introduction to Digital Design Dr. McNames

Write your 6-digit identification number and student identification numbers below. Do not begin the exam or look at the problems until instructed to do so. Once you begin, you have 100 minutes to complete the exam.

Once you begin, write your student ID at the top of each page. This is worth 5 points.

Do not use separate scratch paper. If you need more space, use the backs of the exam pages.

| , | 25 |
| :---: | :---: |
| Problem 2: | / 25 |
| Problem 3: | / 24 |
| Problem 4: | / 21 |
| Problem 5: |  |
| Student ID: |  |

Total: $\qquad$ /115

## 6-Digit Identification Number:

$\qquad$

## Student Identification Number:

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## 1. Latches \& Flip Flops (25 Points)

Fill in the timing diagrams and label the symbols for the following latches and flip flops. Assume that the propagation delay is 0 .
a. (6 pts) SR Latch

b. (6 pts) D Latch with enable

c. (13 pts) JK Flip Flop, falling edge triggered, asynchronous active-low preset and clear.


## 2. Five Variable Karnaugh Maps ( 25 points)


a. (5 pts) Circle all of the prime implicants for the 5-variable Karnaugh map above.
b. (4 pts) Put an asterisk (*) in the upper left corner of each distinguished 1 cell.
c. ( 6 pts ) Write the boolean expression for each prime implicant below.

|  | A' ${ }^{\prime} \mathrm{D}$ | $\mathrm{D}^{\prime} \mathrm{E}$ |
| :--- | :--- | ---: |
|  | $\mathrm{AB}^{\prime} \mathrm{C}^{\prime}$ |  |
| $\mathrm{C}^{\prime} \mathrm{E}$ | $\mathrm{A}^{\prime} \mathrm{BD}$ |  |
| $\mathrm{A}^{\prime} \mathrm{B}^{\prime} \mathrm{E}$ | $\mathrm{B}^{\prime} \mathrm{C}^{\prime} \mathrm{D}$ |  |
|  | $\mathrm{A}^{\prime} \mathrm{BC}^{\prime}$ |  |

d. ( 1 pt ) How many prime implicants are shared among both 4 -variable maps?

| (Circle one of the options) | 1 | 2 | 3 | 4 |
| :--- | :--- | :--- | :--- | :--- |

e. ( 3 pts ) Circle the boolean expression of each essential prime implicant in part c .
f. (5 pts) Write the expression for each minimal sum of products.

$$
Y=A^{\prime} B^{\prime} E+D^{\prime} E+A^{\prime} B D^{\prime}+A B^{\prime} C^{\prime}+A B E+A^{\prime} C^{\prime} D
$$

$Y=$ $\qquad$
$Y=$ $\qquad$
$Y=$ $\qquad$
g. (1 pt) How many minimal sums of products are there? Circle one of the options below.

1) 23
3. Logic Gates (24 Points)
a)

g)

1) 


b)

h)

m)

c)

i)

n)

d)

j)

o)

e)

k)

p)

f) $A \longrightarrow{ }^{21}=F$

| Boolean <br> Expression | Name of <br> Gate | Standard <br> Symbol | IEEE/ANSI <br> Symbol |
| :--- | :--- | :---: | :---: |
| $\mathrm{F}=\overline{\mathrm{A} \oplus \mathrm{B}}$ | XNOR | j | p |
| $\mathrm{F}=\overline{\mathrm{A}} \overline{\mathrm{B}}$ | NOR | m | k |
| $\mathrm{F}=\overline{\mathrm{A}}$ | Inverter | a | b |
| $\mathrm{F}=\overline{\overline{\mathrm{A}}+\overline{\mathrm{B}}}$ | AND | l | o |
| $\mathrm{F}=\overline{\mathrm{A}} \oplus \overline{\mathrm{B}}$ | XOR | h | b |
| $\mathrm{F}=\mathrm{A}+\mathrm{B}$ | OR | e | f |
| $\mathrm{F}=\overline{\mathrm{A}}+\overline{\mathrm{B}}$ | NAND | c | g |
| $\mathrm{F}=\mathrm{A}$ | Buffer | i | n |

## 4. MSI Devices \& Data Sheets ( 21 points)

Use the supplemental data sheet to answer the following questions about the SN7490A.
a. (1 pts) How many counters are in this device? (Circle one) $\quad \mathbf{1} \quad 2 \mathbf{2}$
b. ( 2 pts ) What is the count-length (number of distinct states) of each counter?

| (Circle all that apply) | $\mathbf{1}$ | 2 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 |
| :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- |
| 10 |  |  |  |  |  |  |  |  |  |  |

c. (2 pts) How many flip flops are in this device? (Circle one) $\mathbf{1}$ 1 $2 \mathbf{2}$ 8
d. (2 pts) What is the high noise margin? $\mathrm{NM}_{\mathrm{H}}=0.4 \mathrm{~V}$
e. (1 pt) How are the counter(s) triggered? (Circle one) Rising Edge Falling Edge
f. (1 pt) What is the maximum clock frequency that could be used to drive any of the counters in this device? $\mathrm{f}_{\text {max }}=16 \mathrm{MHz}$
g. (2 pts) What would the outputs be if the inputs $\mathrm{R} 0(1), \mathrm{R} 0(2), \mathrm{R} 9(1)$, and $\mathrm{R} 9(2)$ where all set high (logic value of 1 )? $\mathrm{QD}=\mathrm{H} \quad \mathrm{QC}=\mathrm{L} \quad \mathrm{QB}=\mathrm{L} \quad \mathrm{QA}=\mathrm{H}$
h. ( 5 pts ) Show how the counter could be connected to output a square-wave that is 10 times longer than the clock input. Show how the pins must be connected including the clock input (CLK), power (Vcc), ground (GND), and the output (Y). Some pins may be left unconnected.

i. (5 pts) Show how the counter could be connected to output a binary count sequence with a count length of 10 . Show how the pins must be connected including the clock input (CLK), power (Vcc), ground (GND), and the outputs (Q3, Q2, Q1, and Q0) where Q3 is the most significant bit (MSB). Some pins may be left unconnected.


## 5. Subtractors ( 15 points)

A vending machine manufacturer is in need of a 4-bit subtractor. Work through the following problems to design this device.
a. (2 pts) For the 2-input subtractor shown below, fill in the truth table. Y is the result of the subtraction (C-D) and Bo indicates whether the subtractor needs to borrow a one from the more significant bit.

| C | $\mathbf{D}$ | $\mathbf{Y}$ | Bo |
| :--- | :--- | :--- | :--- |
| 0 | 0 | 0 | 0 |
| 0 | 1 | 1 | 1 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 0 |


b. (2 pts) Using as few gates as possible, draw the logic diagram using traditional symbols for the subtractor outputs Y and Bo.

c. (2 pts) For the 3-input subtractor shown below, fill in the truth table. Bi indicates whether the less significant bit needs to borrow a one. Y and Bo are defined the same as in part a.

| $\mathbf{C}$ | $\mathbf{D}$ |  | $\mathbf{B i}$ | $\mathbf{Y}$ |  | $\mathbf{B o}$ |
| :--- | :--- | :--- | :--- | :--- | :---: | :---: |
| 0 | 0 | 0 | 0 | 0 |  |  |
| 0 | 0 | 1 | 1 | 1 |  |  |
| 0 | 1 | 0 | 1 | 1 |  |  |
| 0 | 1 | 1 | 0 | 1 |  |  |
| 1 | 0 | 0 | 1 | 0 |  |  |
| 1 | 0 | 1 | 0 | 0 |  |  |
| 1 | 1 | 0 | 0 | 0 |  |  |
| 1 | 1 | 1 | 1 | 1 |  |  |



## 5. Subtractors Continued

d. (6 pts) Using as few gates as possible, draw the logic diagram using traditional symbols for the outputs Y and Bo of the subtractor in part c ..


e. (3 pts) Using the symbols in parts a. and c. draw a logic diagram for a 4-bit subtractor. Label the inputs C3,C2,C1,C0 and D3,D2,D1,D0 where C3 and D3 are the most significant bits. Label the outputs Bo and Y3,Y2, Y1, Y0 where Y3 is the most significant bit.


