Exam 1 Solutions

October 20, 1999

ECE 171: Introduction to Digital Design

Dr. McNames
Fall 1999

Write your 6-digit identification number below. Do not begin the exam or look at the problems until instructed to do so.

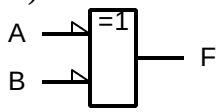
Do not use separate scratch paper. If you need more space write on the backs of the exam pages as necessary.

6-Digit Identification Number:_____

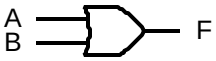
Student Identification Number:_____

1. Logic Symbols

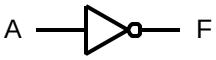
Match the traditional and IEEE/ANSI standard symbols to the expressions below. (24 pts)

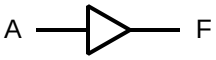
a) 

g) 

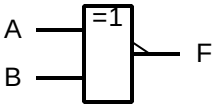
l) 

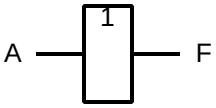
b) 

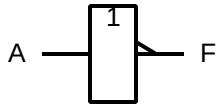
h) 

m) 

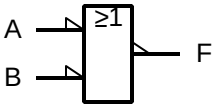
c) 

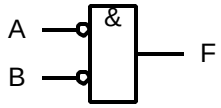
i) 

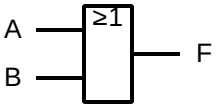
n) 

d) 

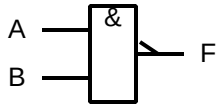
j) 

o) 

e) 

k) 

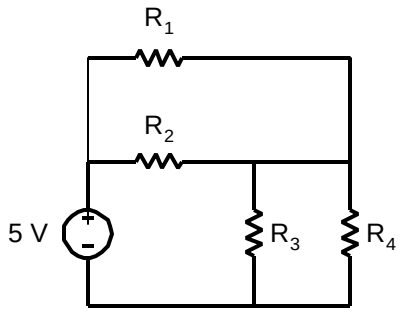
p) 

f) 

Boolean Expression	Name of Gate	Standard Symbol	IEEE/ANSI Symbol
$F = A \oplus B$	XOR	p	a
$F = \overline{A}\,\overline{B}$	NOR	c	e
$F = A$	Buffer	m	n
$F = A\,B$	AND	j	o
$F = \overline{\overline{A} \oplus \overline{B}}$	XNOR	g	i
$F = A + B$	OR	l	k
$F = \overline{A\,B}$	NAND	b	f
$F = \overline{A}$	Inverter	h	d

2. Resistor Circuits

Fill in the missing values for the circuit shown below. (10 pts)

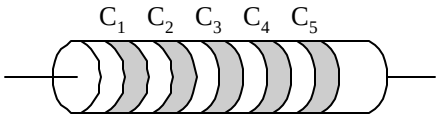


Element	Resistance	Voltage	Current	Power
Power Supply	N. A.	5 V	*0.5 mA*	*2.5 mW*
R_1	16.8 kO	*4.2 V*	*0.25 mA*	*1.05 mW*
R_2	16.8 kO	*4.2 V*	*0.25 mA*	*1.05 mW*
R_3	8 kO	*0.8 V*	*0.1 mA*	*0.08 mW*
R_4	2 kO	*0.8 V*	*0.4 mA*	*0.32 mW*

What is the equivalent resistance connected to the power supply (2 pts)?

R_{eq} = *10 kO*

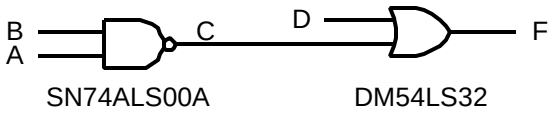
For the resistor shown below with the five color codes, fill in the missing elements of the table (8 pts).



Resistor Band Colors						
C_1	C_2	C_3	C_4	C_5	Resistance	Tolerance
Yellow	Violet	Green	Gold	None	*4.7 MO*	*5%*
Blue	Gray	Red	Silver	None	*68 kO*	*10%*
Gray	Red	Yellow	None	None	*820 kO*	*20%*
Orange	Orange	Orange	Orange	Red	*333 kO*	*2%*
Brown	Black	Brown	Gold	None	*100 O*	*5%*
Red	*Red*	*Orange*	*Gold*	*None*	22 kO	5%
Brown	*Black*	*Yellow*	*Silver*	*None*	100 kO	10%
Brown	*Orange*	*Black*	*Yellow*	*Red*	1.3 MO	2%

3. Data Sheets

The following devices have a voltage supply of 5V and operate at an ambient temperature of 25°C.



a) What is the high noise margin (2 pts)? NM_H = *1V = 3 - 2*

b) What is the low noise margin (2 pts)? NM_L = *0.2 V = 0.7 - 0.5*

c) Are these two devices compatible (1 pt) ? (Please circle one) [Yes] No

Even if the devices are incompatible, answer the following questions as though they were compatible.

d) What is the fanout for a high output state (2 pts)?
FO_H = *20 = |-0.4 mA / 20 µA|*

e) What is the fanout for a low output state (2 pts)?
FO_L = *22 = | 8 mA / -0.36 mA|*

f) How many DM54LS32 OR gates could be connected to the output one SN74ALS00A NAND gate (1 pt)?
Ans = *20*

g) What does the B input of the NAND gate need to be to make C equal to the complement of A (1 pt)?
(Please circle one) [High] Low

h) What does the D input of the OR gate need to be to make F = C (1 pt)?
(Please circle one) High [Low]

i) What is the propagation delay t_{PLH} from A to F (2 pts)?
t_{PLH} = *26 ns = 11 ns + 15 ns*

j) What is the propagation delay t_{PHL} from A to F (2 pts)?
t_{PHL} = *23 ns = 8 ns + 15 ns*

4. Window Alarm Design - Anti-Tagger Device

Goal: Leslie wishes to design an alarm system that prevents vandals from scratching their initials into the windows of small businesses. However, the system must be smart enough that it does not sound the alarm when the windows are touched during business hours or being washed.

Sensors: For this system Leslie has designed a scrape sensor that produces a +5V signal when the window is being scraped and 0V otherwise. Use the letter **S** to represent the output of this sensor.

Leslie has also created a sensor out of a programmable clock that produces a +5V signal during business hours and 0 V otherwise. Use the letter **B** to represent the output of this sensor.

To enable the windows to be washed during non-business hours Leslie has also obtained an electronic lock. When the lock is on, it produces a +5V signal and Leslie wants the alarm system to be enabled. When the lock is off, it produces a 0 V signal and the system should be disabled. Use the letter **L** to represent the state of the lock.

Alarm: To sound the alarm, the system must produce a +5V signal. Otherwise the alarm is off. Use **A** to represent the output of the logic to the alarm.

Leslie has asked you to design the logic for this system.

a) Fill in the truth table for this system. Use zeros to represent low voltages (0 V) and ones to represent high voltages (5 V). (4 pts)

S	**B**	**L**	**A**
0	0	0	*0*
0	0	1	*0*
0	1	0	*0*
0	1	1	*0*
1	0	0	*0*
1	0	1	*1*
1	1	0	*0*
1	1	1	*0*

4. Continued from previous page.

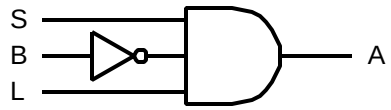
b) Write a smaller truth table using the don't care symbol, X. Use as few rows as possible (4 pts) .

S	B	L	A
0	*X*	*X*	*0*
X	*1*	*X*	*0*
X	*X*	*0*	*0*
1	*0*	*1*	*1*

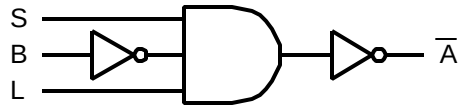
c) Write a boolean equation for this truth table. Simplify the expression as much as possible (2 pts).

$A = S\,\overline{B}\,L$

d) Draw a logic diagram for this circuit using the eight logic gates discussed in class. Use as few gates as possible (3 pts).

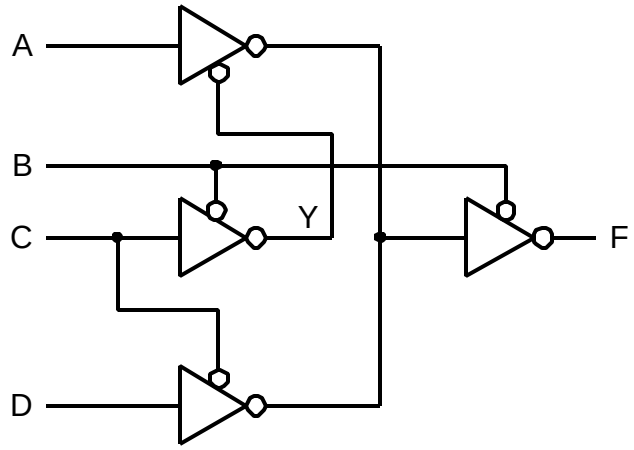


e) After you designed the system Leslie notifies you that the specifications on the alarm were incorrect. The logic that you designed needs to produce a 0V signal to sound the alarm. Modify the circuit designed in part d) by adding or removing <u>a single gate</u> so that it will produce a 0V signal when the alarm should be activated. Draw the new logic diagram in the space below (2 pts).



5. Tristate Buffers

Answer the following questions for the circuit shown below.



a) Fill in the truth table for this system. Use the high-impedance symbol Z as appropriate (8 pts).

A	B	C	D	Y	F
0	0	0	0	*1*	*0*
0	0	0	1	*1*	*1*
0	0	1	0	*0*	*0*
0	0	1	1	*0*	*0*
0	1	0	0	*Z*	*Z*
0	1	0	1	*Z*	*Z*
0	1	1	0	*Z*	*Z*
0	1	1	1	*Z*	*Z*
1	0	0	0	*1*	*0*
1	0	0	1	*1*	*1*
1	0	1	0	*0*	*1*
1	0	1	1	*0*	*1*
1	1	0	0	*Z*	*Z*
1	1	0	1	*Z*	*Z*
1	1	1	0	*Z*	*Z*
1	1	1	1	*Z*	*Z*

5. Continued from previous page.

b) Write a smaller truth table using the don't care symbol, X. Use as few rows as possible. Use the high-impedance symbol Z as appropriate (5 pts).

A	B	C	D	Y	F
X	*1*	*X*	*X*	*Z*	*Z*
0	*0*	*1*	*Z*	*0*	*0*
1	*0*	*1*	*X*	*0*	*0*
X	*0*	*0*	*0*	*1*	*0*
X	*0*	*0*	*1*	*1*	*1*

c) What does the B input have to be to guarantee the F output is never high impedance (1 pt)? (Please circle one) [0] 1

d) With B fixed at the value specified in part c, fill in the following truth table. Use the don't care symbol X to minimize the number of rows (2 pts).

A	C	D	Y	F
0	*1*	*X*	*0*	*0*
1	*1*	*X*	*0*	*1*
X	*0*	*0*	*1*	*0*
X	*0*	*1*	*1*	*1*

e) Write a boolean expression for F with B fixed at the value specified in part c. Simplify the expression as much as possible (2 pts)

F = $A\,C + \overline{C}\,D$

f) Draw an equivalent logic diagram using only OR gates, AND gates, and inverters for B fixed at the value specified in part c. Use as few gates as possible (2 pts)