ECE 416/516
IC Technologies
Lecture 1: Introduction

Professor James E. Morris
Spring 2012

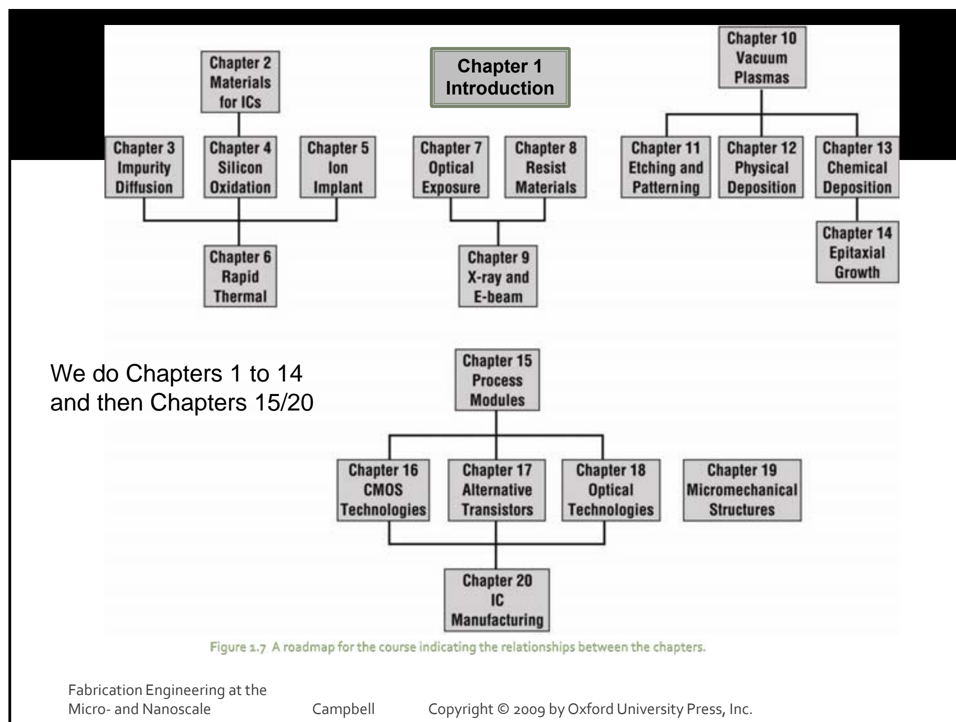

Figure 1.7 A roadmap for the course indicating the relationships between the chapters.

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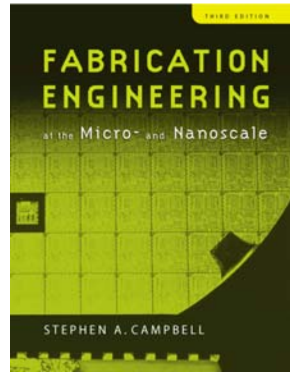
Chapter 1

An Introduction to Microelectronic Fabrication



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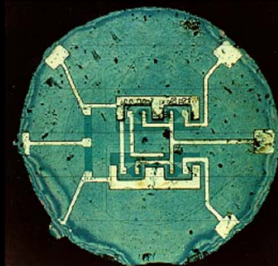
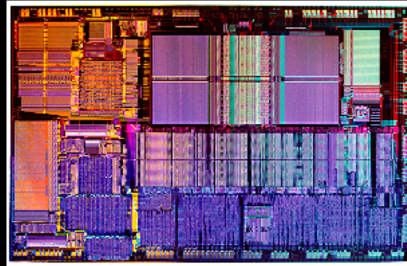
INTRODUCTION

This course is basically about silicon chip fabrication, the technologies used to manufacture ICs.





- **1960 and 1990 integrated circuits.**
- **Progress due to: Feature size reduction - 0.7X/3 years (Moore's Law).**
  Increasing chip size - ≈ 16% per year.
  "Creativity" in implementing functions.

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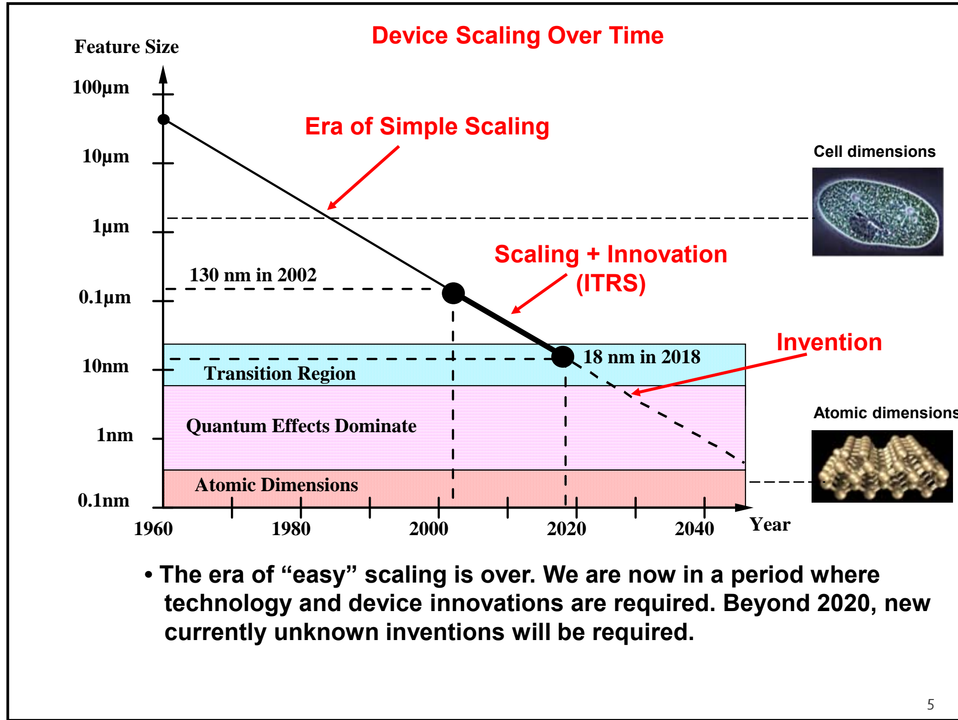

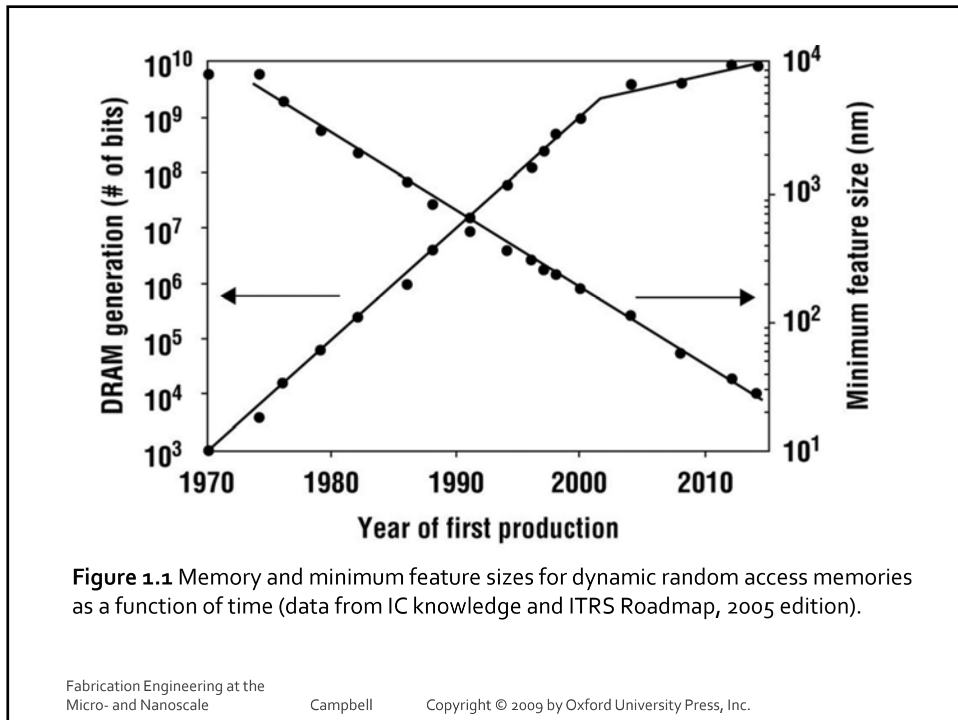

Figure 1.1 Memory and minimum feature sizes for dynamic random access memories as a function of time (data from IC knowledge and ITRS Roadmap, 2005 edition).

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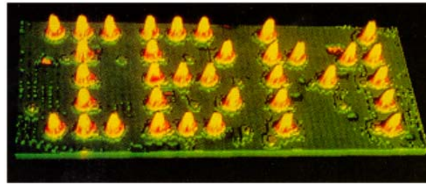
Year of Production	1998	2000	2002	2004	2007	2010	2013	2016	2018
Technology Node (half pitch)	250 nm	180 nm	130 nm	90 nm	65 nm	45 nm	32 nm	22 nm	18 nm
MPU Printed Gate Length		100 nm	70 nm	53 nm	35 nm	25 nm	18 nm	13 nm	10 nm
DRAM Bits/Chip (Sampling)	256M	512M	1G	4G	16G	32G	64G	128G	128G
MPU Transistors/Chip ($x10^6$)				550	1100	2200	4400	8800	14,000
Min Supply Voltage (volts)	1.8-2.5	1.5-1.8	1.2-1.5	0.9-1.2	0.8-1.1	0.7-1-0	06-0.9	0.5-0.8	0.5-0.7

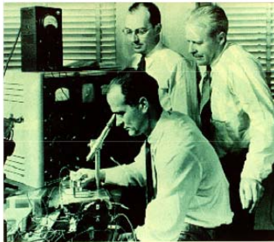
ITRS at http://public.itrs.net/ (2003 version + 2004 update).

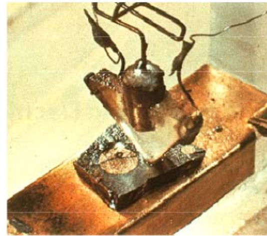
- Assumes CMOS technology dominates over entire roadmap.
- 2 year cycle moving to 3 years (scaling + innovation now required).



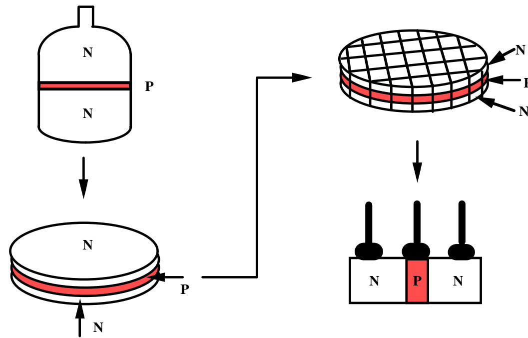
- 1990 IBM demo of Å scale "lithography".
- Technology appears to be capable of making structures much smaller than currently known device limits.

Historical Perspective

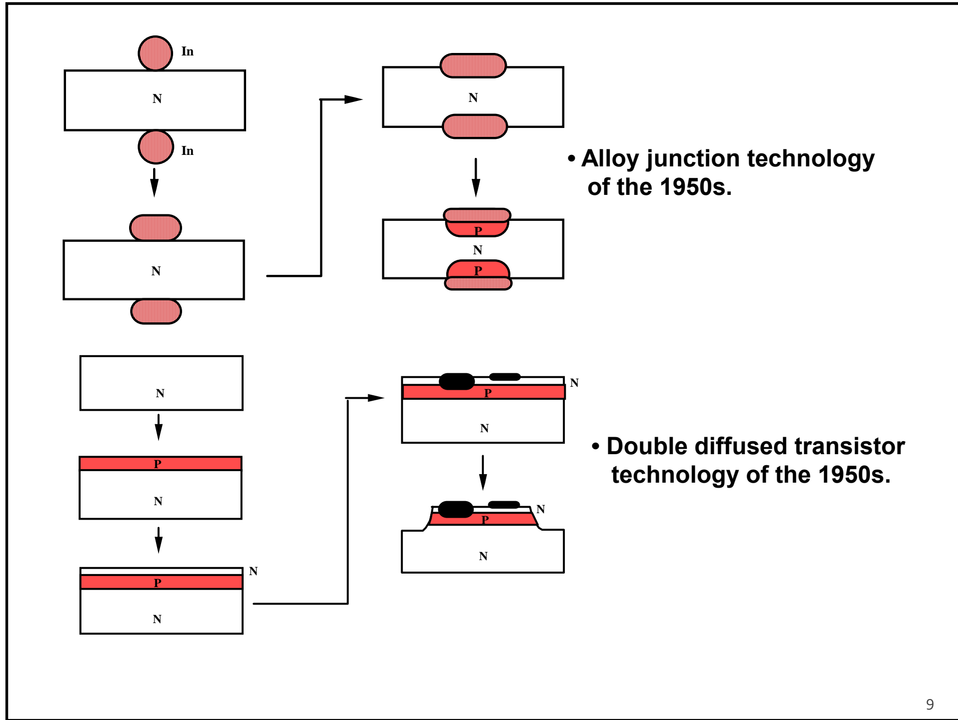


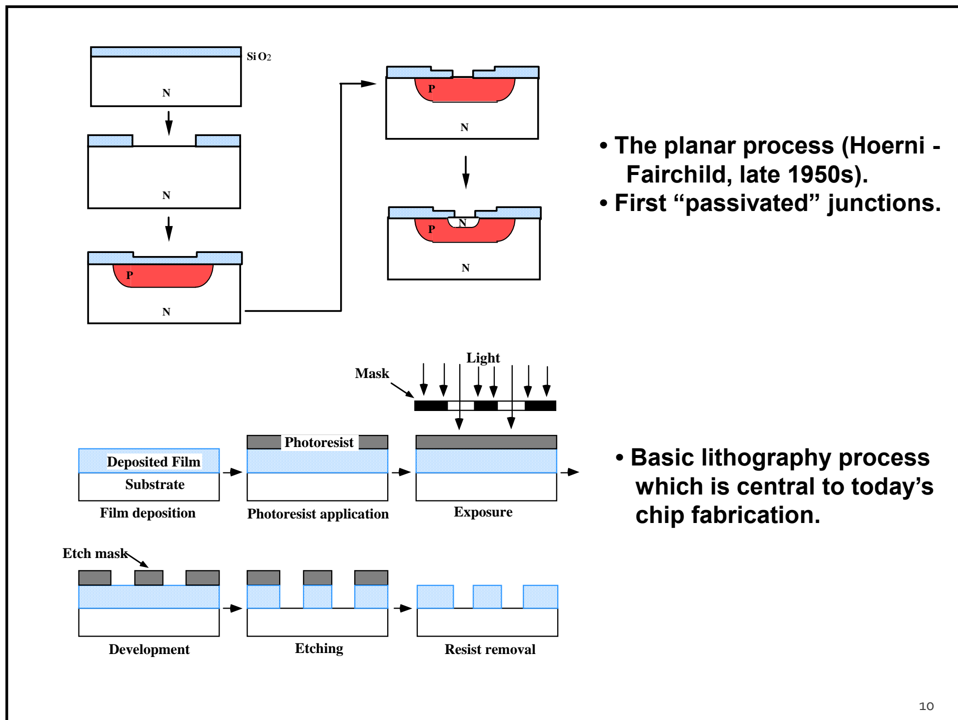


- Invention of the bipolar transistor - 1947, Bell Labs.
- Shockley's "creative failure" methodology



- Grown junction transistor technology of the 1950s


In
N
In
N
N
P
N
P
N
P
N
N
P
N
N
N
P
N
P
N
N
P
N
• Alloy junction technology of the 1950s.
• Double diffused transistor technology of the 1950s.
9


Si O2
N
N
P
N
P
N
P
N
N
• The planar process (Hoerni - Fairchild, late 1950s).
• First "passivated" junctions.
Light
Mask
Deposited Film
Substrate
Film deposition
Photoresist
Photoresist application
Exposure
• Basic lithography process which is central to today's chip fabrication.
Etch mask
Development
Etching
Resist removal
10

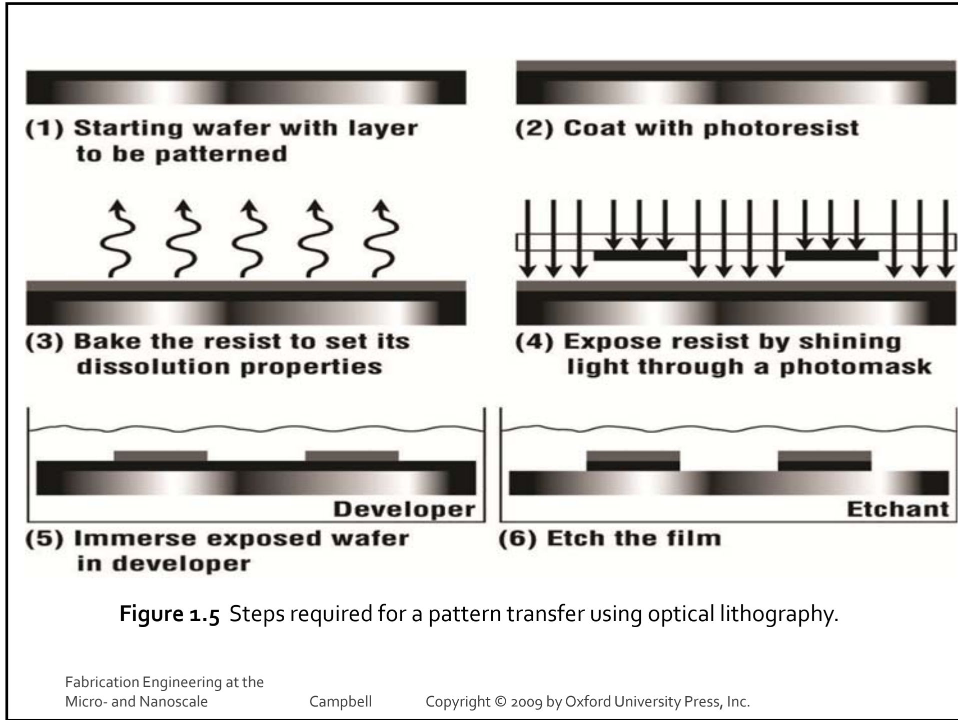
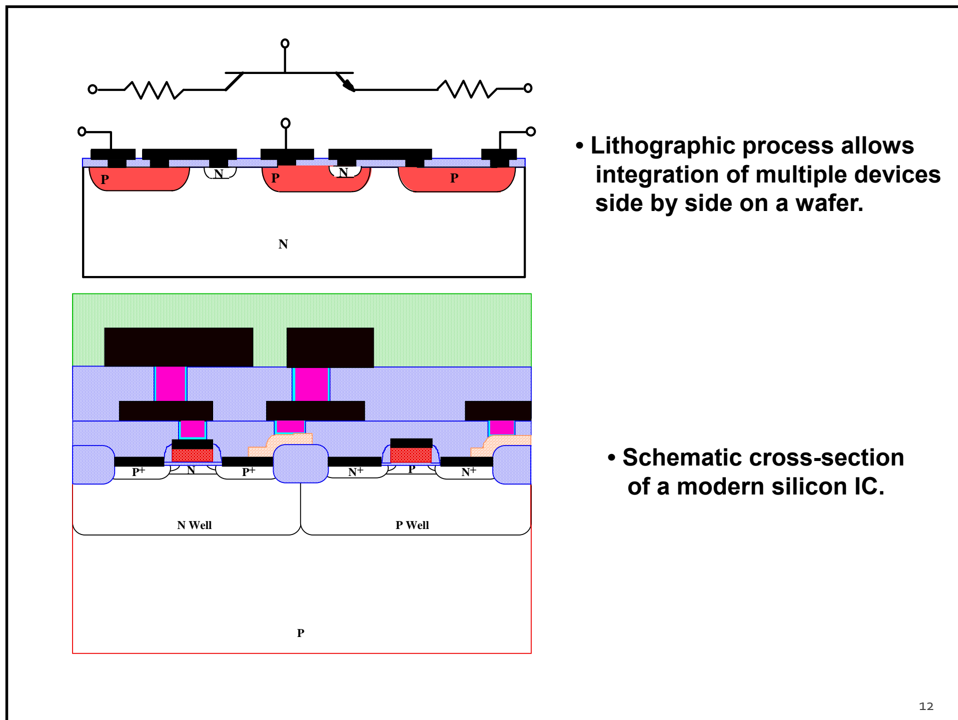


Figure 1.5 Steps required for a pattern transfer using optical lithography.



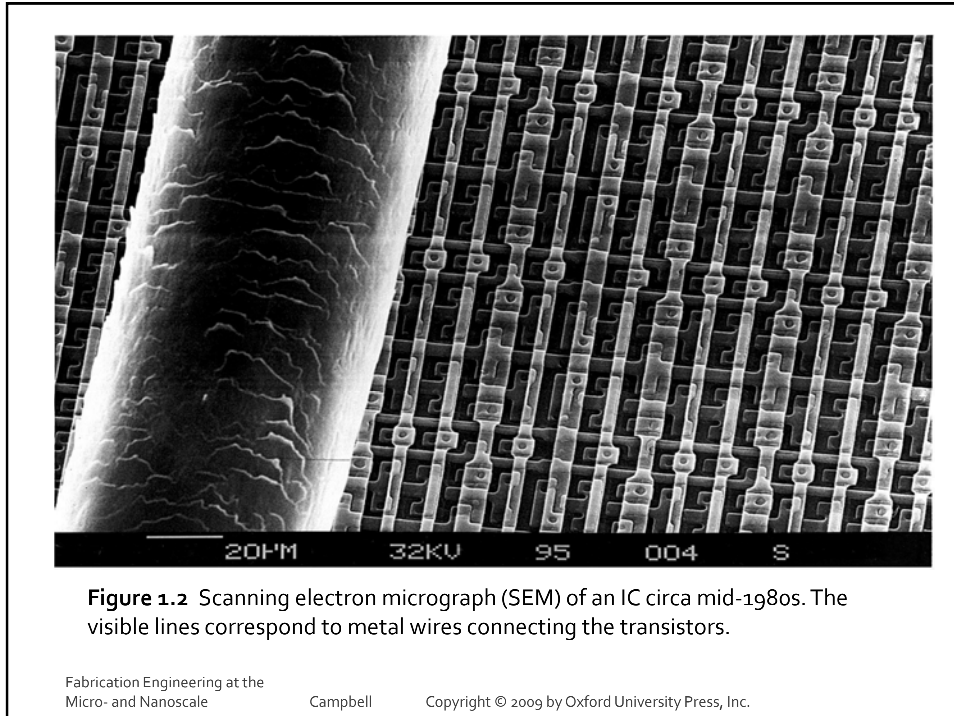


Figure 1.2 Scanning electron micrograph (SEM) of an IC circa mid-1980s. The visible lines correspond to metal wires connecting the transistors.

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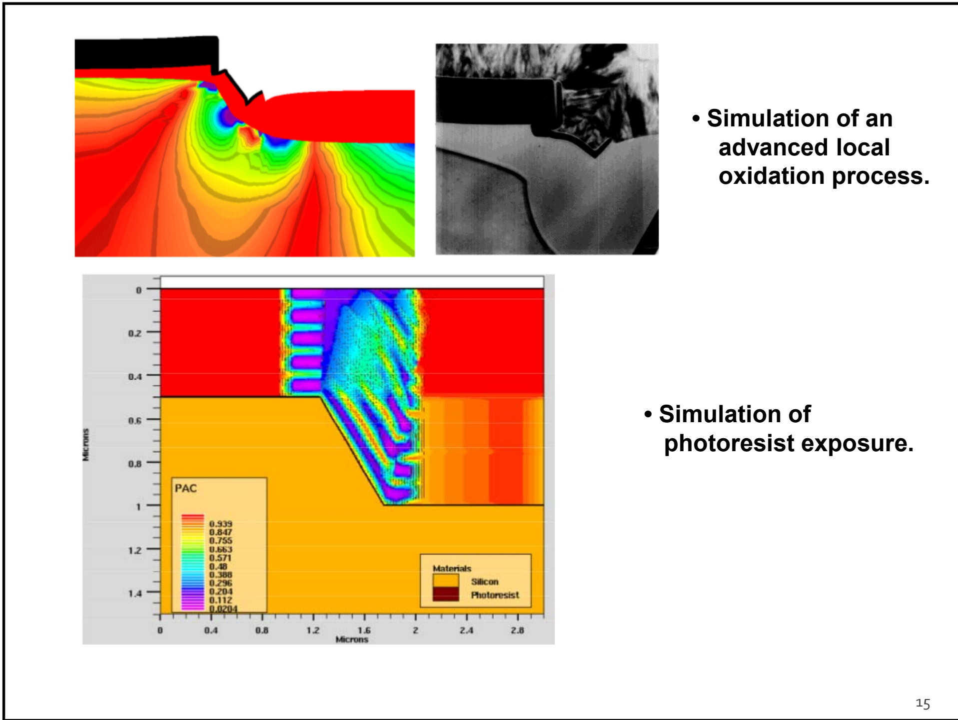
Computer Simulation Tools (TCAD)

•Most of the basic technologies in silicon chip manufacturing can now be simulated.
Simulation is now used for:

- **Designing new processes and devices.**
- **Exploring the limits of semiconductor devices and technology (R&D).**
- **"Centering" manufacturing processes.**
- **Solving manufacturing problems (what-if?)**



Challenges For The Future

- Having a "roadmap" suggests that the future is well defined and there are few challenges to making it happen.
- The truth is that there are enormous technical hurdles to actually achieving the forecasts of the roadmap. Scaling is no longer enough.
- 3 stages for future development:

"Technology Performance Boosters" | Invention

Silicide
Sidewall Spacer
Poly Gate
Gate Dielectric
Silicide
Source
Drain
R_{chan}
S/D Ext
S/D Ext
Substrate

Gate
Source
Drain

S
D
SiO_2
Si back gate

???

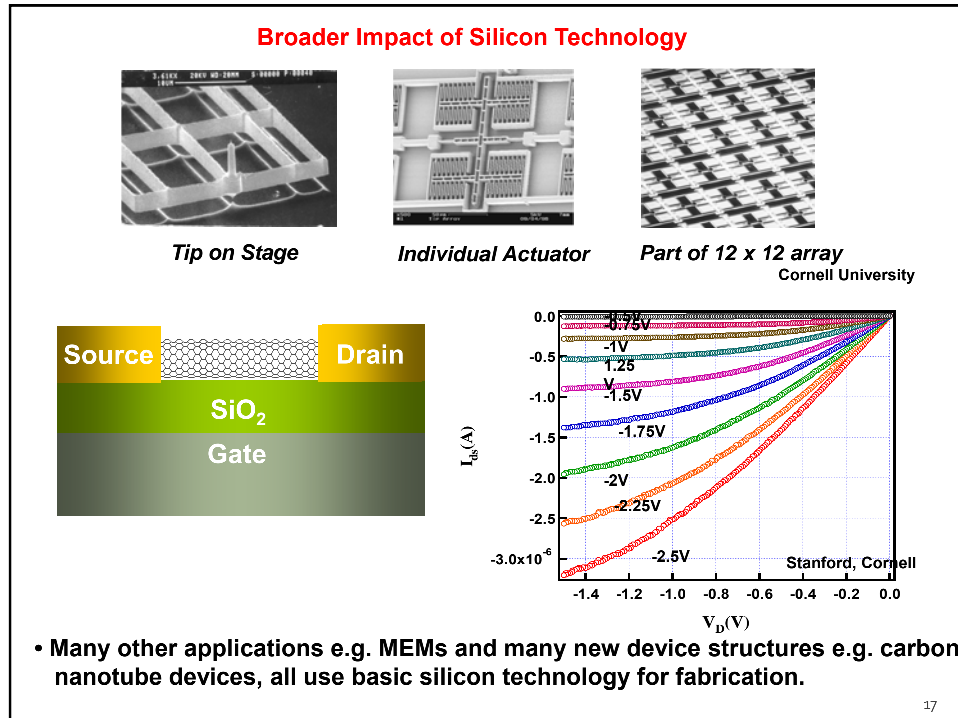
- Spin-based devices
- Molecular devices
- Rapid single flux quantum
- Quantum cellular automata
- Resonant tunneling devices
- Single electron devices

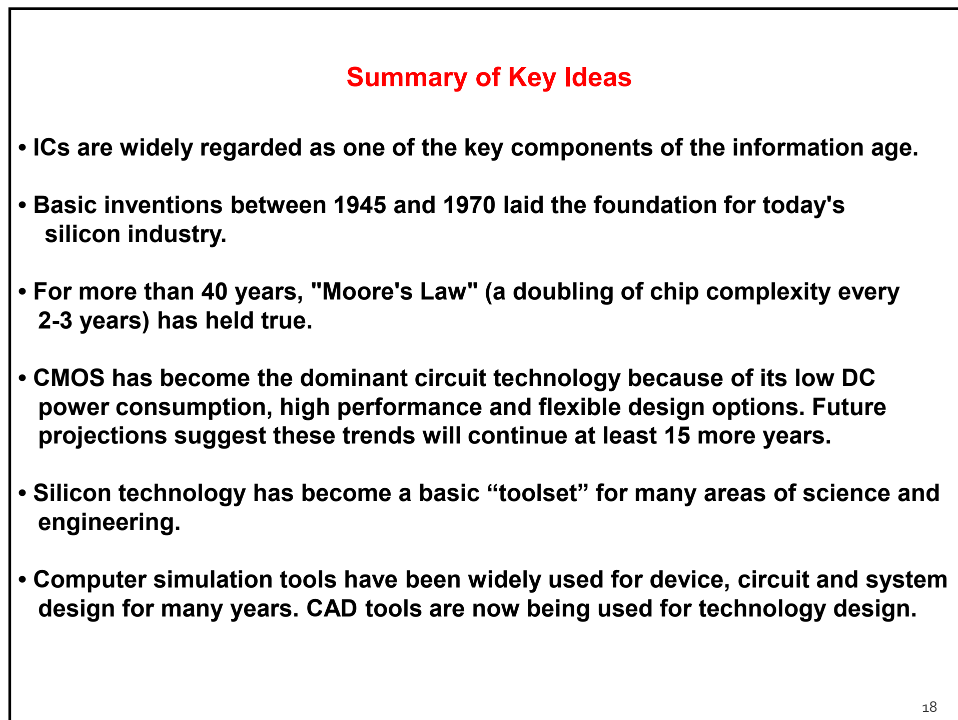
Materials/process innovations
NOW

Device innovations
IN 5-15 YEARS

Beyond Si CMOS
IN 15 YEARS??

16


Broader Impact of Silicon Technology
Tip on Stage
Individual Actuator
Part of 12 x 12 array
Cornell University
Source
Drain
SiO2
Gate
0.0
-0.5
-1.0
-1.5
-2.0
-2.5
-3.0x10-6
-1V
-1.5V
-1.75V
-2V
-2.25V
-2.5V
Ids(A)
-1.4 -1.2 -1.0 -0.8 -0.6 -0.4 -0.2 0.0
VD(V)
Stanford, Cornell
• Many other applications e.g. MEMs and many new device structures e.g. carbon nanotube devices, all use basic silicon technology for fabrication.
17


Summary of Key Ideas
• ICs are widely regarded as one of the key components of the information age.
• Basic inventions between 1945 and 1970 laid the foundation for today's silicon industry.
• For more than 40 years, "Moore's Law" (a doubling of chip complexity every 2-3 years) has held true.
• CMOS has become the dominant circuit technology because of its low DC power consumption, high performance and flexible design options. Future projections suggest these trends will continue at least 15 more years.
• Silicon technology has become a basic "toolset" for many areas of science and engineering.
• Computer simulation tools have been widely used for device, circuit and system design for many years. CAD tools are now being used for technology design.
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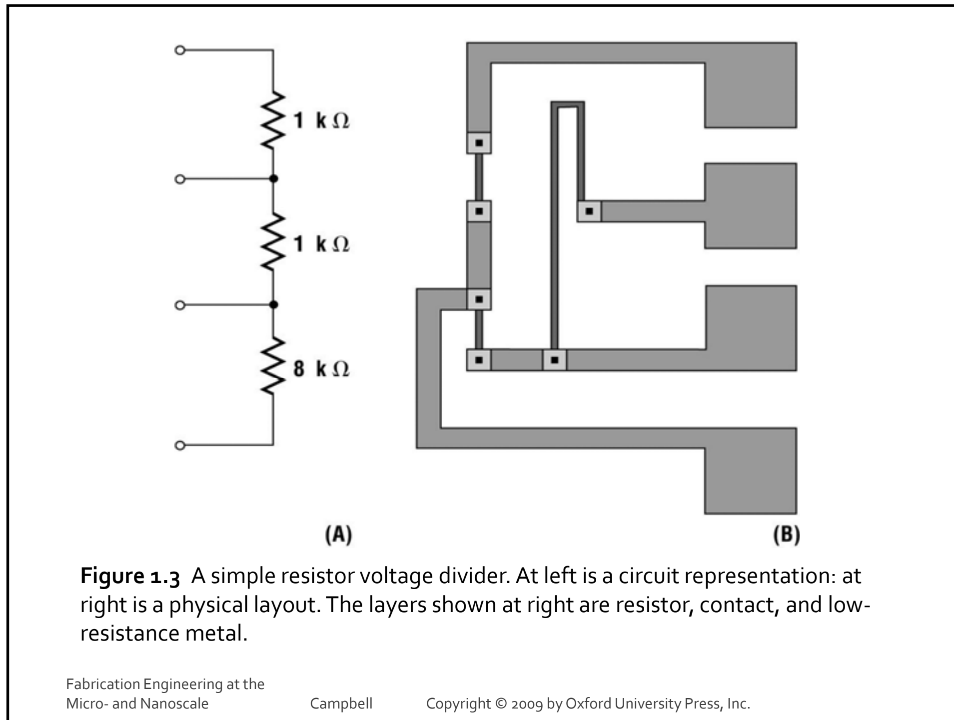

Figure 1.3 A simple resistor voltage divider. At left is a circuit representation: at right is a physical layout. The layers shown at right are resistor, contact, and low-resistance metal.

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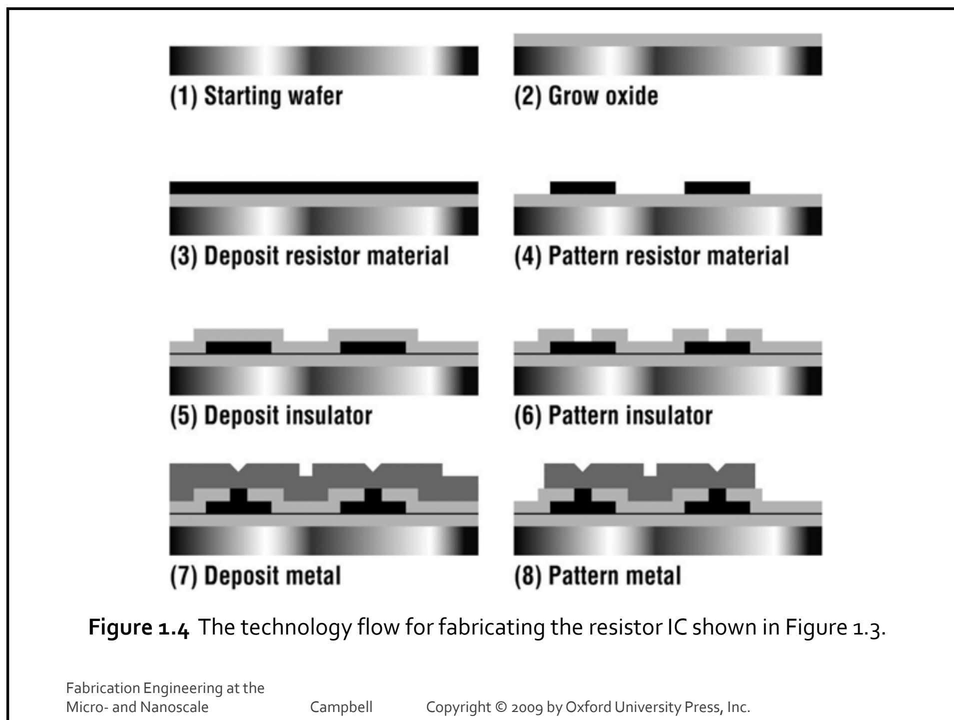

Figure 1.4 The technology flow for fabricating the resistor IC shown in Figure 1.3.

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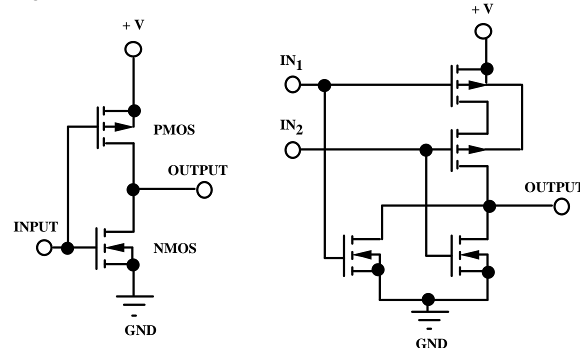
CMOS TECHNOLOGY

- We will describe a modern CMOS process flow.
- In the simplest CMOS technologies, we need to realize simply NMOS and PMOS transistors for circuits like those illustrated below.
- Typical CMOS technologies in manufacturing today add additional steps to implement multiple device V_{TH}, TFT devices for loads in SRAMs, capacitors for DRAMs etc.
- Process described here requires 16 masks (through metal 2) and > 100 process steps.
- There are many possible variations on the process flow described here



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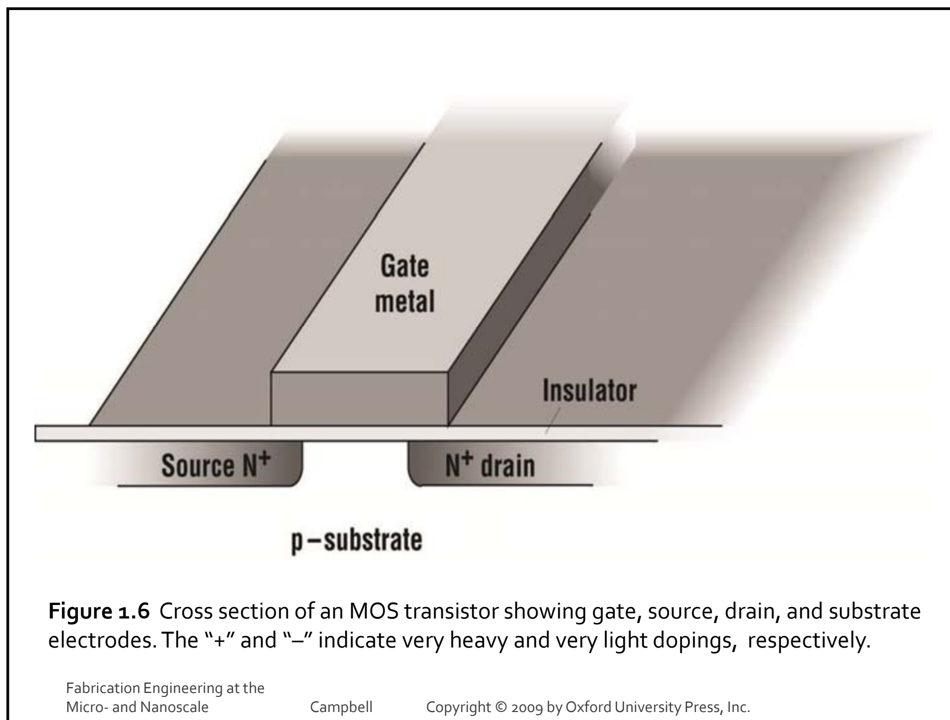

Figure 1.6 Cross section of an MOS transistor showing gate, source, drain, and substrate electrodes. The "+" and "–" indicate very heavy and very light dopings, respectively.

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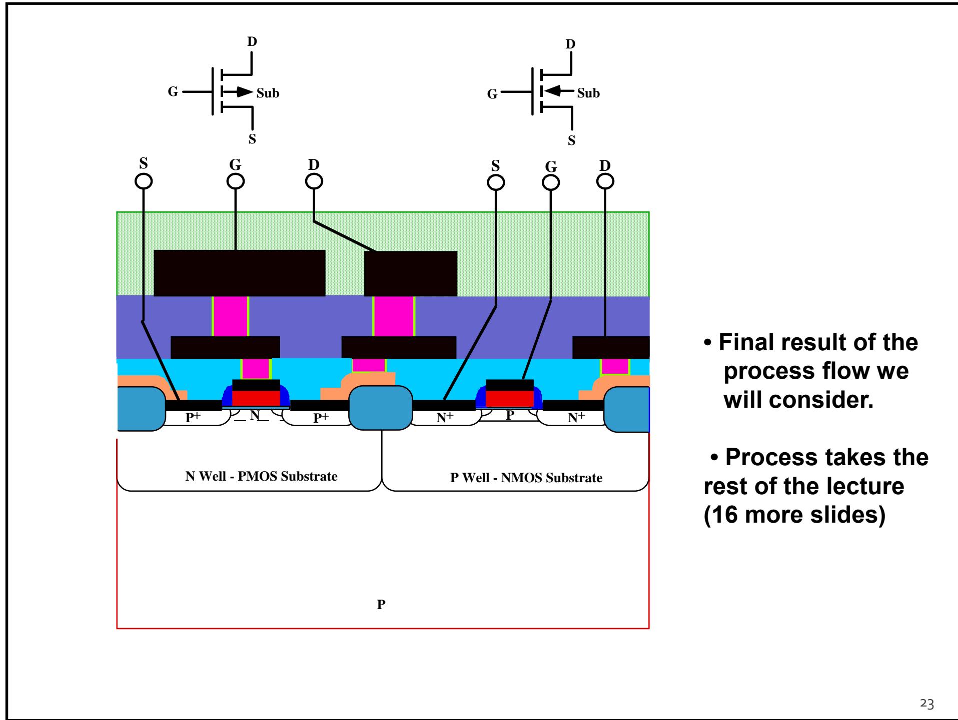
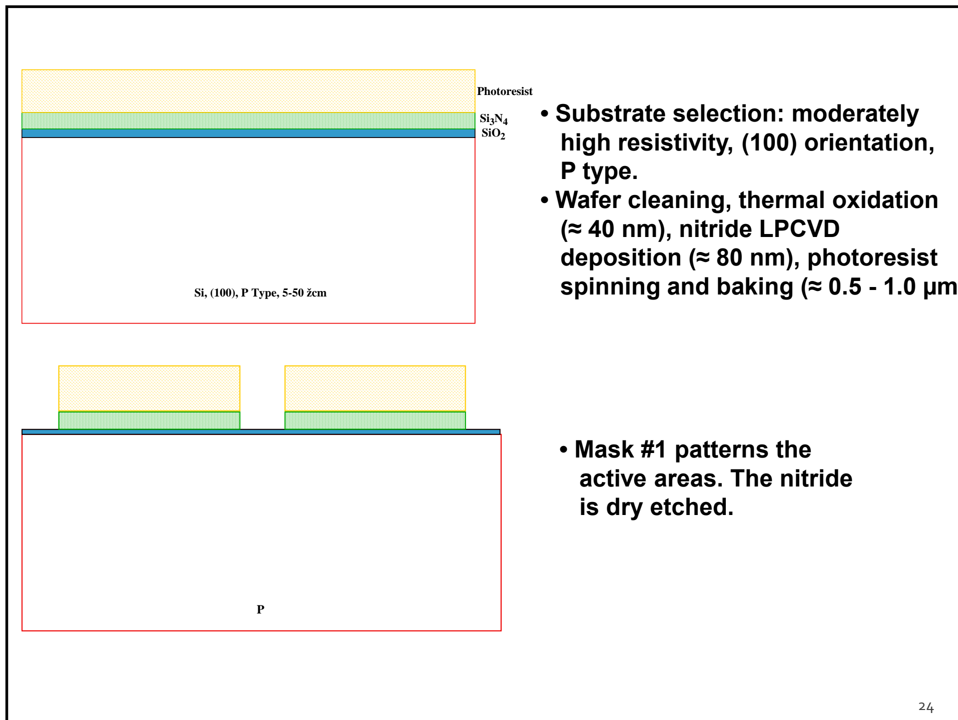

D
G
Sub
S
D
G
Sub
S
S
G
D
S
G
D
P+
N
P+
N+
P
N+
N Well - PMOS Substrate
P Well - NMOS Substrate
P
• Final result of the process flow we will consider.
• Process takes the rest of the lecture (16 more slides)
23


Photoresist
Si3N4
SiO2
Si, (100), P Type, 5-50 žcm
• Substrate selection: moderately high resistivity, (100) orientation, P type.
• Wafer cleaning, thermal oxidation (≈ 40 nm), nitride LPCVD deposition (≈ 80 nm), photoresist spinning and baking (≈ 0.5 - 1.0 μm)
P
• Mask #1 patterns the active areas. The nitride is dry etched.
24

- Field oxide is grown using a LOCOS process. Typically 90 min @ 1000 ˚C in H_2O grows ≈ 0.5 μm.
- Mask #2 blocks a B^+ implant to form the wells for the NMOS devices. Typically 10^{13} cm^{-2} @ 150-200 KeV.

25

- Mask #3 blocks a P^+ implant to form the wells for the PMOS devices. Typically 10^{13} cm^{-2} @ 300^+ KeV.
- A high temperature drive-in produces the “final” well depths and repairs implant damage. Typically 4-6 hours @ 1000 ˚C - 1100 ˚C or equivalent Dt.

26

Boron

N Well

P Well

P

Arsenic

N

- Mask #4 is used to mask the PMOS devices. A V_{TH} adjust implant is done on the NMOS devices, typically a 1-5 x 10^{12} cm^{-2} B^+ implant @ 50 - 75 KeV.

- Mask #5 is used to mask the NMOS devices. A V_{TH} adjust implant is done on the PMOS devices, typically 1-5 x 10^{12} cm^{-2} As^+ implant @ 75 - 100 KeV.

27

- The thin oxide over the active regions is stripped and a new gate oxide grown, typically 3 - 5 nm, which could be grown in 0.5 - 1 hrs @ 800 ˚C in O_2.

- Polysilicon is deposited by LPCVD (≈ 0.5 µm). An unmasked P^+ or As^+ implant dopes the poly (typically 5 x 10^{15} cm^{-2}).

28

- Mask #6 is used to protect the MOS gates. The poly is plasma etched using an anisotropic etch.

- Mask #7 protects the PMOS devices. A P^+ implant forms the LDD regions in the NMOS devices (typically 5 x 10^{13} cm^{-2} @ 50 KeV).

- Mask #8 protects the NMOS devices. A B^+ implant forms the LDD regions in the PMOS devices (typically 5 x 10^{13} cm^{-2} @ 50 KeV).

- Conformal layer of SiO_2 is deposited (typically 0.5 µm).
- Anisotropic etching leaves "sidewall spacers" along the edges of the poly gates.

31

- Mask #9 protects the PMOS devices, An As^+ implant forms the NMOS source and drain regions (typically 2-4 x 10^{15} cm^{-2} @ 75 KeV).
- Mask #10 protects the NMOS devices, A B^+ implant forms the PMOS source and drain regions (typically 1-3 x 10^{15} cm^{-2} @ 50 KeV).

32

- A final high temperature anneal drives-in the junctions and repairs implant damage (typically 30 min @ 900˚C or 1 min RTA @ 1000˚C.

- An unmasked oxide etch allows contacts to Si and poly regions.

33

- Ti is deposited by sputtering (typically 100 nm).

- The Ti is reacted in an N_2 ambient, forming $TiSi_2$ and TiN (typically 1 min @ 600 - 700 ˚C).

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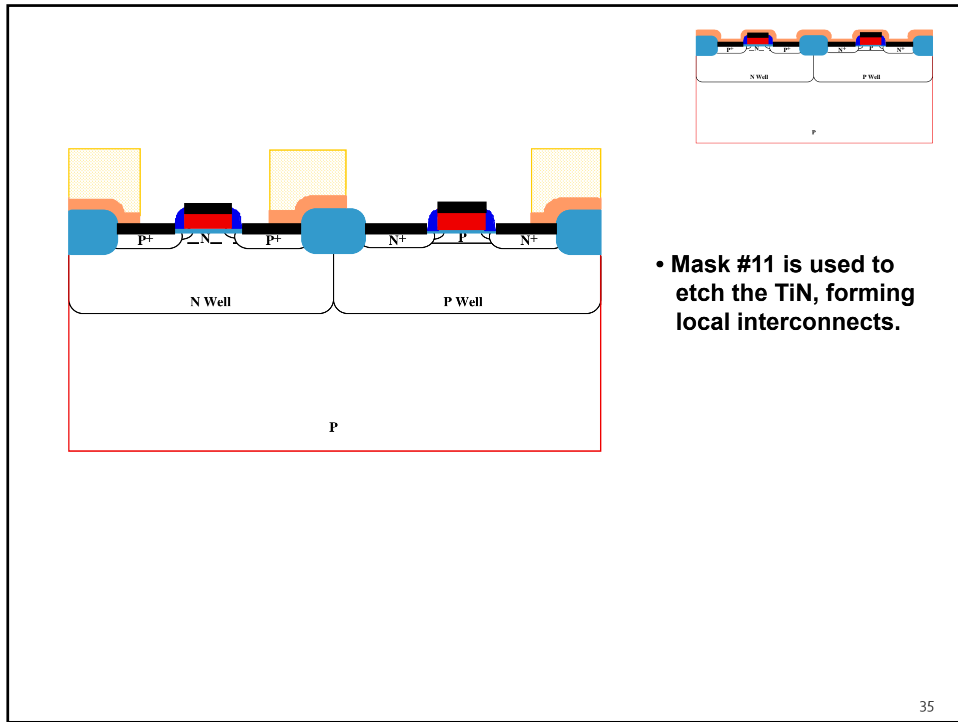
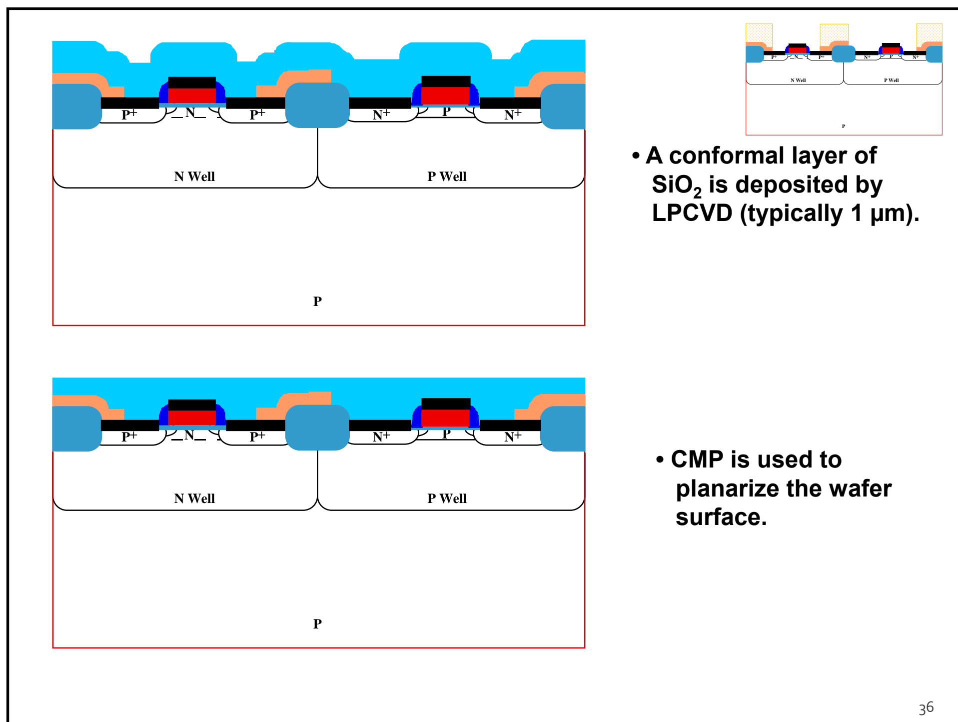

P+
N
P+
N+
P
N+
N Well
P Well
P
• Mask #11 is used to etch the TiN, forming local interconnects.
35


P+
N
P+
N+
P
N+
N Well
P Well
P
• A conformal layer of SiO_2 is deposited by LPCVD (typically 1 µm).
P+
N
P+
N+
P
N+
N Well
P Well
P
• CMP is used to planarize the wafer surface.
36

N Well
P Well
P

- Mask #12 is used to define the contact holes. The SiO_2 is etched.

W
TiN
N Well
P Well
P

- A thin TiN barrier layer is deposited by sputtering (typically a few tens of nm), followed by W CVD deposition.

37

N Well
P Well
P

- CMP is used to planarize the wafer surface, completing the damascene process.

N Well
P Well
P

- Al is deposited on the wafer by sputtering. Mask #13 is used to pattern the Al and plasma etching is used to etch it.

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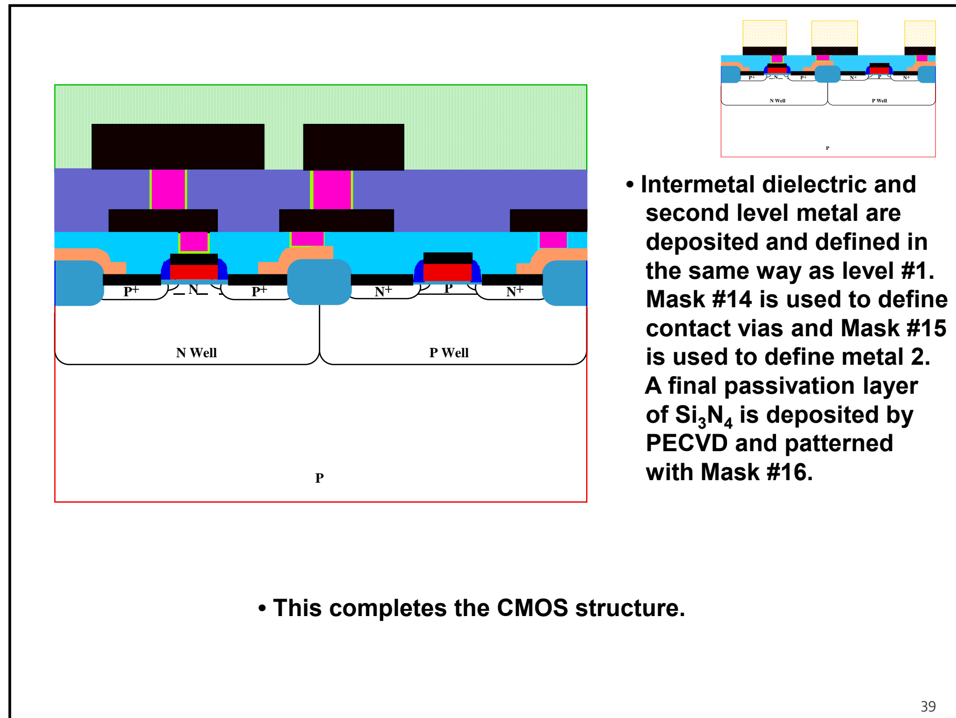

• Intermetal dielectric and second level metal are deposited and defined in the same way as level #1. Mask #14 is used to define contact vias and Mask #15 is used to define metal 2. A final passivation layer of Si_3N_4 is deposited by PECVD and patterned with Mask #16.

• This completes the CMOS structure.

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Summary of Key ideas

• This chapter serves as an introduction to CMOS technology.

• It provides a perspective on how individual technologies like oxidation and ion implantation are actually used.

• There are many variations on CMOS process flows used in industry.

• The process described here is intended to be representative, although it is simplified compared to many current process flows.

• Fabrication involves the repeated application of the same basic processes: oxidation, diffusion, ion implantation, lithography, etching, PVD/CVD, annealing, etc.

• Perhaps the most important point is that while individual process steps like oxidation and ion implantation are usually studied as isolated technologies, their actual use is complicated by the fact that IC manufacturing consists of many sequential steps, each of which must integrate together to make the whole process flow work in manufacturing. Subsequent process steps, especially at high temperatures, may change the properties of what has been done before.

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