Plastic Package Reliability

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Abstract

Today, plastic packaged integrated circuits are ubiquitous even for high-reliability applications. Reliability testing and standards play a key role in reliability engineering to achieve the necessary reliability performance. Traditional stress-based standards are easy to use but often over- or under-stress units and don't focus on key vulnerabilities, particularly moisture-related ones. Knowledge-based standards have evolved to fix this, but rely on knowledge of mechanisms, control of board manufacturing conditions, and understanding and specifying end use conditions. This motivates a survey of plastic package mechanisms and testing with particular focus on moisture-related mechanisms and testing. The moisture-related examples will cover HAST testing, and the "popcorn" mechanism.

Learning Objectives

1. Understand the philosophy and methods behind reliability testing of ICs as applied to plastic-packaged ICs.
2. Learn the historical development of the JEDEC temperature-humidity-bias (HAST) moisture reliability testing standard.
3. Get a practical overview of key thermal, thermo-mechanical, moisture (chemical), and moisture ("popcorn") mechanisms.

Biography

Dr. Shirley is with the Integrated Circuits Design and Test Laboratory at Portland State University. He joined PSU in 2008 on retirement after 23 years at Intel in 2007. At Intel, Dr. Shirley worked in Quality and Reliability, mostly in Technology Development. He started with package reliability fundamentals, including assembly test chips and moisture reliability, and moved on to moisture reliability of silicon, accelerated moisture test hardware (HAST), and industry standards. He also led the development of Intel's burn-in methodology. In 1995 he founded Sort-Test TD Q&R, which developed test methodologies such as test time reduction, socket elimination, etc. for high-volume manufacturing test. In 2004 he founded a group responsible for all Q&R modeling at Intel, after which he joined Intel's Corporate Quality Network staff where he was responsible, as Intel's Q&R Systems Architect and co-manager, for development of Intel's quality systems. Prior to Intel, Dr. Shirley worked at Motorola, and at U.S. Steel. He has a PhD in Physics from Arizona State University.