Design of 3D-Specific Systems

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History of Integration

- **Integrated Circuit**
  - *Fairchild*

- **Printed Circuit Board**
  - *Trilogy*

- **Wafer Scale Integration**

- **Multichip Modules**
  - *3DIC with TSV - Tezzaron*

Timeline:
- 1960
- 2010
History of Integration

Increased Performance/Price Faster than Alternative Technologies

How much? >~ 25%

1960 2010
Outline

- Overview of the Vectors in 3D Product Design
- Short term – find the low-hanging fruit
- Medium term – Logic on logic, memory on logic
- Long term – Extreme Scaling; Heterogeneous integration; Miniaturization
- Overcoming Barriers to Employment
Future 3DIC Product Space

- Image sensor
- Server Memory
- Interposer
- 3D Mobile
- Sensor Node
- Heterogeneous
- 3D Processor
- “Extreme” 3D Integration Time
3DIC Technology Set

Bulk Silicon TSVs and bumps (25 - 40 μm pitch)

Face to face microbumps (1 - 30 μm pitch)

$C_{TSV} \sim 30$ fF
... 3DIC Technology Set

TSVs in an SOI process

MIT Lincoln Labs
3DIC Technology Set

- Interposers: Thin film or 65/90 nm BEOL

- Assembly: Chip to Wafer or Wafer to wafer
Value Propositions

Fundamentally, 3DIC permits:

- **Shorter wires**
  - consuming less power, and costing less
  - The memory interface is the biggest source of large wire bundles

- **Heterogeneous integration**
  - Each layer is different!
  - Giving fundamental performance and cost advantages, particularly if high interconnectivity is advantageous

- **Consolidated “super chips”**
  - Reducing packaging overhead
  - Enabling integrated microsystems
The Demand for Memory Bandwidth

Computing

<table>
<thead>
<tr>
<th>MULTICORE AND REVERSE SCALING</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
</tr>
<tr>
<td>Frequency</td>
</tr>
<tr>
<td>No. of Cores</td>
</tr>
<tr>
<td>Core rel. IPC</td>
</tr>
<tr>
<td>Total Flops</td>
</tr>
<tr>
<td>Supply</td>
</tr>
<tr>
<td>Power</td>
</tr>
<tr>
<td>Bandwidth requirement</td>
</tr>
</tbody>
</table>

Similar demands in Networking and Graphics

Ideal: 1 TB / 1 TBps memory stack
Memory on Logic

Conventional

- x32 or x128
- nVidia

TSV Enabled

- Less Overhead
- Flexible bank access
- Less interface power
  - 3.2 GHz @ >10 pJ/bit
  - → 1 GHz @ 0.3 pJ/bit
- Flexible architecture
- Short on-chip wires

Processor

or

Mobile

N x 128 “wide I/O”
**Mobile Graphics**

- **Problem**: Want more graphics capacity but total power is constrained
- **Solution**: Trade power in memory interface with power to spend on computation

**POP with LPDDR2**

- LPDDR2
- Power Consumption
- GPU
- 532 M triangles/s

**TSV Enabled**

- TSV IO
- Power Consumption
- GPU
- 695 M triangles/s

Won Ha Choi
Dark Silicon

- Performance per unit power
  - Systems increasingly limited by power consumption, not number of transistors
  - “Dark Silicon” : Most of the chip will be OFF to meet thermal limits
## Energy per Operation

<table>
<thead>
<tr>
<th>Component</th>
<th>Energy per Operation</th>
</tr>
</thead>
<tbody>
<tr>
<td>DDR3</td>
<td>4.8 nJ/word</td>
</tr>
<tr>
<td>Optimized DRAM core</td>
<td>128 pJ/word</td>
</tr>
<tr>
<td>MIPS 64 core</td>
<td>400 pJ/cycle</td>
</tr>
<tr>
<td>11 nm 0.4 V core</td>
<td>200 pJ/op</td>
</tr>
<tr>
<td>45 nm 0.8 V FPU</td>
<td>38 pJ/Op</td>
</tr>
<tr>
<td>SERDES I/O</td>
<td>1.9 nJ/Word</td>
</tr>
<tr>
<td>20 mV I/O</td>
<td>128 pJ/Word</td>
</tr>
<tr>
<td>LPDDR2</td>
<td>512 pJ/Word</td>
</tr>
<tr>
<td>1 cm / high-loss interposer</td>
<td>300 pJ/Word</td>
</tr>
<tr>
<td>0.4 V / low-loss interposer</td>
<td>45 pJ/Word</td>
</tr>
<tr>
<td>On-chip/mm</td>
<td>7 pJ/Word</td>
</tr>
<tr>
<td>TSV I/O (ESD)</td>
<td>7 pJ/Word</td>
</tr>
<tr>
<td>TSV I/O (secondary ESD)</td>
<td>2 pJ/Word</td>
</tr>
</tbody>
</table>

Various Sources
Synthetic Aperture Radar Processor

- Built FFT in Lincoln Labs 3D Process

<table>
<thead>
<tr>
<th>Metric</th>
<th>Undivided</th>
<th>Divided</th>
<th>%</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bandwidth (GBps)</td>
<td>13.4</td>
<td>128.4</td>
<td>+854.9</td>
</tr>
<tr>
<td>Energy Per Write (pJ)</td>
<td>14.48</td>
<td>6.142</td>
<td>-57.6</td>
</tr>
<tr>
<td>Energy Per Read (pJ)</td>
<td>68.205</td>
<td>26.718</td>
<td>-60.8</td>
</tr>
<tr>
<td>Memory Pins (#)</td>
<td>150</td>
<td>2272</td>
<td>+1414.7</td>
</tr>
<tr>
<td>Total Area (mm²)</td>
<td>23.4</td>
<td>26.7</td>
<td>+16.8%</td>
</tr>
</tbody>
</table>

Thor Thorolfsson
3D FFT Floorplan

- All communications is vertical
- Support multiple small memories WITHOUT an interconnect penalty
  - AND Gives 60% memory power savings
RePartition FFT to Exploit Locality

- Every partition is a PE
- Every unique intersection is a memory
# 2DIC vs. 3DIC Implementation

<table>
<thead>
<tr>
<th>Metric</th>
<th>2D</th>
<th>3D</th>
<th>Change</th>
</tr>
</thead>
<tbody>
<tr>
<td>Total Area (mm²)</td>
<td>31.36</td>
<td>23.4</td>
<td>-25.3%</td>
</tr>
<tr>
<td>Total Wire Length (m)</td>
<td>19.107</td>
<td>8.238</td>
<td>-56.9%</td>
</tr>
<tr>
<td>Max Speed (Mhz)</td>
<td>63.7</td>
<td>79.4</td>
<td>+24.6%</td>
</tr>
<tr>
<td>Power @ 63.7MHz (mW)</td>
<td>340.0</td>
<td>324.9</td>
<td>-4.4%</td>
</tr>
<tr>
<td>FFT Logic Energy (µJ)</td>
<td>3.552</td>
<td>3.366</td>
<td>-5.2%</td>
</tr>
</tbody>
</table>

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Increasing the Return

1. 3D specific architectures

2. Exploiting Heterogeneity

3. Ultra 3D Scaling

High Performance
Low Power/Acceleration
Specialized RAM
General RAM

Deliver power at high voltage

Storage Class Memory

Power reduction through 3D architectures

Test and yield management

Scalable interconnect fabric

Aggressive Cooling
Extreme Integration

**Motivation:** Database Servers; High End DSP

Deliver power at high voltage

- High Capacity Memory
- Power reduction through 3D architectures
- Aggressive Cooling
- Test and yield management
- Scalable interconnect fabric
3D Miniaturization

Miniature Sensors
- $mm^3$ scale - Human Implantable (with Jan Rabaey, UC(B))
- $cm^3$ scale - Food Safety & Agriculture (with KP Sandeep, NCSU)

- Problems:
  - Power harvesting @ any angle (mm-scale)
  - Local power management (cm scale)

Peter Gadfort, Akalu Lentiro, Steve Lipa
“True” 3D Integration

- Orientation of mm-scale sensor will be random
  - Building antenna “through” 3DIC chip stack on edge will be very lossy
  - Need power harvesting on all 3 sides
  - Developed packaging integration flow to achieve this
## Mid-term Barriers to Deployment

<table>
<thead>
<tr>
<th>Barrier</th>
<th>Solutions</th>
</tr>
</thead>
<tbody>
<tr>
<td>Thermal</td>
<td>Early System Codesign of floorplan and thermal evaluation</td>
</tr>
<tr>
<td></td>
<td>DRAM thermal isolation</td>
</tr>
<tr>
<td>Test</td>
<td>Specialized test port &amp; test flow</td>
</tr>
<tr>
<td>Codesign</td>
<td>“Pathfinding” in SystemC</td>
</tr>
<tr>
<td></td>
<td>CAD Interchange Standards</td>
</tr>
<tr>
<td>Cost &amp; Yield</td>
<td>Supporting low manufacturing cost through design</td>
</tr>
</tbody>
</table>
Technologies for Thermal Isolation

- Introduce thermal isolation material between CPU and DRAM
- Use inductive coupling for communications

**Diagram:**
- CPU
- DRAMs
- Inductor
- SiO2
- Aerogel
- SiO2

**Graphical Data:**
- DRAM surface 50°C cooler than SOC vs. Only 9°C cooler with direct attachment

Ming Li, John Wilson, Neil DiSpigna
Thermal and Physical Flow:

1. Comprehensive technology file
2. Composite technology file
3. Resolution of simulation: Grid Size
4. WireX: Thermal Extractor
5. PETSC: Sparse Matrix Solver
6. Static Thermal Profile
7. Thermal MNAM
8. Power vector
9. Power
10. Petideal
11. Hotspot only
12. Transient Simulator e.g., HSPICE/FEEDA
13. Transient Thermal Profile

Shivam Priyadashi
Pathfinder 3D:

- Goals:
  - Electronic System Level (ESL) codesign for fast investigation of performance, logic, power delivery, and thermal tradeoffs
  - Focus to date: Thermal/speed tradeoffs – static and transient

- Test case: Stacking of Heterogeneous Cores

Design (a) vs. Design (b)

Cross section view

Shivam Priyadarshi
## Long-term Barriers to Deployment

<table>
<thead>
<tr>
<th>Barrier</th>
<th>Solutions</th>
</tr>
</thead>
<tbody>
<tr>
<td>Thermal &amp; Power Deliver</td>
<td>3D specific temperature management</td>
</tr>
<tr>
<td></td>
<td>New structures and architectures for power delivery</td>
</tr>
<tr>
<td>Test &amp; Yield management</td>
<td>Modular, scalable test and repair</td>
</tr>
<tr>
<td>Co-implementation</td>
<td>Support for Modularity and Scalability</td>
</tr>
<tr>
<td>Cost &amp; Yield</td>
<td>Supporting low manufacturing cost through design</td>
</tr>
</tbody>
</table>
3D Specific Interface IP

Proposal:

**Open Source IP for 3D and 2.5D interfaces**

An interface specification that supports signaling, timing, power delivery, and thermal control within a 3D chip-stack, 2.5D (interposer) structure and SIP solutions

(Proc. 3DIC 2011)
Conclusions

- Three dimensional integration offers potential to
  - Deliver memory bandwidth power-effectively;
  - Improve system power efficiency through 3D optimized codesign
  - Enable new products through aggressive Heterogeneous Integration

- Main challenges in 3D integration (from design perspective)
  - Effective early codesign to realize these advantages in workable solutions
  - Managing cost and yield, including test and test escape
  - Managing thermal, power and signal integrity while achieving performance goals
  - Scaling and interface scaling
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