# Carbon Nanotube FET-based circuits in the Presence of Metallic Tubes

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## ABSTRACT

CNFETs are at the forefront of devices being considered for post silicon era because of their excellent electronic properties. The properties like near ballistic transport, high, in the range of $10^3$~$10^4$cm$^2$/Vs, carrier mobilities in semiconducting CNTs, and easy integration of high-k dielectric material resulting in better gate electrostatics. Researchers are currently exploring two main types of CNFETs. These are the Schottky Barrier (SB) CNFETs and enhancement type CNFETs. The unipolar conduction characteristic and the absence of SB in enhancement type of CNFETs results in much lower *OFF* state leakage current and higher *ON* state current as compared to SB CNFET. Also, the enhancement-type CNFETs are compatible with the current CMOS technology. Physical implementations of some basic circuits build with CNFETs have been demonstrated.

The seminar will discuss basic properties of carbon nanotubes and its application as a channel material in FET devices. We will discuss major challenges associated with the fabrication of CNFETs such as variation in the diameter and spacing of tubes, unwanted growth of metallic tubes, and misaligned carbon nanotubes. The presence of misaligned tubes and unwanted growth of metallic tubes poses a serious challenge in the building of reliable carbon nanotube based integrated circuits.

We will focus on layout and circuit techniques to design robust CNFET-based digital circuits in the presence of fabrication challenges, variations, tube misalignment and metallic tubes. Yield-aware circuit techniques using different CNFET transistor configurations and tube-level, gate-level and circuit-level redundancy will be covered. Monte Carlo simulation results will be presented and discussed as a vehicle for further improvements. Methods to improve a functional yield under performance and power constraints will be presented.