

# SYLLABUS

## ECE321 Electronics I

Fall 2006

### Catalog

Introduction to solid state electronics, leading to the physical properties and characteristics of solid state electronic devices: diodes, bipolar junction transistors and field effect transistors. Analysis and design of analog systems and operational amplifier based amplifiers, active filters, oscillators and rectifier topologies. Application of a computer-aided design (CAD) tool, such as SPICE. Prerequisite: ECE222.

### Coordinator

<b>Name</b>	James E. Morris
<b>Office</b>	FAB 160-13
<b>Phone</b>	725-9588
<b>Email</b>	<a href="mailto:jmorris@cecs.pdx.edu">jmorris@cecs.pdx.edu</a>
<b>Office hours</b>	Tu/Th 10:00 - 11:00

### Credits

4

### Textbook(s)

**Microelectronic Circuits (5th Edition)**, Adel Sedra & Kenneth Smith  
Oxford University Press, (2004) ISBN: 0-19-514251-9, (required); [incl suppl probs]

### Reference(s)

**The Spice Book**, *Andrei Vladimirescu*, Wiley, 1994, ISBN 0-471-6926-9, 1st Ed.  
**SPICE**, *G.W.Roberts & A.S.Sedra*, OUP, 1997, (designed to supplement the text.)  
Other similar Spice support text, e.g. Tuinenga, Banzhaf, Rashid, Keown, Hambley  
"Electrical Engineering, 3e" Appendix D, (all P-H) [Optional]

### Prerequisites

By course number:

- ECE223

By topic:

- Linear circuit analysis: Norton/Thevenin, node/mesh analysis
- Ideal operational amplifiers and circuits
- Transfer functions and circuit responses in the time and frequency domains
- Spice, (or similar circuit simulator)

### Corequisites

By course number:

- ECE301 (Tues 15.00-17.50; Wed 16.00-18.50)

### Grading

- Eight weekly assignments (8 x 5% = 40%)
- One mid-term test (20%) & one final exam (20%)
- Eight ECE301 experiments (8 x 2.5% = 20%)

## Grading Scale

Letter Grade	Range
A	90+
A-	85 - 90
B+	80 - 85
B	75 - 80
B-	70 - 75
C+	65 - 70
C	60 - 65
C-	55 - 60
D+	50 - 55
D	45 - 50
D-	40 - 45
F	40-

## Course Outcomes

- Ability to analyze and design ideal OPAMP-based amplifiers & other circuits.
- Ability to analyze and design non-ideal OPAMP-based circuits.
- Understand the principles of solid-state material properties (energy band structures, conductivity through drift and diffusion, PN-junctions)
- Ability to analyze and design diode circuits for power conversion and wave-shaping.
- Understand the semiconductor principles of Bipolar Junction Transistor (BJT) and Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET) operation.
- Ability to analyze and design single-BJT amplifiers (in all three topologies) and switches (including biasing.)
- Ability to analyze and design single-MOSFET amplifiers (in all three topologies) and switches (including biasing.)
- Ability to use circuit simulation tools for the design and analysis of OPAMP, diode, BJT, and MOS circuits.

### Course/Program outcome mapping

## Structure

- Two 110 minute lecture periods per week.
- Weekly homework and reading assignments
- One mid-term test and one final exam
- (Occasional in-class “pop” quizzes)
- ECE301 lab (separate registration) grades included
- (“On-line” project/assignment/questionnaire)

## Topics

- I. **Introduction to Electronics.** Signal classification & spectrum; amplifiers, circuit models, & frequency response; digital logic inverter; ideal op-amp review. (2 hours)

- II. **Operational Amplifiers.** Op-amp circuits; non-ideal op-amps; frequency response of op-amps; large-signal limitations; integration & differentiation; macro-modeling. (6 hours)
- III. **Solid-state Electronics.** Semiconductors: drift & diffusion currents; covalent bonds, doping, & energy band models; mobility & resistivity; PN junction; MOSFET structure & operation; BJT structure & operation. (6 hours)
- IV. **Diodes.** Diode characteristics; diode models; zener diodes ; rectification ; clipping & clamping; op-amp superdiode. (4 hours)
- V. **Bipolar Junction Transistors.** BJT characteristics & operation regions; BJT switch & inverter; single-stage amplifier topologies; DC analysis & biasing; small signal operation & models; high-frequency effects & CE frequency response; Spice model. (11 hours)
- VI. **MOSFETs.** MOSFET characteristics & operation regions; MOSFET switch & amplifier; DC analysis & biasing; small signal operation & models; single-stage amplifier topologies; high-frequency effects & CS frequency response; CMOS inverter, Spice model. (7 hours)

## Assignments

Week	Reading	ECE301 Lab & Homework problems
1	1.1 – 1.7 2.1 – 2.3	Lab organization meeting Problems 1: Sections 1.1 – 2.3
2	2.4 – 2.6 2.7 – 2.9	Expt 1: PSpice Introduction Problems 2: Sections 2.4 – 2.9
3	3.1 – 3.3 3.4 - 3.6	Expt 2: Opamp Circuits Problems 3: Sections 3.1 – 3.6
4	3.7 - 3.9 4.1 – 4.2	Expt 3: Audio Equalizer Problems 4: Sections 3.7 – 4.2
5	4.3 – 4.5 4.6 – 4.7	Expt : Diode Characteristics Problems 5: Sections 4.3 – 4.7
6	5.1 – 5.2 5.3 – 5.4	Expt 5: Diode Circuits Problems 6: Sections 5.1 – 5.4
7	Mid-term test: first 10 lectures 5.5 – 5.6	Expt 6: MOSFETs
8	5.7 5.8 – 5.9	Problems 7: Sections 5.5 – 5.7 Expt 7: BJT Biasing
9	4.8 – 4.9 Thanksgiving	Problems 8: Sections 4.8, 4.9, 5.8, & 5.9 Expt 8: BJT Amplifiers
10	4.10 - 4.12 5.10-12; Review	

### Note:

Problems 1-6 assigned Thur.  
Problems 7-8 assigned Tues.  
Problems due at the following Tuesday lecture at noon, returned in Thur lecture.

Final exam:  
Thur 7<sup>th</sup> Dec  
10.15 – 12.05pm

Prepared by: James E. Morris

Updated: Oct 9<sup>th</sup>, 2006

- Notes: 1. Course information (outline, assignments, textbook figures) at: <http://www.ece.pdx.edu/~jmorris/ece321>  
2. Lecture streaming videos available from:

## Teaching Assistants

### ECE321:

Hui She

FAB 25-03

Recitation:

Office hours:

[hshe@pdx.edu](mailto:hshe@pdx.edu)

Thursday 14.00-14.50  
NH 385

Thursday 15.00-16.30  
FAB 25-03

### ECE301 (Tues 15.00-17.50):

Tony Muilenburg

FAB

Office hours:

[tonymuilenburg@gmail.com](mailto:tonymuilenburg@gmail.com)

[muilenta@pdx.edu](mailto:muilenta@pdx.edu)

(WebCT preferred)

Tuesday 14.00-14.50  
(before lab) in FAB 100

### ECE301 (Wed 16.00-18.50):

Ping Xu

FAB

Office hours:

[pingxu@cecs.pdx.edu](mailto:pingxu@cecs.pdx.edu)

(WebCT preferred)

Wednesday 15.00-15.50  
(before lab) in FAB 100