EXERCISE: Find the Q-point in the circuit in Fig. 4.36 if R_S is changed to 62 kΩ.

ANSWER: (25.4 μA, −6.52 V)

EXERCISE: (a) Use SPICE to find the Q-point in the circuit in Fig. 4.36. (b) Repeat if R_S is changed to 62 kΩ. (c) Repeat parts (a) and (b) with $\lambda = 0.02$. (*Suggestion:* Insert an ammeter to measure I_D and a voltmeter to measure V_{DS}.)

ANSWERS: (a) (34.4 μA, −6.08 V); (b) (25.4 μA, −6.52 V); (c) (35.9 μA, −5.91 V), (26.3 μA, −6.39 V)

EXAMPLE 4.10 TWO-RESISTOR BIAS FOR THE PMOS TRANSISTOR

The circuit in Fig. 4.37 applies the two-resistor bias technique of Ex. 4.7 to the PMOS transistor. R_D determines both the drain current and the source-drain voltage of the transistor. Resistor R_G provides a dc connection between the gate and drain, and also serves to isolate the two terminals when signals are applied.

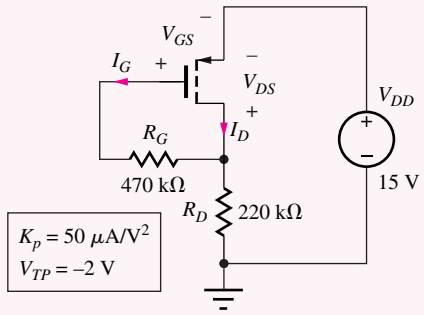

Figure 4.37 Two-resistor bias for a PMOS transistor.

PROBLEM Find the Q-point (I_D, V_{DS}) for the PMOS FET in the two resistor bias circuit of Fig. 4.37.

SOLUTION **Known Information and Given Data:** The circuit schematic in Fig. 4.37 with $V_{DD} = 15$ V, $R_D = 220\ \text{k}\Omega$, $R_G = 470\ \text{k}\Omega$, $K_P = 50\ \mu\text{A/V}^2$, and $V_{TP} = -2$ V

Unknowns: I_D, V_{DS}, and V_{GS}

Approach: First find the value of V_{GS}; use V_{GS} to find I_D; use I_D to find V_{DS}.

Assumptions: $I_G = 0$. Note that the region of operation is actually known. For $I_G = 0$, there is no voltage drop across resistor R_G, and $V_{GS} = V_{DS}$. Since the transistor is an enhancement-mode device ($V_{TP} < 0$) , it is automatically operating in the saturation region — remember the Design Note in Sec. 4.8!

Analysis: Writing loop equations for V_{GS} and V_{DS} yields

$$\begin{aligned} V_{GS} + (470\,\text{k}\Omega)I_G + V_{DS} &= 0 \\ 15\,\text{V} + V_{DS} - (220\,\text{k}\Omega)I_D &= 0 \end{aligned} \tag{4.69}$$

Because $I_G = 0$, $V_{DS} = V_{GS}$, and the enhancement-mode transistor is "saturated by connection." Using Eq. (4.35) with $\lambda = 0$ and the transistor parameters from the figure, the second expression in Eq. (4.69) yields

$$15\,\text{V} + V_{GS} - (220\,\text{k}\Omega)\frac{50}{2}\frac{\mu\text{A}}{\text{V}^2}(V_{GS} + 2)^2 = 0$$

and

$$V_{GS} = -0.369\,\text{V}, -3.45\,\text{V}$$

Because $V_{TP} = -2$ V, $V_{GS} = -0.369$ V is not sufficient to turn on the PMOS transistor, so the answer must be $V_{GS} = -3.45$ V, which gives

$$I_D = 52.5\mu\text{A} \qquad \text{and} \qquad V_{DS} = -3.45\,\text{V}$$

Check of Results: Although we know that $V_{DS} = V_{GS}$, let us double check the voltages for practice: $V_{GS} - V_{TP} = -1.45$ V, and so it is true that $|V_{DS}| > |V_{GS} - V_{TP}|$. The assumption of saturation region operation is correct, and the final Q-point is $(I_D, V_{DS}) = (52.5\ \mu\text{A}, -3.45\ \text{V})$.

Evaluation and Discussion: The two-resistor bias circuit in Fig. 4.37 is another example of a circuit that uses negative feedback to stabilize the operating point. The negative feedback mechanism can be viewed in the following manner. Suppose for some reason that I_D begins to increase. An increase in I_D will cause a decrease in the magnitude of V_{DS} and hence a decrease in the size of V_{GS} since $V_{GS} = V_{DS}$. This decrease will cause I_D to decrease back toward its original value.

EXERCISE: Find the Q-point of the PMOS transistor in Fig. 4.37 if $V_{TP} = -1$ V and $K_P = 250\,\mu\text{A/V}^2$.

ANSWER: (60.5 μA, −1.70 V) Note the relatively small shift in I_D for large changes in K_P and V_{TP} — another example of the stabilizing effect of feedback.

EXERCISE: Use SPICE to find the Q-point in the circuit in Fig. 4.37

4.10 CURRENT SOURCES AND THE MOS CURRENT MIRROR

Current sources are widely used to establish transistor operating points in integrated circuits, and an important application of the MOSFET (as well as other electronic devices) is as an electronic current source. The i-v characteristic for an ideal current source is shown in Fig. 4.38, in which an ideal source provides a constant 50-μA output current regardless of the polarity of the voltage across the source.

The output characteristic of an NMOS transistor with a fixed gate-source bias $V_{GS} = 3$ V is also given in Fig. 4.38. If the value of V_{DD} is chosen to be larger than the value needed to pinch off the MOSFET [in this case, $V_{DD} \geq (V_{GS} - V_{TN}) = 3 - 1 = 2$ V], then the FET drain current will also be constant at 50 μA. For $V_{DD} \geq 2$ V, the MOSFET represents an **electronic current source** with a 50-μA output current.

Figure 4.39 shows an NMOS transistor biased with a fixed 3-V dc source. This simple two-terminal MOSFET circuit will behave as an electronic current source as long as the external