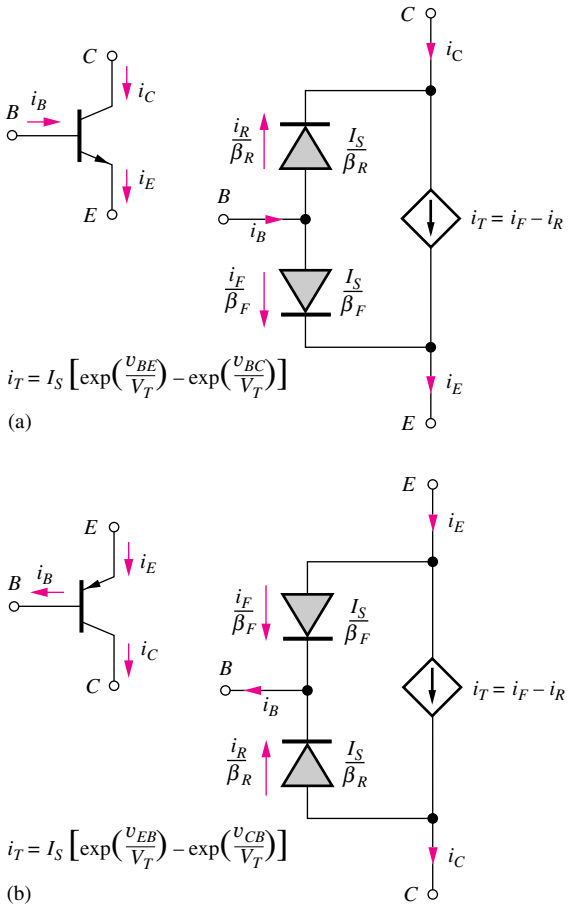

Figure 5.8 (a) Transport model equivalent circuit for the *npn* transistor. (b) Transport model equivalent circuit for the *pnp* transistor.

EXERCISE: Find i_T if $I_S = 10^{-15}$ A, $V_{BE} = 0.75$ V, and $V_{BC} = -2.0$ V.

ANSWER: 10.7 mA

EXERCISE: Find the dc transport current I_T for the transistor in Example 5.1 on page 282.

ANSWER: $I_T = 1.47$ mA

5.5 THE EBERS-MOLL MODEL (ADVANCED TOPIC)

The classic mathematical model for the bipolar junction transistor is the Ebers-Moll model formulated by J. J. Ebers and J. L. Moll from Bell Laboratories in the early 1950s [5]. The Ebers-Moll model provides an alternative view or representation of the equations developed in Sec. 5.2 and is formulated using the same superposition of currents in the forward and reverse directions.

5.5.1 Forward Characteristics of the *npn* Transistor

The total current crossing the emitter-base junction in the forward direction in Fig. 5.3 is described by Eq. (5.5) and can be rewritten as

$$i_E = \frac{I_S}{\alpha_F}\left[\exp\left(\frac{v_{BE}}{V_T}\right) - 1\right] = I_{ES}\left[\exp\left(\frac{v_{BE}}{V_T}\right) - 1\right] \qquad \text{where } I_{ES} = \frac{I_S}{\alpha_F} \tag{5.20}$$

in which the new parameter I_{ES} represents the reverse saturation current of the base-emitter diode. The collector current in Eq. (5.1) can be rewritten in terms of I_{ES} as

$$i_C = I_S\left[\exp\left(\frac{v_{BE}}{V_T}\right) - 1\right] = \alpha_F I_{ES}\left[\exp\left(\frac{v_{BE}}{V_T}\right) - 1\right] \tag{5.21}$$

The forward common-base current gain α_F represents the fraction of the emitter current that crosses the base and appears in the collector terminal.

5.5.2 Reverse Characteristics of the *npn* Transistor

For the reverse direction depicted in Fig. 5.4, the current crossing the collector-base junction is described by Eq. (5.11) and can be written as

$$i_C = -\frac{I_S}{\alpha_R}\left[\exp\left(\frac{v_{BC}}{V_T}\right) - 1\right] = -I_{CS}\left[\exp\left(\frac{v_{BC}}{V_T}\right) - 1\right] \qquad \text{where } I_{CS} = \frac{I_S}{\alpha_R} \tag{5.22}$$

The new parameter I_{CS} represents the reverse saturation current of the base-emitter diode. The emitter current from Eq. (5.9) can be rewritten in terms of I_{CS} as

$$i_E = -I_S\left[\exp\left(\frac{v_{BC}}{V_T}\right) - 1\right] = -\alpha_R I_{CS}\left[\exp\left(\frac{v_{BC}}{V_T}\right) - 1\right] \tag{5.23}$$

The reverse common-base current gain α_R represents the fraction of the collector current that crosses the base from the emitter terminal.

5.5.3 The Ebers-Moll Model for the *npn* Transistor

The full Ebers-Moll equations are obtained by combining Eqs. (5.20) to (5.23):

$$\begin{aligned} i_E &= I_{ES}\left[\exp\left(\frac{v_{BE}}{V_T}\right) - 1\right] - \alpha_R I_{CS}\left[\exp\left(\frac{v_{BC}}{V_T}\right) - 1\right] \\ i_C &= \alpha_F I_{ES}\left[\exp\left(\frac{v_{BE}}{V_T}\right) - 1\right] - I_{CS}\left[\exp\left(\frac{v_{BC}}{V_T}\right) - 1\right] \end{aligned} \tag{5.24}$$

This model contains four parameters, I_{ES}, I_{CS}, α_F, and α_R. From the definitions of I_{ES} and I_{CS}, we can obtain the important auxillary relation

$$\alpha_F I_{ES} = \alpha_R I_{CS} \tag{5.25}$$

which shows that there are only three independent parameters in the Ebers-Moll model, just as in the transport formulation. The base current, given by $i_B = i_E - i_C$, is

$$i_B = (1-\alpha_F)I_{ES}\left[\exp\left(\frac{v_{BE}}{V_T}\right)-1\right] + (1-\alpha_R)I_{CS}\left[\exp\left(\frac{v_{BC}}{V_T}\right)-1\right] \tag{5.26}$$

which is equivalent to the base current expression in Eq. (5.13).

5.5.4 The Ebers-Moll Model for the *pnp* Transistor

The equation set for the *pnp* transistor can be derived in a manner analogous to that of the *npn* device, and such an analysis yields Eq. (5.27):

$$\begin{aligned} i_E &= I_{ES}\left[\exp\left(\frac{v_{EB}}{V_T}\right)-1\right] - \alpha_R I_{CS}\left[\exp\left(\frac{v_{CB}}{V_T}\right)-1\right] \\ i_C &= \alpha_F I_{ES}\left[\exp\left(\frac{v_{EB}}{V_T}\right)-1\right] - I_{CS}\left[\exp\left(\frac{v_{CB}}{V_T}\right)-1\right] \\ i_B &= (1-\alpha_F)I_{ES}\left[\exp\left(\frac{v_{EB}}{V_T}\right)-1\right] + (1-\alpha_R)I_{CS}\left[\exp\left(\frac{v_{CB}}{V_T}\right)-1\right] \end{aligned} \tag{5.27}$$

Note that the current and voltage polarities for the *pnp* transistor are all opposite those of the *npn* device, as originally shown in Fig. 5.6.

5.5.5 Equivalent Circuit Representations for the Ebers-Moll Models

Equivalent circuit representations of the Ebers-Moll equations are useful as aids in hand analysis and have been used as the model in many circuit simulation packages. The Ebers-Moll equivalent circuits for the *npn* and *pnp* transistors are presented in Figs. 5.9(a) and 5.9(b), respectively. Diode currents i_F and i_R are established by the voltages v_{BE} and v_{BC} applied to the base-emitter and base-collector junctions, as represented by Eqs. (5.20) and (5.22), and the current-controlled current sources represent the portions of the diode currents that are transported across the base region of the devices.

Exercise: What are the values of α_F, α_R, I_{ES}, and I_{CS} for the transistor in Example 5.1? Show that $\alpha_F I_{ES} = \alpha_R I_{CS}$

Answers: 0.980, 0.500, 1.02×10^{-16} A, 2.00×10^{-16} A, 1.00×10^{-16} A $= 1.00 \times 10^{-16}$ A

Exercise: Derive the Ebers-Moll equation set that describes the *pnp* transistor.

Answer: See Eq. (5.27)

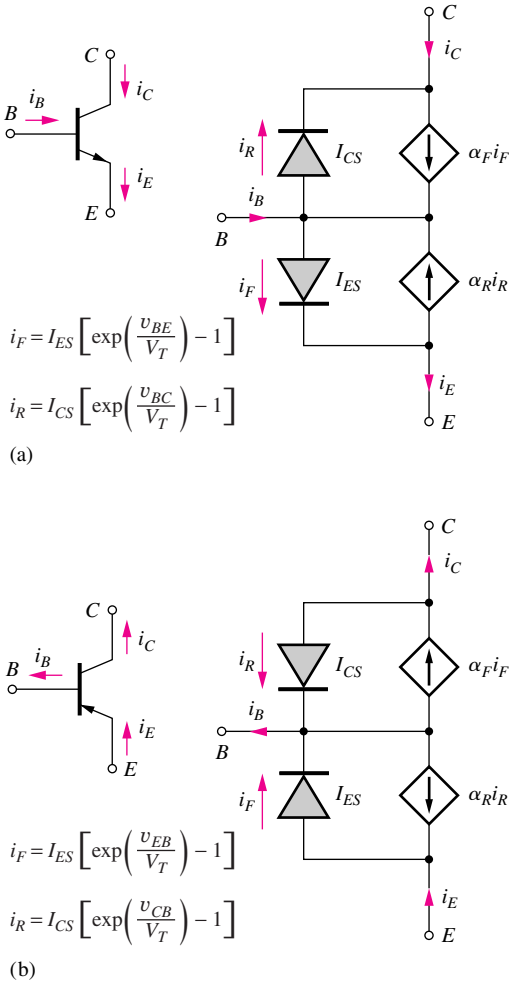

Figure 5.9 Equivalent circuit models for the Ebers-Moll models for the (a) *npn* and (b) *pnp* transistors.

5.6 THE OPERATING REGIONS OF THE BIPOLAR TRANSISTOR

In the bipolar transistor, each *pn* junction may independently be forward-biased or reverse-biased, so there are four possible regions of operation, as defined in Table 5.2. The operating point establishes the region of operation of the transistor and can be defined by any two of the four terminal voltages or currents. The characteristics of the transistor are quite different for each of the four regions of operation, and in order to simplify our circuit analysis task, we need to be able to make an educated guess as to the region of operation of the BJT.

When both junctions are reverse-biased, the transistor is essentially nonconducting or *cut off* (**cutoff region**) and can be considered an open switch. If both junctions are forward-biased, the transistor is operating in the **saturation region**[8] and appears as a closed switch. Cutoff and saturation (colored in Table 5.2) are most often used to represent the two states in binary logic circuits

[8] It is important to note that the saturation region of the bipolar transistor does *not* correspond to the saturation region of the FET. This unfortunate use of terms is historical in nature and something we just have to accept.