Rewriting Eq. (3.31),

$$I_D = \frac{10 - V_{on}}{10\ \text{k}\Omega} = \frac{10\ \text{V}}{10\ \text{k}\Omega}\left(1 - \frac{V_{on}}{10}\right) = (1.00\ \text{mA})\left(1 - \frac{V_{on}}{10}\right) \tag{3.32}$$

we see that the value of I_D is approximately 1 mA for $V_{on} \ll 10$ V. Variations in V_{on} have only a small effect on the result. However, the situation would be significantly different if the source voltage were only 1 V for example (see Prob. 3.65).

3.11 MULTIPLE-DIODE CIRCUITS

The load-line technique is applicable only to single-diode circuits, and the mathematical model, or numerical iteration technique, becomes much more complex for circuits with more than one nonlinear element. In fact, the SPICE electronic circuit simulation program referred to throughout this book is designed to provide numerical solutions to just such complex problems. However, we also need to be able to perform hand analysis to predict the operation of multidiode circuits as well as to build our understanding and intuition of diode circuit operation. In this section we discuss the use of the simplified diode models for hand analysis of more complicated diode circuits.

3.11.1 A Two-Diode Circuit

For our first example of multiple diode circuits, consider the circuit containing two diodes in Fig. 3.33, which is redrawn in Fig. 3.34. For simplicity, the positive and negative voltage sources have been replaced with +15 V written at node C and −10 V at node F. We often use this "shorthand" representation to help avoid clutter in circuit diagrams as they become more complex. Such representations should always be interpreted to mean that a voltage source with the given value is connected between the node and the reference terminal for the circuit.

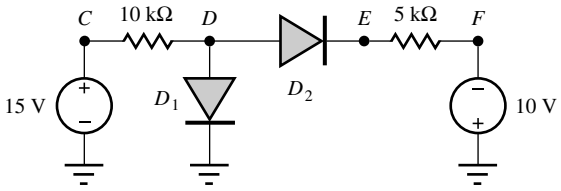


Figure 3.33 Circuit containing two diodes.

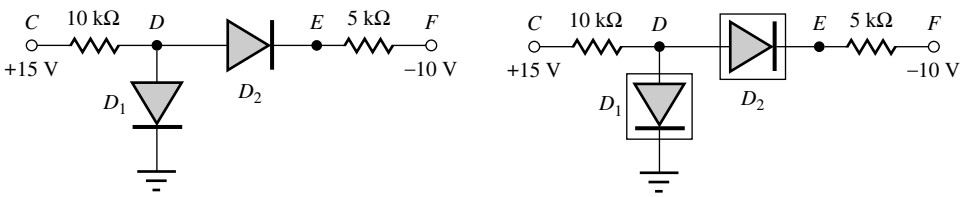


Figure 3.34 (a) Simplified representation of the circuit from Fig. 3.33. (b) Diodes replaced by the ideal diodes.

EXAMPLE 3.8 ANALYSIS OF A CIRCUIT CONTAINING TWO DIODES

As the complexity of diode circuits grows, we must rely on our intuition to eliminate unreasonable solution choices. Intuition is developed by working problems, and here we analyze our first circuit containing more than one diode.

PROBLEM Find the Q-points for both diodes in the circuit in Figs. 3.33 and 3.34.

SOLUTION **Known Information and Given Data:** Circuit topology and element values appear in Fig. 3.33.

Unknowns: (I_{D1}, V_{D1}), (I_{D2}, V_{D2})

Approach: Following the five steps in Sec. 3.10, the ideal diode model was chosen for the analysis, and in Fig. 3.34(b), the circuit is redrawn using this model. With two diodes, there will be four potential piecewise linear models for the circuit corresponding to the four diode states in Table 3.4. We must try to use some intuition to make a choice of states. It appears that the +15-V source will try to force a current in the positive direction through both diodes D_1 and D_2; the −10-V source will also try to force a current through D_2 in the positive direction. A reasonable initial choice for this circuit, therefore, is to assume that both diodes are in the on state.

TABLE 3.4
Possible Diode States for Circuit in Fig. 3.34(b)

D_1	D_2
Off	Off
Off	On
On	On
On	Off

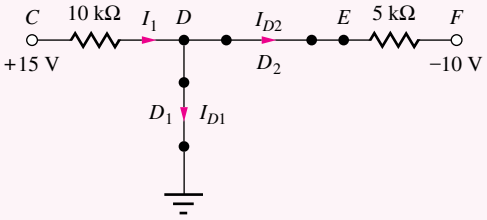


Figure 3.35 Circuit with both diodes assumed to be on.

Assumptions: Use of the ideal diode model is adequate for the analysis

Analysis: The circuit is redrawn in Fig. 3.35 using the piecewise linear models assuming both ideal diodes are in the on state. The currents in the circuit can now be found using a combination of Ohm's law and Kirchhoff's current law. Because the voltage at node D is zero due to the short circuit of ideal diode D_1, the currents I_1 and I_{D2} can be written directly using Ohm's law:

$$I_1 = \frac{(15-0)\text{ V}}{10\text{ k}\Omega} = 1.50\text{ mA} \qquad \text{and} \qquad I_{D2} = \frac{0-(-10)\text{ V}}{5\text{ k}\Omega} = 2.00\text{ mA} \tag{3.33}$$

At node D, $I_1 = I_{D1} + I_{D2}$, so $I_{D1} = 1.50 - 2.00 = -0.50$ mA.

Check of Results: The calculated Q-points are (−0.5 mA, 0 V) and (2.0 mA, 0 V). The result, $I_{D2} > 0$, is consistent with D_2 being on, but $I_{D1} < 0$ is not allowed by the diode. Our assumed state must be incorrect, so we must change our assumptions and try again.

A SECOND ITERATION Because the current in D_2 was valid but that in D_1 was invalid, an appropriate second guess would be D_1 off and D_2 on. Note, however, that there is no guarantee that this choice will in fact be correct. Analysis of the new circuit in Fig. 3.36 proceeds as follows. Because I_{D1} is now

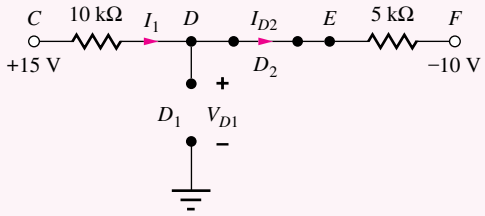


Figure 3.36 Circuit with D_1 off and D_2 on.

assumed to be zero, $I_{D2} = I_1$ and a single-loop equation can be written for I_1:

$$\begin{aligned} 15 - 10{,}000I_1 - 5000I_{D2} - (-10) &= 0 \\ 25 &= 10{,}000I_1 + 5000I_1 \qquad \text{because } I_{D2} = I_1 \\ I_1 &= \frac{25 \text{ V}}{15{,}000\ \Omega} = 1.67 \text{ mA} \end{aligned} \tag{3.34}$$

The voltage across diode D_1 is given by

$$V_{D1} = 15 - 10{,}000I_1 = 15 - 16.7 = -1.67 \text{ V} \tag{3.35}$$

Check of Results: The Q-points of the two diodes are now given by

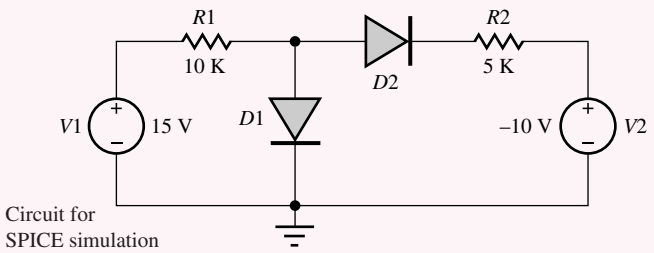
D_1: (0 mA, −1.67 V): off ✔

D_2: (1.67 mA, 0 V): on ✔

Both Q-points are consistent with the assumed states of the diodes, so we have found the correct solution.

Discussion: In the worst situation, we could have to perform four analyses to find the correct answer. As our understanding of diode circuits matures, we should be able to eliminate most of the unfruitful possibilities.

Computer-Aided Analysis: SPICE is always a good avenue to check our analysis. In this circuit, IS defaults to 10 fA. The device parameters and Q-points can be obtained directly from SPICE with the SHOW and SHOWMOD commands, and the results are (−1.23 pA, −1.22 V) and (1.62 mA, 0.667 V). Our hand calculations agree well with these results. The large reverse leakage current in D1 results from a more complex diode model in the author's version of SPICE. The diode voltage of 0.645 V does not significantly affect the current in D2 because the driving voltage in the loop is so high (25 V).



EXERCISE: Find the Q-points for the two diodes in Fig. 3.33 if the value of the 5 kΩ resistor is changed to 10 kΩ.

ANSWERS: (0.50 mA, 0 V); (1.00 mA, 0 V)

EXERCISE: Use SPICE to calculate the Q-points of the diodes in the previous exercise. Use $I_S = 10$ fA.

ANSWERS: (0.439 mA, 0.634 V); (0.998 mA, 0.655 V)

3.11.2 A THREE-DIODE CIRCUIT

Figure 3.37 is a second example of a circuit with several diodes. In the analysis of this circuit, we will use the CVD model for improved accuracy.

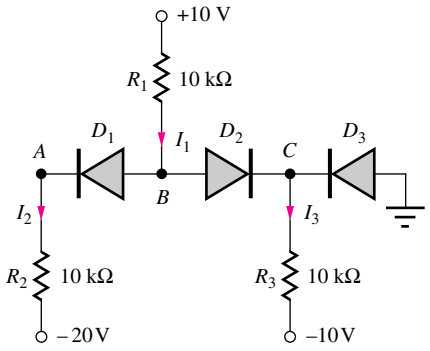


Figure 3.37 Example of a circuit containing three diodes.

EXAMPLE 3.9 ANALYSIS OF A CIRCUIT CONTAINING THREE DIODES

Now we will attempt to find the solution for a three-diode circuit. Our analysis will employ the CVD model.

PROBLEM Find the Q-points for the three diodes in Fig. 3.37. Use the constant voltage drop model for the diodes.

SOLUTION **Known Information and Given Data:** Circuit topology and element values in Fig. 3.37

Unknowns: (I_{D1}, V_{D1}), (I_{D2}, V_{D2}), (I_{D3}, V_{D3})

Approach: With three diodes, there are eight possibilities. For this circuit, it appears that the +10-V supply will tend to forward-bias D_1 and D_2, and the −10-V supply will tend to forward-bias D_2 and D_3. The −20-V supply will also try to forward-bias D_1, so our initial circuit model will assume that all three diodes are on.

Assumptions: Use the constant voltage drop model with $V_{on} = 0.6$ V.

Analysis: The circuit is redrawn using the CVD diode models in Fig. 3.38. Here we skipped the step of physically drawing the circuit with the ideal diode symbols but instead incorporated