5.4.9

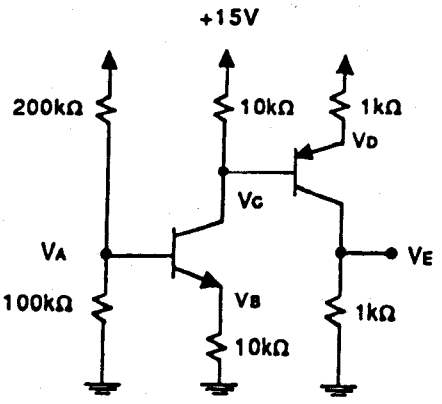

Fig. Q5.4.9

For the circuit shown, find the labelled node voltages when β is (a) ∞ and (b) 100.

SECTION 5.5: BIASING IN BJT AMPLIFIER CIRCUITS

D

5.5.1 Consider the one-supply bias scheme in Fig. 5.44 of the Text. For $R_B = R_E$, above what value of β is I_E constant to within 1%?

D

5.5.2 Using the rule ($V_{BB} = V_{CB} = V_{CC}/3$) and $R_B = \beta R_E/10$, provide a design for the circuit of Fig. 5.44 in the Text, in which $V_{CC} = 12$ V and $I_E = 100$ mA. For the BJT, $\beta = 50$ and $V_{BE} = 0.7$ V. Find R_E, R_1, R_2, and R_C to the nearest single significant digit. What values of I_E and V_{CE} does your design provide?

D

5.5.3 For the bias arrangement shown in Fig. 5.45 in the Text, using ±5-V supplies, a design is required for which I_E is fixed to within 5% and a ±1-V signal output range is available, for $\beta \geq 20$ and $R_C = 1$ kΩ.

D

5.5.4 A design is required of the feedback-bias scheme shown in Fig. 5.46 in the Text which will maintain $V_{CB} \geq 0.5$ V for $\beta \leq 200$, $V_{CC} = 5$ V, and $R_C = 3.6$ kΩ, with $V_{BE} = 0.7$ V. For $\beta \geq 50$, what is the range of I_E and V_{CB} you achieve?

D

5.5.5 In the situation described in P5.5.4 above, a designer, faced with the possibility of β being uncontrollably high, chooses to shunt the base–emitter junction with resistor R_β. What is its value for $\beta_{eq} \leq 200$? Find R_B to meet the other specifications. What ranges of I_E and V_{CB} result for $\beta \geq 50$?

D

5.5.6 Repeat P5.5.5 for $\beta_{eq} \leq 100$.

5.5.7 For a BJT operating with the constant-current-source bias shown in Fig. 5.47a in the Text, the manufacturer specifies β to lie in a range from 40 to 200. The bias–current source operates at 1 mA for voltages at its upper end in the range ±5 V. For $V_{BE} = 0.70$ V, what is the largest value of R_B that can be tolerated? For this value of R_B, what is the range of dc voltages to be found at the base? For $R_B = 100\, r_\pi$ at the lowest value of β, what range of base voltages results?

5.5.8 A current source using the current–mirror circuit shown in Fig. 5.47b of the Text operates from ±5-V supplies. Select a value of R for $I = 1$ mA. Over what range of voltages V does the current remain essentially constant? Use $V_{BE} = 0.7$ V and assume that linear operation is possible until V_{BC} reaches the edge of conduction at 0.5 V.

SECTION 5.6: SMALL-SIGNAL OPERATION AND MODELS

5.6.1 What values of transconductance apply to BJTs biased at 1 μA, 100 μA, 1 mA, and 100 mA?

5.6.2 For the current levels listed in P5.6.1, what equivalent small-signal input resistances model operation as seen at the emitter? At the base, for $\beta = 100$?

D

5.6.3 In the design of a particular amplifier, a young engineer considers the use of bias currents I_E, from 0.1 to 10 mA. Unfortunately, the application requires that the dc voltage across the load resistor be held constant to provide correct biasing of a connected amplifier stage. Find the range of gains she can expect from this gain stage.

5.6.4 A particular amplifier utilizes a BJT biased at $I_E = 100$ μA and having $\beta = 150$ to drive a load of 10 kΩ. For the emitter grounded for signals, what is the input resistance at the base, and the voltage gain from base to collector?

5.6.5

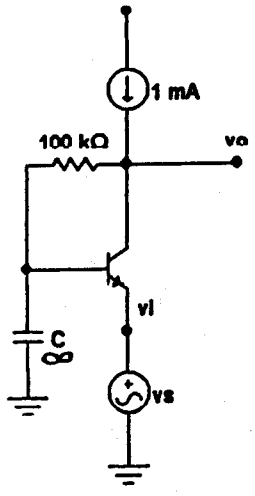

Fig. Q5.6.5

What is the voltage gain v_o/v_i of the amplifier shown? Note that capacitor C grounds the base of the amplifier for ac signals. Note that the gain is essentially independent of β (although the dc voltage V_O is not). What is the input resistance "seen" by the source v_s? What does the gain v_O/v_s, become if the source resistance is 75 Ω?

5.6.6 A BJT having a particular β and bias current has a resistor r_E added in series with the emitter. Use the T model shown in Fig. 5.52a of the Text to create a simplified hybrid-π model for the overall amplifier (including r_E). For this model find g'_m and r'_π in terms of r_E, g_m, and r_π of the basic BJT. What is the equivalent input resistance (r'_π) and transconductance (g'_m) of the modified amplifier, for $\beta = 100$, $I_C = 1$ mA, and $r_E = 3r_e$?

L

5.6.7 An appropriate choice of one of the BJT models of Figs. 5.51 and 5.52 of the Text often makes the solution of a particular problem somewhat easier. To illustrate, find the gain υ_o/υ_s for each of the circuits below using the model(s) suggested as Π_{gm}, Π_β, T_{gm}, and T_α, corresponding to Figs. 5.51a, 5.51b, 5.52a, and 5.52b, respectively. In each case, assume (for simplicity) that I_E = 1 mA, r_e = 25 Ω, r_π = 2.5 kΩ, $\beta \approx 100$, α = 0.99 and g_m = 40 mA/V. (Note that biasing is generally not shown in detail.)

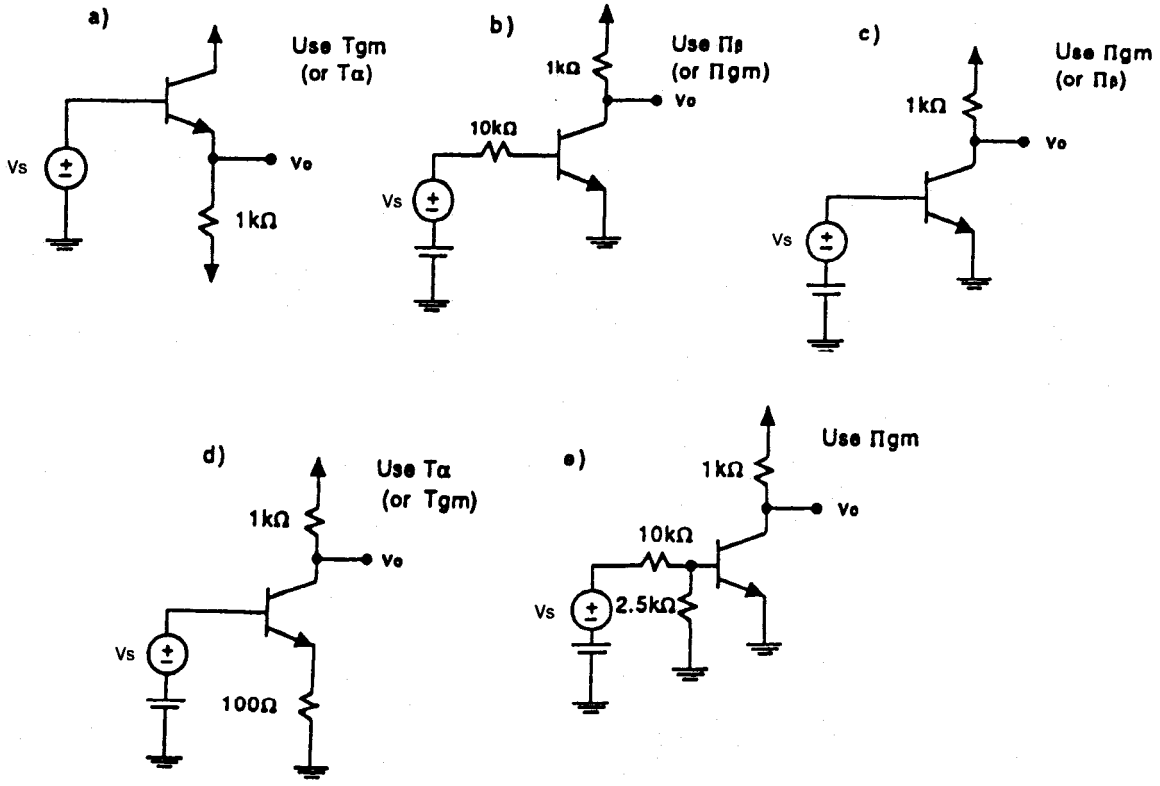

Fig. Q5.6.7

5.6.8

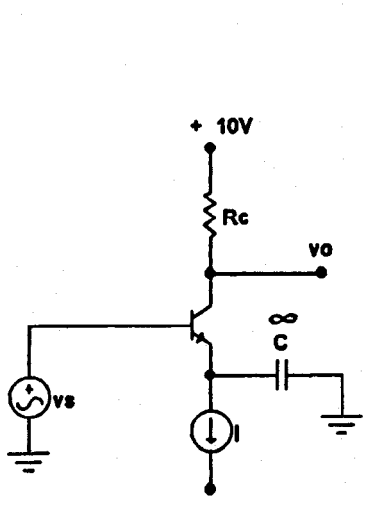

Fig. Q5.6.8

In the circuit shown, I = 1 mA, R_C = 7.5 kΩ, and α = 0.99. What is the voltage gain υ_o/υ_s? What is the largest sine-wave output for which the transistor remains in the active region? What is the peak value of the corresponding input?

5.7.6

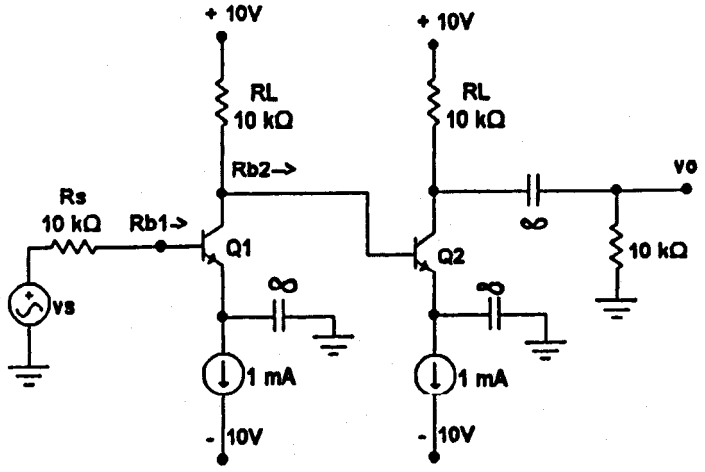

Fig. Q5.7.6

For $\beta = 150$, find $\frac{\upsilon_o}{\upsilon_{b2}}$, R_{b2}, $\frac{\upsilon_{b2}}{\upsilon_{b1}}$, R_{b1}, $\frac{\upsilon_{b1}}{\upsilon_s}$, and $\frac{\upsilon_o}{\upsilon_s}$.

D

5.7.7 Provide a design using the basic circuit in Fig. P5.136 on page 535 of the Text in which R_L (shown as 250 Ω) is chosen so R_{in} is 10 kΩ for $\beta = 50$. What is its voltage gain from υ_s, for the load reduced (from 20 kΩ) to 2 kΩ?

5.7.8 A common-base amplifier, biased at an emitter current of 3 mA, employs an unbypassed base resistor R_B = 2 kΩ, with R_C = 3 kΩ, R_E = 3 kΩ, and R_L = 1 kΩ. For $\beta \geq 150$, what range of input resistances result? What range of voltage gains result from a 100-Ω source? What does the input resistance and gain become if R_B = 0 Ω? Note how much simplier the design now becomes!

5.7.9

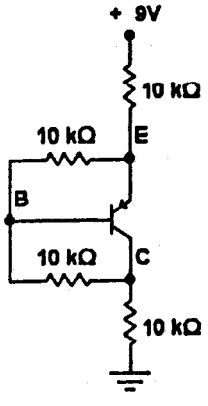

Fig. Q5.7.9

For the circuit shown, evaluate V_E, V_B, V_C, and I_C for $\beta = 100$. Show capacitor-coupled connections to a 0-Ω source, a 10-kΩ load, and ground to achieve voltage gains of:

(a) ≈ +1 V/V.

(b) −1 V/V. (*Hint*: Use an extra resistor.)

(c) −K, where K is large.

(d) +K, where K is large.

5.7.10 For each of the designs created in P5.7.9 above, calculate the exact gains assuming $\beta = 100$, $V_A = \infty$.

5.7.11 An emitter follower biassed at 0.1 mA employs a 100-kΩ base resistor and a 50-kΩ emitter resistor. The BJT has $\beta = 50$ and $V_A = 100$ V. When driven by a capacitor-coupled 20-kΩ source and driving a 2-kΩ capacitor-coupled load, what is the voltage gain that results?

5.7.12

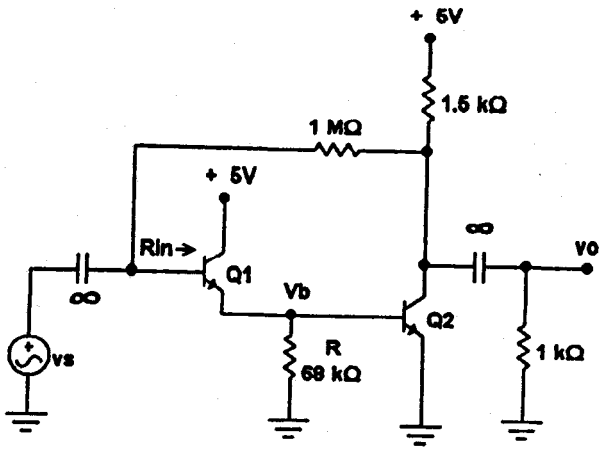

Fig. Q5.7.12

The circuit shown is a combination of a follower and common-emitter amplifier (it is called a *CC–CE* cascade), which has the advantage of a simple biasing structure and relatively high input resistance. For $\beta = 100$ and $V_A = 100$ V, find υ_o/υ_s and R_{in} for the circuit (a) as shown and (b) with R removed. [*Hint*: To calculate R_{in}, realize that the 1-MΩ resistor R_f has an important effect since at its right-hand side the voltage is υ_o/υ_s times that at its left. Thus for a test-voltage input υ_x at the left, the input current is $i_x = \upsilon_x\,(1 - \upsilon_o/\upsilon_s)/R_f$. This is an example of the Miller-effect idea introduced earlier in P2.2.8 in this book.]

SECTION 5.8: THE BJT INTERNAL CAPACITANCES AND HIGH-FREQUENCY MODEL

5.8.1 Consider the *npn* transistor whose detailed physical parameters are as specified in P5.2 of the Text, when operating at $I_C = 1$ mA. For $W = 1$ μm and 5 μm, calculate the stored base charge, the forward base transit time, and the emitter diffusion capacitance.

5.8.2 For the BJT specified in P5.2 of the Text having a base width of 1 μm, calculate C_{je} and C_μ using Equations 5.155 and 5.156 with Equations 3.56 and 3.48. Use a grading coefficient of 0.4 for the CBJ, which is 10 times the area of the EBJ and reverse biased by 2.0 V. Note that the permittivity of silicon is $\varepsilon_S = 1.04 \times 10^{-12}$ F/cm. Using the result for the emitter diffusion capacitance at 1 mA found in P5.8.1 above, calculate C_π and f_T.

5.8.3 A particular BJT for which f_T is 10 GHz at $I_C = 10$ mA has f_T reduce to 7 GHz at $I_C = 1$ mA. Estimate values for $C_\mu + C_{je}$, and C_{de} at 10 mA and at 10 μA. What is f_T at 10 μA?

5.8.4 A need arises to adapt the BJT described in Exercise 5.48 of the Text to a new application in which operation is desired at $I_C = 4$ mA, but with the base–emitter voltage unchanged. A decision is made to use the same process but to double the perimeter of the square base area. What do the values of τ_F, C_{je0}, $C_{\mu 0}$, V_{0e}, m_{CBJ}, C_{de}, C_{je}, C_π, C_μ, and f_T become for operation at 4 mA? What f_T results at $I_C = 1$ mA?

5.8.5 The 500-MHz transistor in Exercise 5.49 of the Text is being considered for operation at $i_C = 10$ μA and even $i_C = 1$ μA. What unity gain frequencies would likely apply? If it is possible to reduce each of the sides of the square base used in this device structure by a factor of 10, what values of f_T would you expect at 10 μA and 1 μA?

5.8.6 For a particular BJT transistor, for which $C_\mu = 0.5$ pF, operating at 2 mA, with $\beta = 200$ and $f_\beta = 12.7$ MHz, find the corresponding values of unity-gain frequency f_T and C_π. (*Hint*: See Equation 5.163 on page 489 of the Text.) If the bias current is increased to 10 mA, what values of f_β and C_π apply? For the usual situation described, for what range of currents is f_T maintained at the value estimated, as defined by the situation in which $C_\pi \geq C_\mu$?

SECTION 5.9: FREQUENCY RESPONSE OF THE COMMON-EMITTER AMPLIFIER

5.9.1 For a particular BJT *CE* amplifier use the circuit of Fig. 5.71a of the Text, with the current source I replaced by resistor R_E, $V_E = 0$, $R_s = 10$ kΩ, $R_B = 40$ kΩ, $R_E = 8.2$ kΩ, $R_C = 9.1$ kΩ, $R_L = 10$ kΩ, and $V_{CC} = 5$ V. Under these conditions, I_E is 0.15 mA, at which $\beta = 150$, $r_o = 500$ kΩ, $f_T = 1$ GHz and $C_\mu = 0.3$ pF. Estimate the midband gain and the upper 3-dB cutoff frequency assuming large bypass and coupling capacitors.

5.9.2 For the situation described in P5.9.1, with all coupling and bypass capacitors appropriately large, an additional resistor $R = 350$ Ω is included in series with C_E. What new values of midband gain and upper 3-dB frequency result?

5.9.3 An amplifier having a gain of −50 V/V and dominant poles at 50 Hz and 50 MHz is supplied by a negative pulse of 50-mV amplitude and 50-μs duration. Completely characterize the output pulse produced. (*Hint*: Consult Appendix D, pages D-12 to D-15 of the Text.)

5.9.4 For a particular BJT CE amplifier use the circuit of Fig. 5.71 of the Text, where the current source I is replaced by resistor R_E, $V_{EE} = 0$, $R_S = 10$ kΩ, $R_B = 40$ kΩ, $R_E = 8.2$ kΩ, $R_C = 9.1$ kΩ, $R_L = R_{sig} = 10$ kΩ, and $V_{CC} = 5$ V. Under these conditions, I_E is 0.15 mA, at which $\beta = 150$ and $r_o = 500$ kΩ. Coupling capacitors of value $C_{C1} = C_{C2} = 1$ μF and a bypass capacitor $C_E = 10$ μF are used. Calculate the three associated pole and zero frequencies, and estimate the gain and lower 3-dB frequency.

5.9.5 For the situation described in P5.9.4, find suitable values for C_{C1}, C_{C2}, and C_E so that the dominant low-frequency pole is at 20 Hz, another pole is at 2 Hz, and the third pole and zero coincide.

5.9.6 For the situation described in P5.9.4, an additional resistor of 350 Ω is included in series with C_E. Calculate the midband gain and the associated pole and zero frequencies and estimate the lower 3-dB frequency.

5.9.7 For a particular implementation of the CE amplifier shown in Fig. 5.71 on page 491 of the Text, $I = 2$ mA, $R_{sig} = 10$ kΩ, $R_B = 20$ kΩ, $R_L = 5$ kΩ, $\beta = 150$, and $V_A = 150$ V. Find the midband gain A_M.

5.9.8 Various BJT amplifiers are partially specified as follows:

(a) direct-coupled with BW = 100 kHz;

(b) capacitor-coupled with 3-dB frequencies at 1 kHz and 20 kHz;

(c) lower 3-dB frequency at 100 Hz, and an f_H/f_L ratio of 500;

(d) f_H of 10 MHz and a BW/f_C ratio of 1.6, where $f_C = (f_H + f_L)/2$.

For each, list estimates of the upper and lower 3-dB frequencies and corresponding BW.

5.9.9 In the amplifier specified in P5.9.7, a BJT is used for which $r_x = 50$ Ω, $C_\mu = 0.9$ pF, and $f_T = 900$ MHz. Find the Miller multiplier, the value of the Miller-multiplied capacitance, C_{eq}, C_{in}, the resistance seen by C_{in}, and the upper 3-dB frequency.

5.9.10 Repeat Example 5.18 on page 496 of the Text, using the same transistor, but with all external resistors reduced by a factor of 2, and the bias current doubled. Compare A_M and f_H in the two designs.

5.9.11 Consider signal-coupling and bypass aspects of the CE amplifier presented in Fig. 5.71 on page 491 of the Text, and then in Fig. 5.73 on page 499 of the Text. In a particular design, using the resistor values and

SECTION 4.8: THE MOSFET INTERNAL CAPACITANCES AND HIGH-FREQUENCY MODEL

L

4.8.1 The gate-to-channel capacitance of a MOS transistor is often used as an explicit capacitor in MOS circuits, in which case the gate and source are joined to form the second electrode. Use the data provided in Table 4.1 on page 261 of the Text to calculate the dimensions of a square capacitor of 1 pF for the range of technologies cited, where oxide thickness ranges from 20 nm to 100 nm. In a 0.8-μm feature-size technology, in which the minimum-size NMOS digital device has L = 1.2 μm and W = 2.4 μm, to how many such transistors do these capacitor areas correspond?

4.8.2 For the 1-μm technology whose parameters are provided in Example 4.36 on page 322 of the Text, calculate values of C_{ov}, C_{gs}, G_{gd}, C_{sb}, and C_{db} for transistors operating in saturation at $|V_{SB}| = |V_{DB}| = 1$ V for which: (a) L = 2.4 μm, W = 100 μm and (b) L = 24 μm, W = 10 μm. (*Hint*: Recall in calculating C_{sb} and C_{db} that the values at C_{sb0} and C_{db0} provided are approximately proportional to source and drain areas, respectively and correspondingly to device widths.)

4.8.3 For each of the transistors in P4.8.2 above, operating at I_D = 100 μA with k_n' = 100 μ/V², calculate f_T. What does f_T become in each case if the operating current is reduced to 10 μA?

4.8.4 For the transistor evaluated in Examples 4.37 and 4.36 on pages 325 and 322, respectively, of the Text, what is the gate input impedance of the NMOS device with output shorted when operating at f_T. What does the input impedance become at $f_T/10$ if the FET operates there with a voltage gain of −2 V/V?

L

4.8.5 An n-channel enhancement MOSFET, for which C_{ox} – 1.0 fF/μm², μ_n – 0.05 m²/Vs, L = 3 μm, W = 27 μm, and V_t = 0.5 V, operates with $\upsilon_{GS} = \upsilon_{DS}$ = 2.5 V, and the source grounded. The gate overlap is about 0.3 μm. Estimate C_{gs}, C_{gd} and the unity-gain frequency f_T which corresponds.

4.8.6 Find values of the FET unity-gain frequency f_T (for operation in the grounded-source (CS) configuration) for:

(a) A JFET for which I_{DSS} = 4 mA, V_p = −2 V, C_{gs} = 2 pF, and C_{gd} = 0.2 pF, operating at 1 mA.

(b) A MOSFET with gate-to-channel capacitance of 0.15 pF, overlap capacitance of 20 fF, gate-to-substrate capacitance of 0.1 pF, having V_t = 1 V, and $k'(W/L)$ = 200 μA/V², operating at 200 μA.

(c) A GaAs MESFET for which g_m = 10 mA/V at relatively high bias currents with C_{gs} = 0.15 pF and C_{gd} = 15 fF.

(*Hint*: See the development associated with Equation 4.118 on page 324 of the Text.)

4.8.7 A particular FET transistor is to be operated in one of two grounded-source topologies for which the gain from gate to drain is either −1 or −100 V/V. Its C_{gs} = 200 fF, C_{db} = 100 fF, C_{gd} = 20 fF. Find the equivalent capacitances to ground at the gate and at the drain of each circuit.

SECTION 4.9: FREQUENCY RESPONSE OF THE CS AMPLIFIER

D

4.9.1 A particular FET operates in a common-source circuit environment in which g_m = 1 mA/V, r_o = 50 kΩ, C_{gs} = 1 pF, C_{gd} = 0.5 pF, R_s = 100 kΩ, R_{in} = 1 MΩ, R_D = 10 kΩ, and R_L = 30 kΩ. Find the equivalent input capacitance at the gate, output capacitance at the drain, two poles, and an estimate of the upper 3-dB frequency. What is the highest frequency to which f_H can be raised by lowering R_s? What is the value of R_s which reduces f_H to 90% of that frequency?

4.9.2 For the situation described in P4.9.1, find exact values of the associated poles and zero, and an estimate of f_H. To what do all these frequencies change if the signal-source resistance R_s is reduced to 1 kΩ?

C

4.9.3 A high-performance n-channel MOS device for which $V_t = 1$ V and $f_T = 1$ GHz (see Equation 4.118 of the Text) operates at 1 mA and $V_{GS} = 2$ V in a common-source amplifier stage for which the gain is −3 V/V. If C_{gd} is known to be $\leq 0.2C_{gs} \approx C_{db}$, what is the equivalent input capacitance? If driven from a similar amplifier whose output impedance is approximately $(3/g_m) \parallel 4C_{db}$, what 3-dB frequency would you estimate?

4.9.4 A MOSFET amplifier using the topology of Fig. 4.49 of the Text with an additional R_3 in parallel with C_S, employing $R_{sig} = 100$ kΩ, $R_G = 10$ MΩ ∥ 22 MΩ, $R_S = R_D = 10$ kΩ, $R_L = 20$ kΩ, $C_{C1} = 0.01$ μF, $C_{C2} = 0.1$ μF, and $C_S = 1$ μF, operates with $g_m = 2$ mA/V. Find the midband gain, and 3 poles and a zero at low frequencies.

4.9.5 For the situation described in P4.9.4, it is desired to have a single dominant pole at 10 Hz or less and have two coincident ones at about 1 Hz. What values of coupling and bypass capacitors should be used which minimize the total capacitance? Specify the capacitors to 1 significant digit. What poles and zero actually result?

CDL

4.9.6 The circuit and situation described in P4.9.4 is modified by the addition of a resistor r_S in series with C_S. Find expressions for the associated zero and pole, and the gain which correspond to Equation 4.139. For gain reduced from its maximum value by a factor of 2 using V_S, what do the new pole and zero associated with C_S become?

4.9.7 Consider the capactively coupled CS amplifier of Fig. 4.49 on page 327 of the Text, with $R_{sig} = 1$ MΩ, $R_G = 10$ MΩ, $R_D = 10$ kΩ, $R_L = 10$ kΩ, with $r_o = 100$ kΩ and $g_m = 1$ mA/V. Assuming large coupling and bypass capacitors, find A_M.

4.9.8 Repeat P4.9.7 for a MOS device operating at 100 μA for which $V_t = 0.5$ V, $k'(W/L) = 500$ μA/V², and $V_A = 15$ V. Find A_M.

4.9.9 For the amplifiers whose upper and lower 3-dB frequencies, f_H and f_L, are listed below, find the value of the bandwidth, BW. In which cases is the usual approximation reasonably valid:

(a) 20 kHz, 20 Hz,

(b) 1 MHz, 50 kHz,

(c) 1600 kHz, 500 kHz,

(d) 3 kHz, 300 Hz,

(e) 10.9 MHz, 10.5 MHz.

4.9.10 A MOS transistor operating in a CS configuration has $C_{gs} = 0.5$ pF, $C_{gd} = 0.1$ pF, $g_m = 0.9$ mA/V, $r_o = 100$ kΩ, with $R_D = 12$ kΩ, $R_L = 12$ kΩ. It is driven from a 12-kΩ source, capacitor-coupled to a 10-MΩ gate-bias resistor. What is the midband gain? What is the Miller multiplier that applies? What is the value of the Miller-multiplied equivalent capacitance? What is the value of C_{in}? What is the value of the driving-source resistance? What is the corresponding value of f_H?

4.9.11 A young designer, realizing that the low-frequency input impedance of a CS amplifier is very high, arranges to drive the CS amplifier described in P4.9.10 from a source for which $R_{sig} = 1$ MΩ. By what factor does the resulting value of f_H change? (Note that to answer this question, you need not do a great deal of work!)