ECE321 Electronics I
Fall 2006

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Lecture 4
5th October, 2006

Operational Amplifiers (Real)

2.7 DC Imperfections
2.8 Integration & Differentiation
2.9 SPICE

2

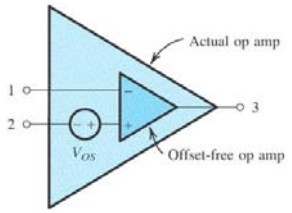

Figure 2.28 Circuit model for an op amp with input offset voltage V_{OS}.

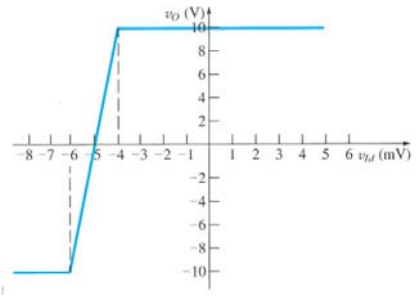

Figure E2.23 Transfer characteristic of an op amp with V_{OS} = 5 mV.

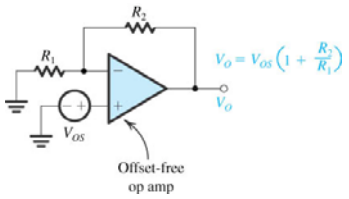

Figure 2.29 Evaluating the output dc offset voltage due to V_{OS} in a closed-loop amplifier.

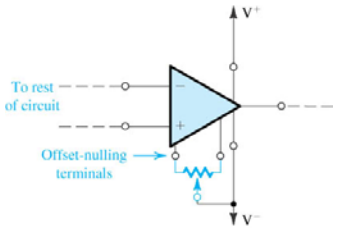

Figure 2.30 The output dc offset voltage of an op amp can be trimmed to zero by connecting a potentiometer to the two offset-nulling terminals. The wiper of the potentiometer is connected to the negative supply of the op amp.

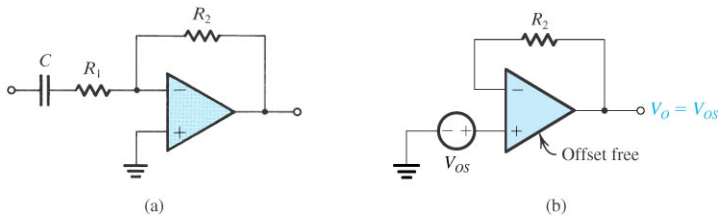

Figure 2.31 **(a)** A capacitively coupled inverting amplifier, and **(b)** the equivalent circuit for determining its dc output offset voltage V_O.

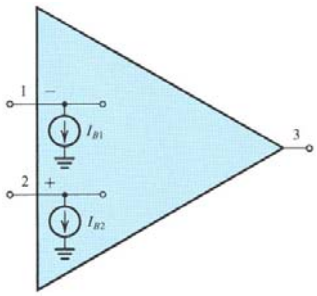

Figure 2.32 The op-amp input bias currents represented by two current sources I_{B1} and I_{B2}.

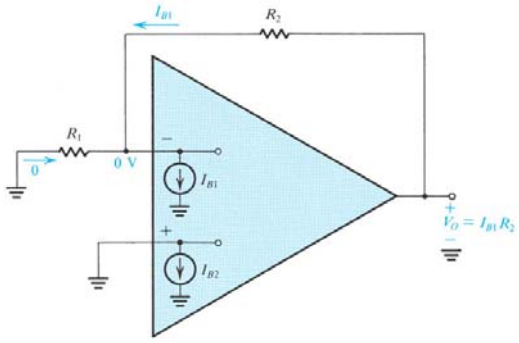

Figure 2.33 Analysis of the closed-loop amplifier, taking into account the input bias currents.

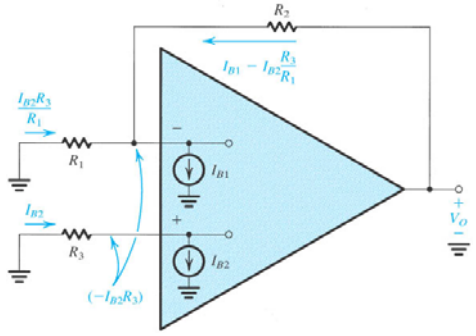

Figure 2.34 Reducing the effect of the input bias currents by introducing a resistor R_3.

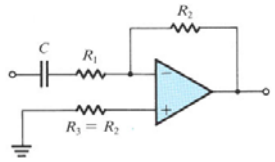

Figure 2.35 In an ac-coupled amplifier the dc resistance seen by the inverting terminal is R_2; hence R_3 is chosen equal to R_2.

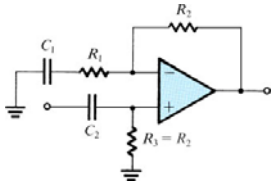

Figure 2.36 Illustrating the need for a continuous dc path for each of the op-amp input terminals. Specifically, note that the amplifier will *not* work without resistor R_3.

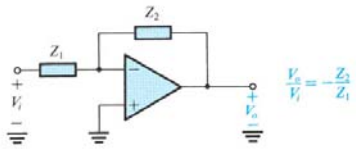

Figure 2.37 The inverting configuration with general impedances in the feedback and the feed-in paths.

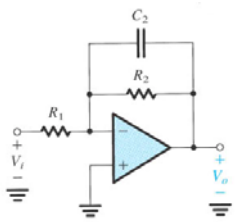

Figure 2.38 Circuit for Example 2.6.

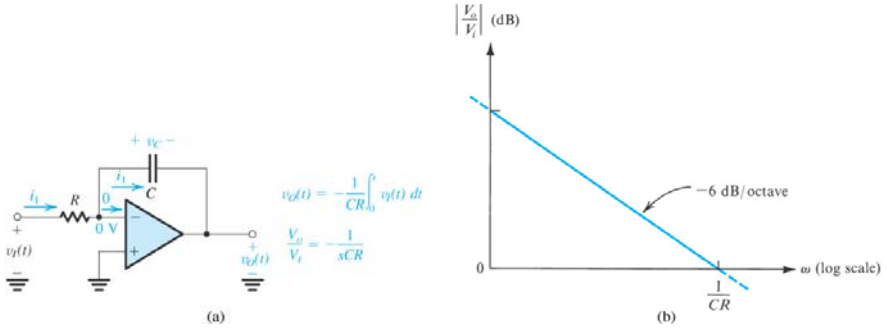

Figure 2.39 **(a)** The Miller or inverting integrator. **(b)** Frequency response of the integrator.

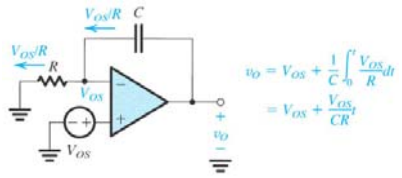

Figure 2.40 Determining the effect of the op-amp input offset voltage V_{OS} on the Miller integrator circuit. Note that since the output rises with time, the op amp eventually saturates.

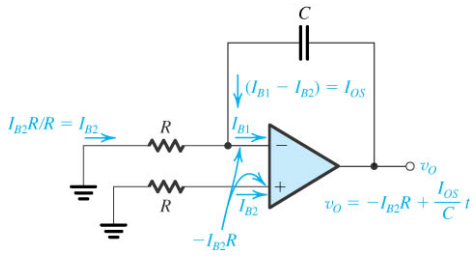

Figure 2.41 Effect of the op-amp input bias and offset currents on the performance of the Miller integrator circuit.

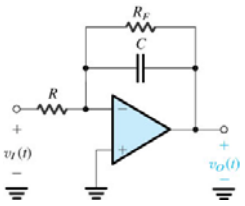

Figure 2.42 The Miller integrator with a large resistance R_F connected in parallel with C in order to provide negative feedback and hence finite gain at dc.

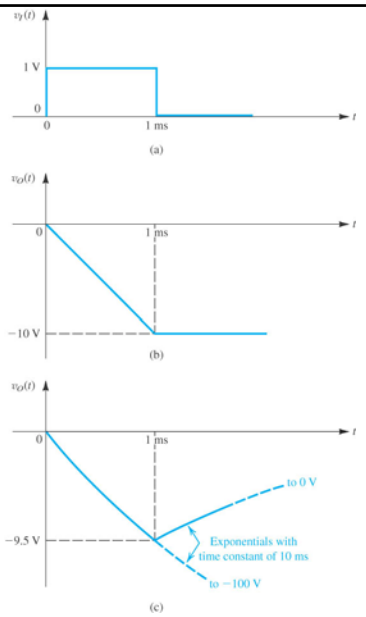

Figure 2.43 Waveforms for Example 2.7: **(a)** Input pulse. **(b)** Output linear ramp of ideal integrator with time constant of 0.1 ms. **(c)** Output exponential ramp with resistor R_F connected across integrator capacitor.

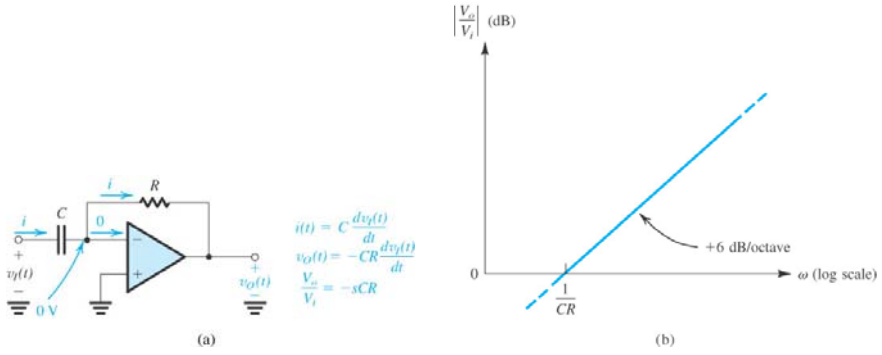

Figure 2.44 **(a)** A differentiator. **(b)** Frequency response of a differentiator with a time-constant *CR*.

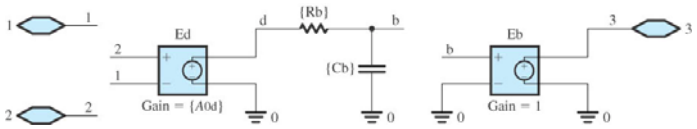

Figure 2.45 A linear macromodel used to model the finite gain and bandwidth of an internally compensated op amp.

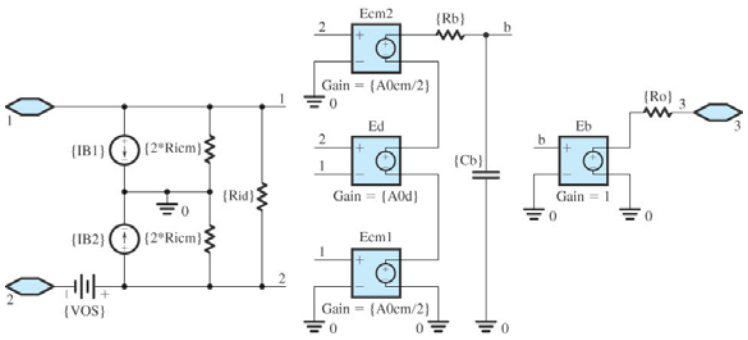

Figure 2.46 A comprehensive linear macromodel of an internally compensated op amp.

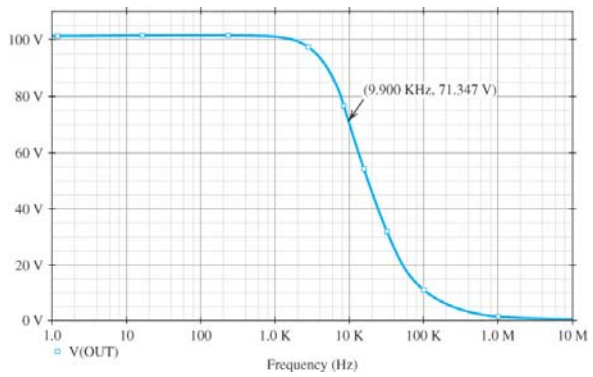

Figure 2.47 Frequency response of the closed-loop amplifier in Example 2.8.

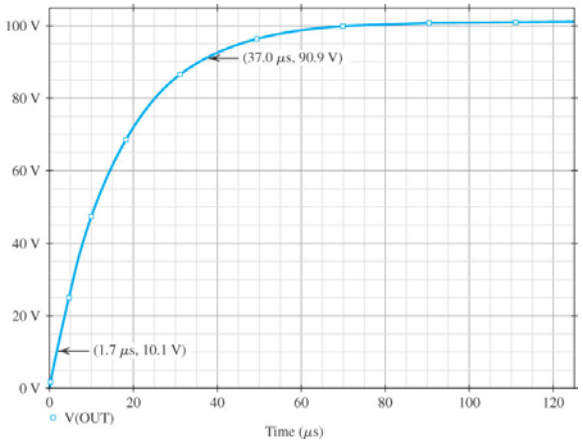

Figure 2.48 Step response of the closed-loop amplifier in Example 2.8.

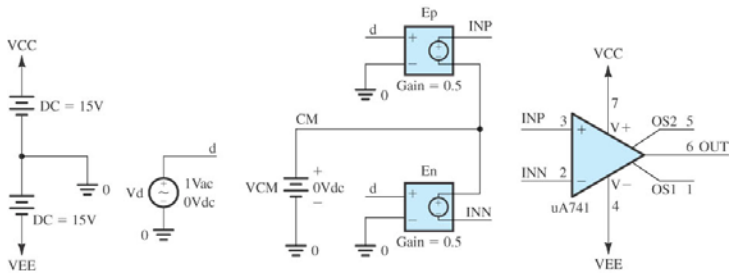

Figure 2.49 Simulating the frequency response of the μA741 op-amp in Example 2.9.

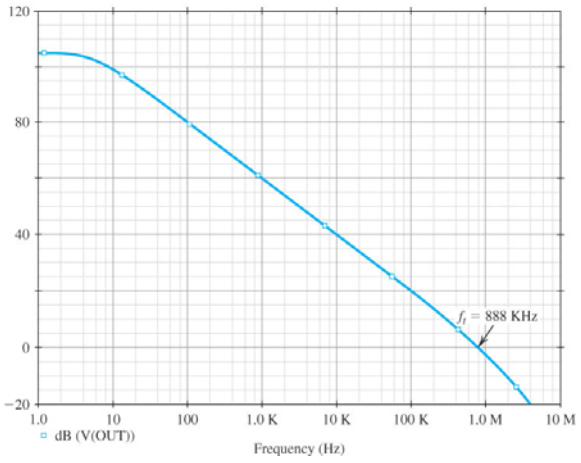

Figure 2.50 Frequency response of the μA741 op amp in Example 2.9.

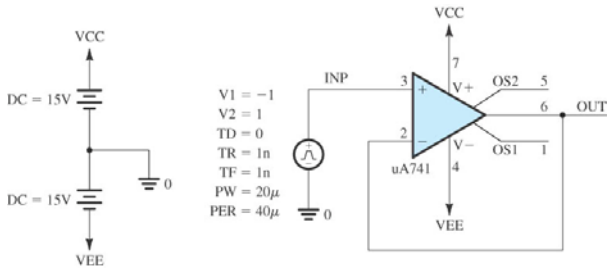

Figure 2.51 Circuit for determining the slew rate of the μA741 op amp in Example 2.9.

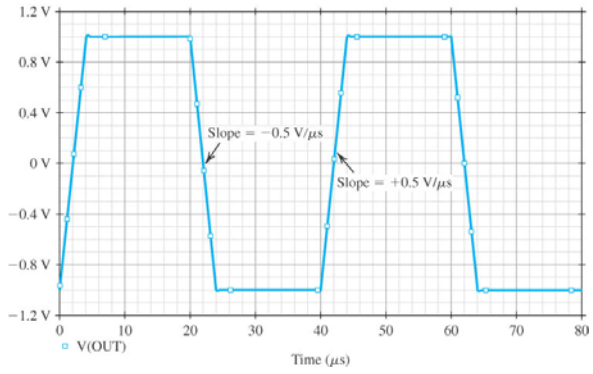

Figure 2.52 Square-wave response of the μA741 op amp connected in the unity-gain configuration shown in Fig. 2.51.