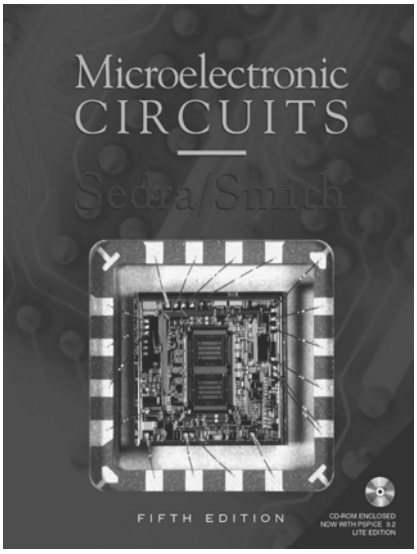
ECE321 Electronics I
Fall 2006

Professor James E. Morris

Lecture 1
25th September, 2006



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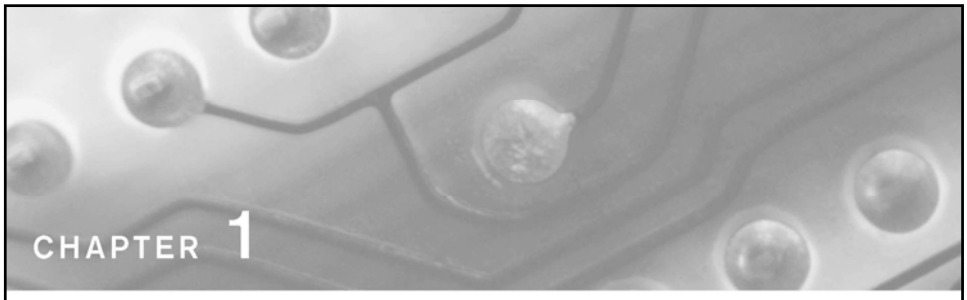

Introduction to Electronics

1.1 Signals / 1.2 Spectrum / 1.3 Analog & Digital

1.4 Amplifiers / 1.5 Amplifier Models

1.6 Amplifier Frequency Response

1.7 Logic Inverters / (1.8 SPICE)

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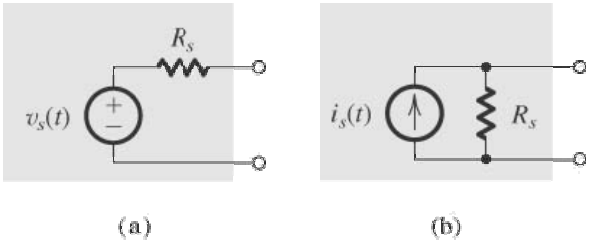

Figure 1.1 Two alternative representations of a signal source: **(a)** the Thévenin form, and **(b)** the Norton form.

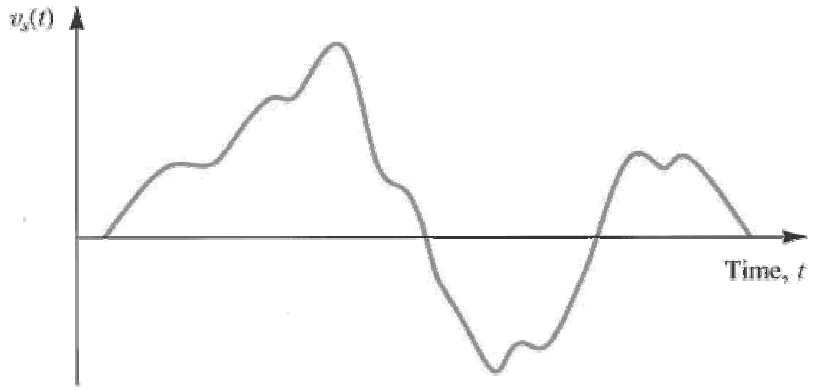

Figure 1.2 An arbitrary voltage signal $v_s(t)$.

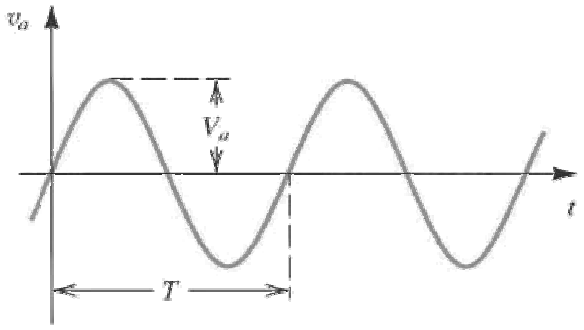

Figure 1.3 Sine-wave voltage signal of amplitude V_a and frequency $f = 1/T$ Hz. The angular frequency $\omega = 2\pi f$ rad/s.

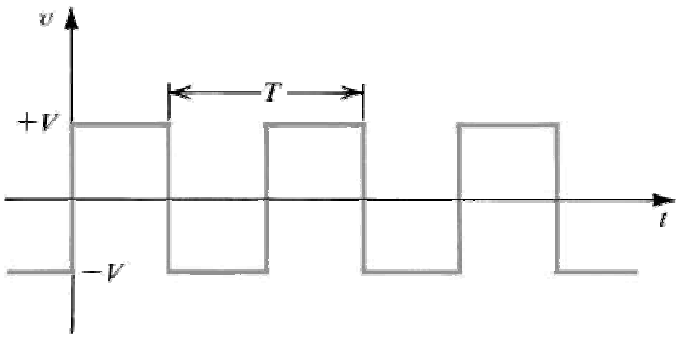

Figure 1.4 A symmetrical square-wave signal of amplitude V.

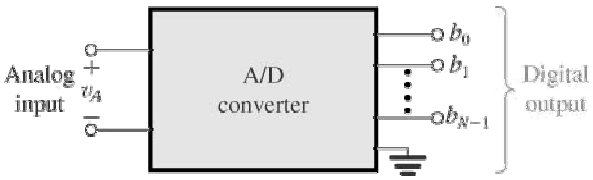

Figure 1.9 Block-diagram representation of the analog-to-digital converter (ADC).

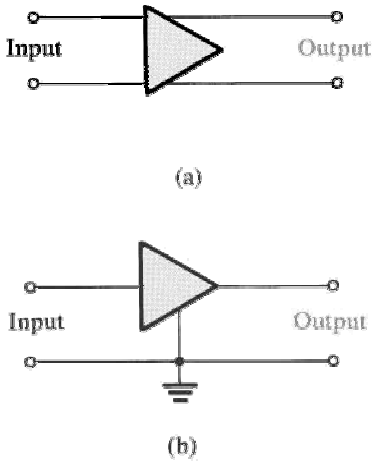

Figure 1.10 **(a)** Circuit symbol for amplifier. **(b)** An amplifier with a common terminal (ground) between the input and output ports.

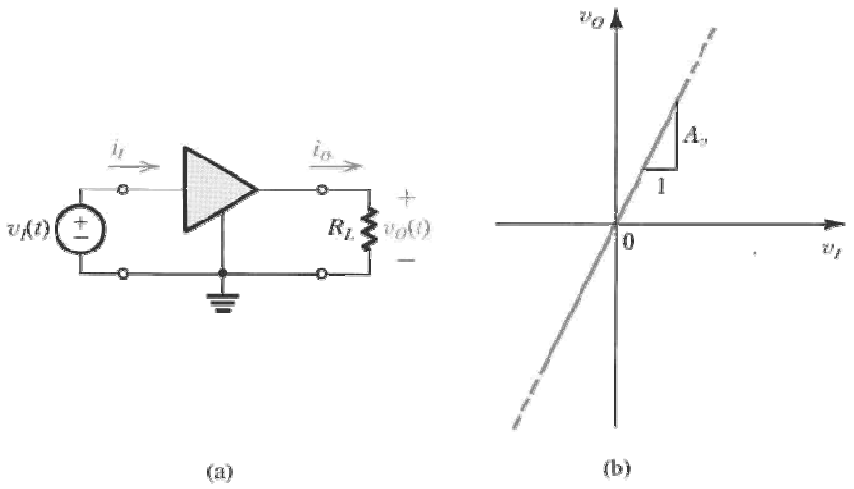

Figure 1.11 **(a)** A voltage amplifier fed with a signal $v_I(t)$ and connected to a load resistance R_L. **(b)** Transfer characteristic of a linear voltage amplifier with voltage gain A_v.

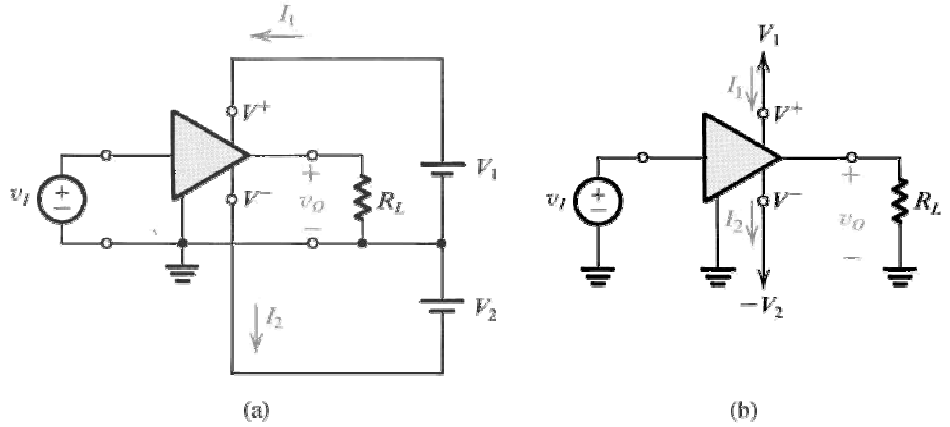

Figure 1.12 An amplifier that requires two dc supplies (shown as batteries) for operation.

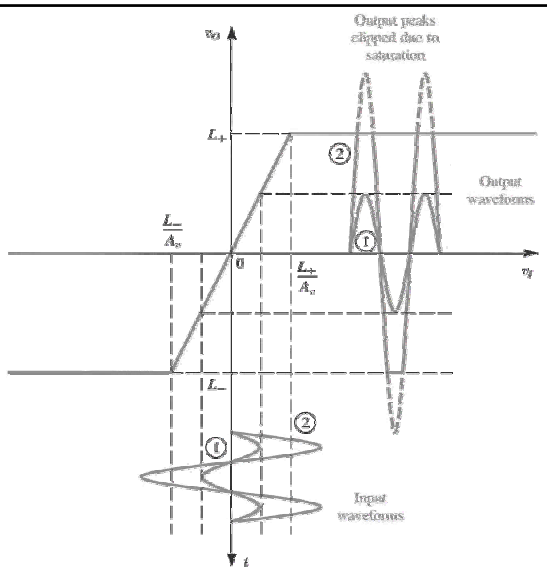

Figure 1.13 An amplifier transfer characteristic that is linear except for output saturation.

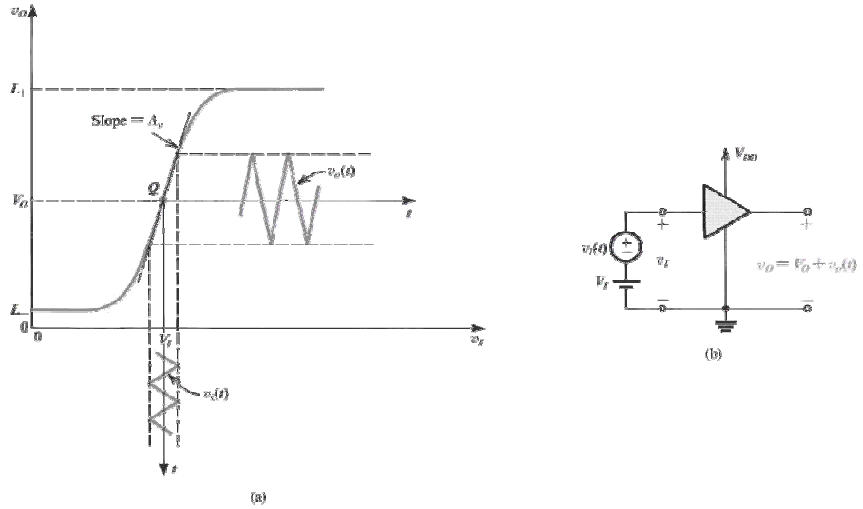

Figure 1.14 (a) An amplifier transfer characteristic that shows considerable nonlinearity. **(b)** To obtain linear operation the amplifier is biased as shown, and the signal amplitude is kept small. Observe that this amplifier is operated from a single power supply, V_{DD}.

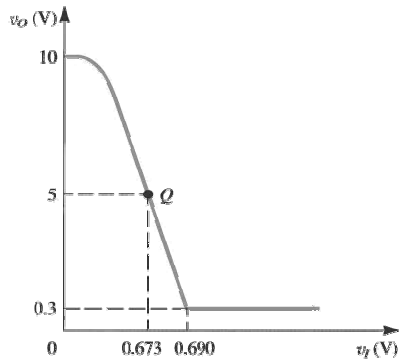

Figure 1.15 A sketch of the transfer characteristic of the amplifier of Example 1.2. Note that this amplifier is inverting (i.e., with a gain that is negative).

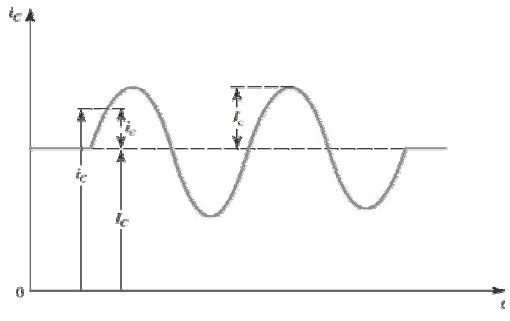

Figure 1.16 Symbol convention employed throughout the book.

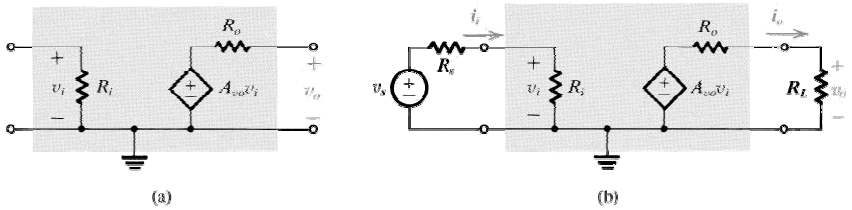

Figure 1.17 **(a)** Circuit model for the voltage amplifier. **(b)** The voltage amplifier with input signal source and load.

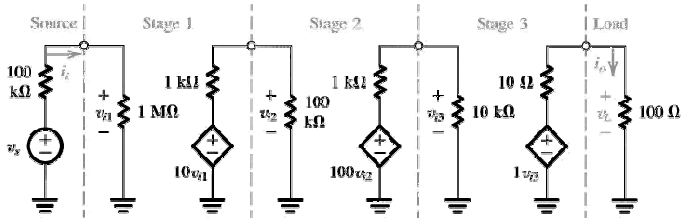

Figure 1.18 Three-stage amplifier for Example 1.3.

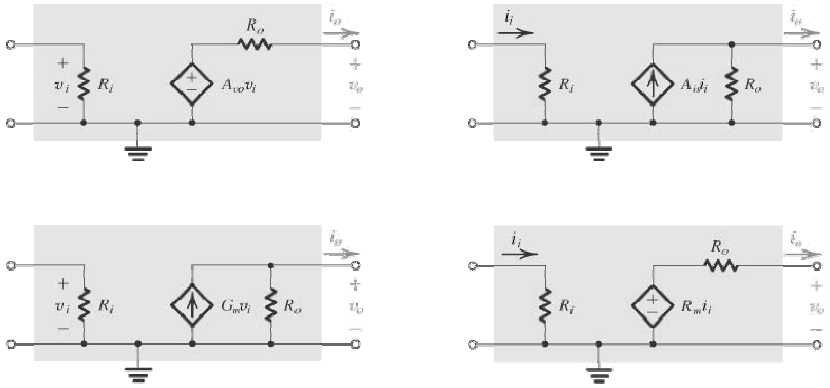

Table 1.1 The Four Amplifier Types

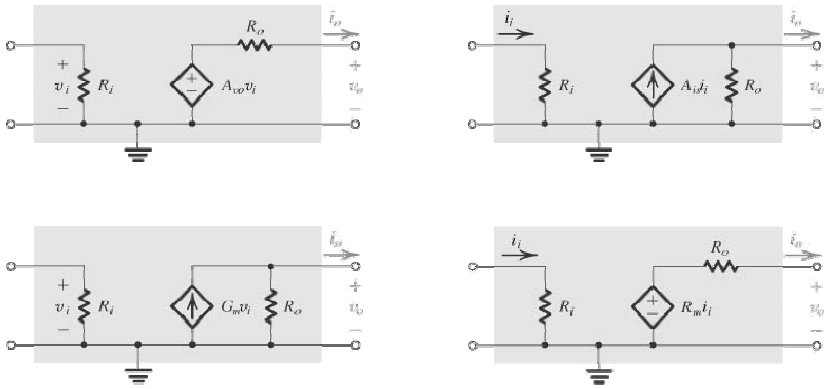

Table 1.1 The Four Amplifier Types

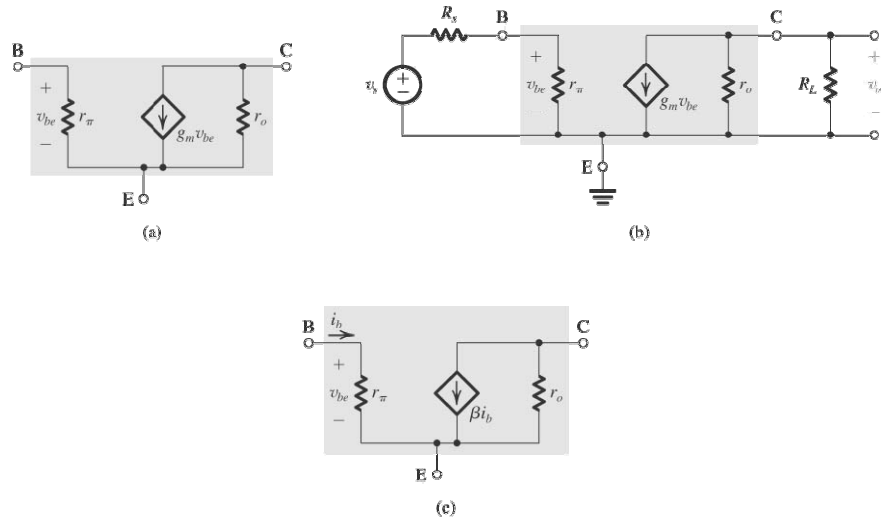

Figure 1.19 (a) Small-signal circuit model for a bipolar junction transistor (BJT). **(b)** The BJT connected as an amplifier with the emitter as a common terminal between input and output (called a common-emitter amplifier). **(c)** An alternative small-signal circuit model for the BJT.

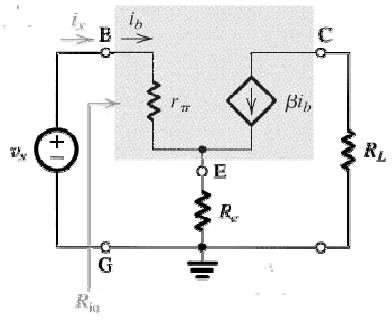

Figure E1.20

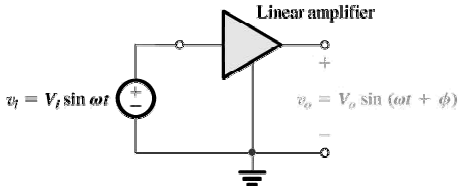

Figure 1.20 Measuring the frequency response of a linear amplifier. At the test frequency *v*, the amplifier gain is characterized by its magnitude (V_o/V_i) and phase *f*.

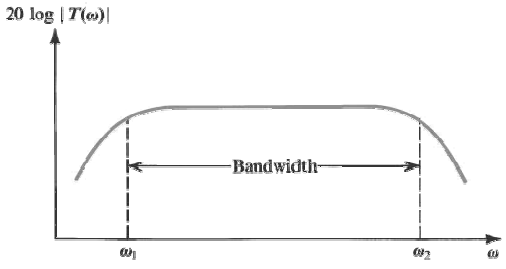

Figure 1.21 Typical magnitude response of an amplifier. $|T(V)|$ is the magnitude of the amplifier transfer function—that is, the ratio of the output $V_o(V)$ to the input $V_i(V)$.

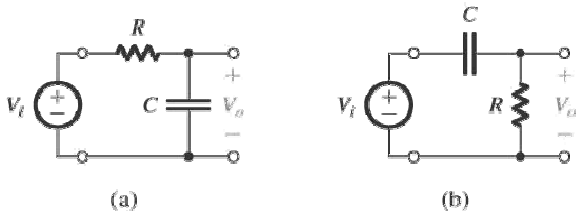

Figure 1.22 Two examples of STC networks: **(a)** a low-pass network and **(b)** a high-pass network.

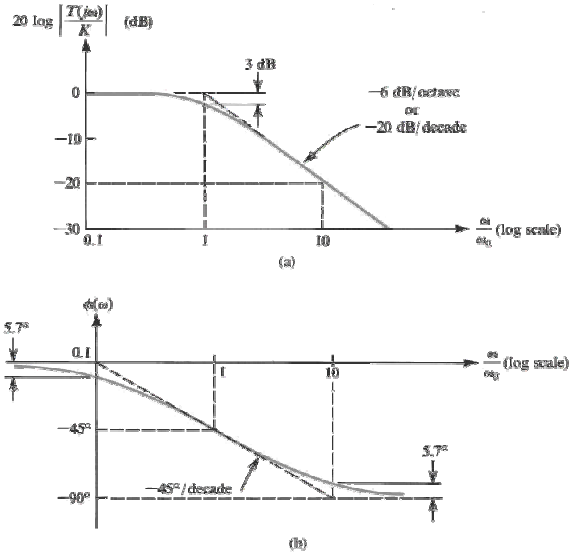

Figure 1.23 **(a)** Magnitude and **(b)** phase response of STC networks of the low-pass type.

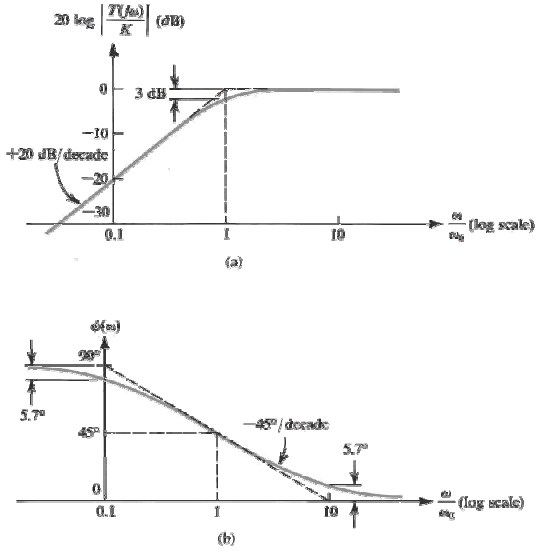

Figure 1.24 **(a)** Magnitude and **(b)** phase response of STC networks of the high-pass type.

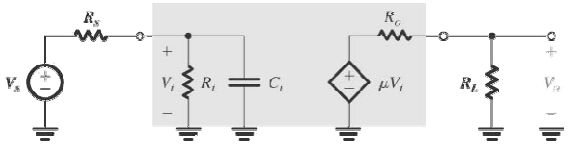

Figure 1.25 Circuit for Example 1.5.

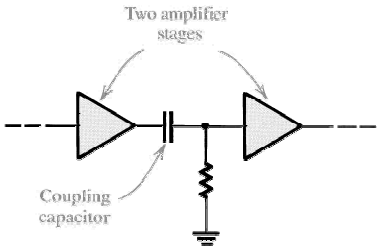

Figure 1.27 Use of a capacitor to couple amplifier stages.

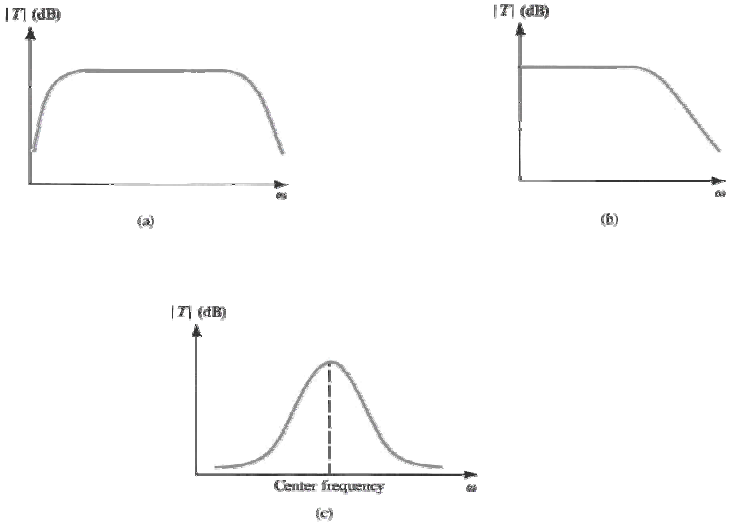

Figure 1.26 Frequency response for **(a)** a capacitively coupled amplifier, **(b)** a direct-coupled amplifier, and **(c)** a tuned or bandpass amplifier.

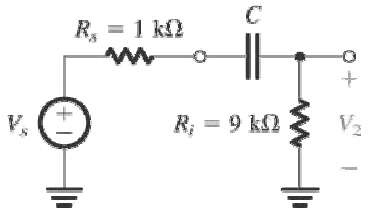

Figure E1.23

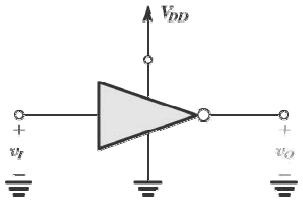

Figure 1.28 A logic inverter operating from a dc supply V_{DD}.

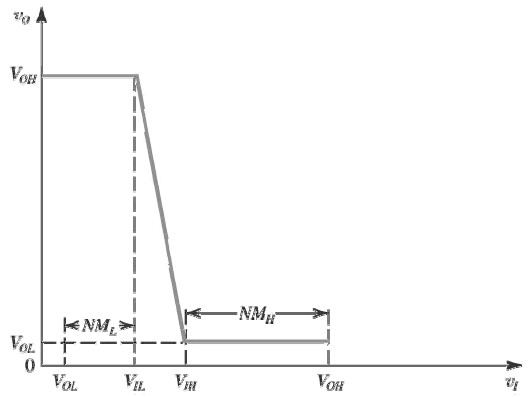

Figure 1.29 Voltage transfer characteristic of an inverter. The VTC is approximated by three straightline segments. Note the four parameters of the VTC (V_{OH}, V_{OL}, V_{IL}, and V_{IH}) and their use in determining the noise margins (NM_H and NM_L).

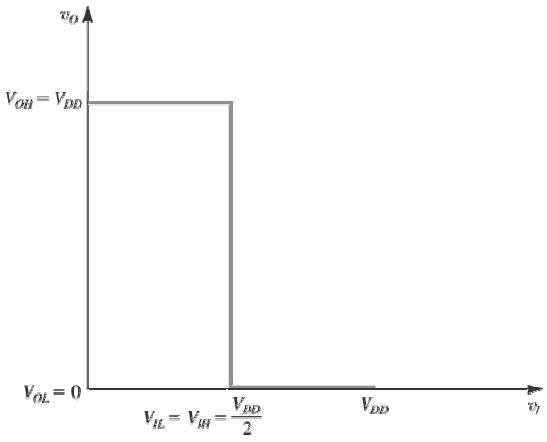

Figure 1.30 The VTC of an ideal inverter.

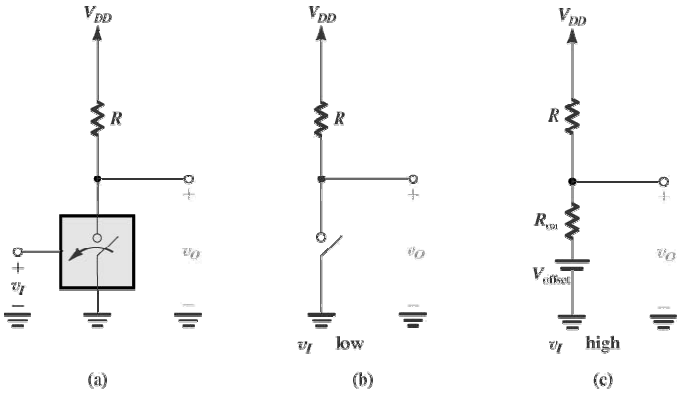

Figure 1.31 **(a)** The simplest implementation of a logic inverter using a voltage-controlled switch; **(b)** equivalent circuit when v_I is low; and **(c)** equivalent circuit when v_I is high. Note that the switch is assumed to close when v_I is high.

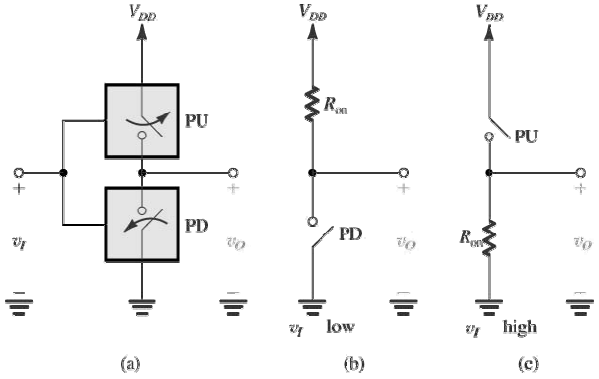

Figure 1.32 A more elaborate implementation of the logic inverter utilizing two complementary switches. This is the basis of the CMOS inverter studied in Section 4.10.

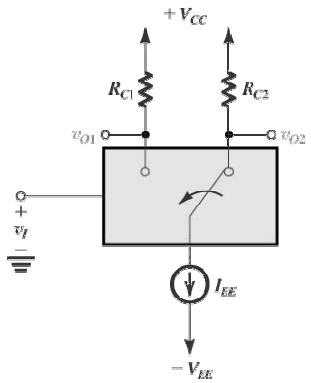

Figure 1.33 Another inverter implementation utilizing a double-throw switch to steer the constant current I_{EE} to R_{C1} (when v_I is high) or R_{C2} (when v_I is low). This is the basis of the emitter-coupled logic (ECL) studied in Chapters 7 and 11.

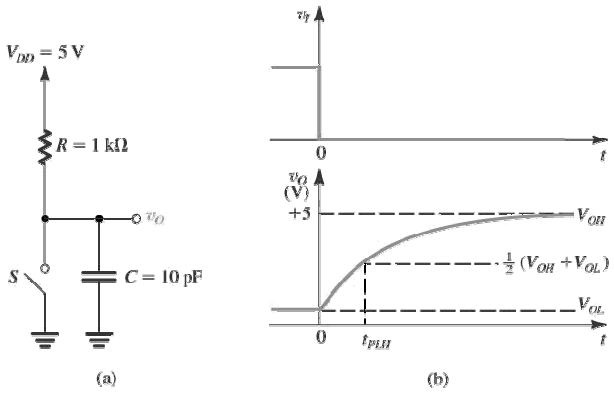

Figure 1.34 Example 1.6: **(a)** The inverter circuit after the switch opens (i.e., for $t \geq 0+$). **(b)** Waveforms of v_I and v_O. Observe that the switch is assumed to operate instantaneously. v_O rises exponentially, starting at V_{OL} and heading toward V_{OH}.

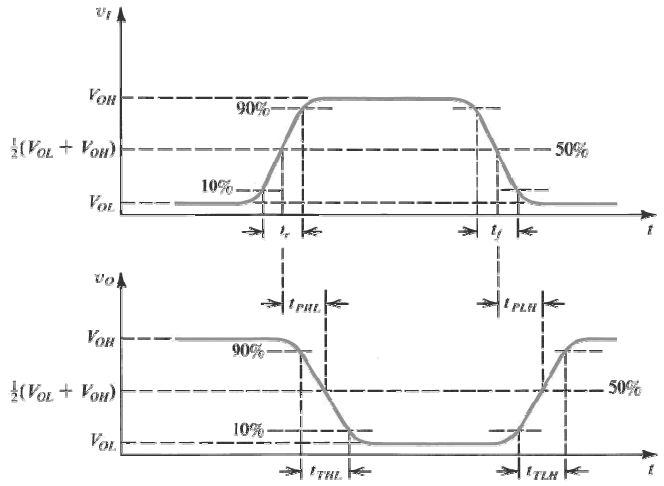

Figure 1.35 Definitions of propagation delays and transition times of the logic inverter.