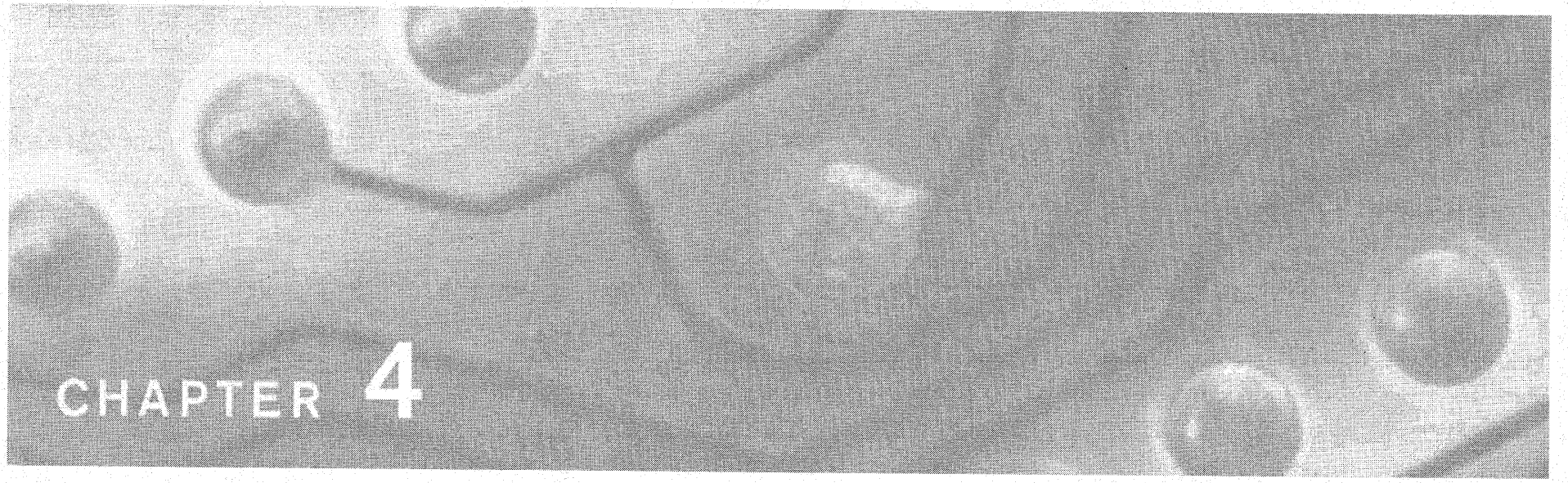
ECE321 Electronics I
Fall 2006

Professor James E. Morris

Lecture 8

19th October, 2006



MOS Field-Effect Transistors (MOSFETs)

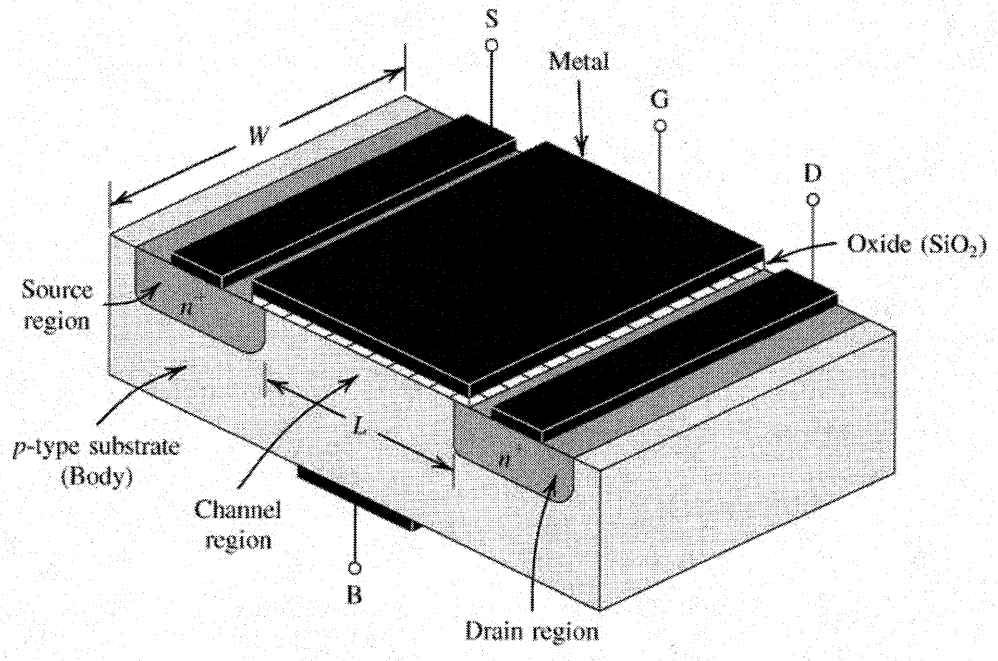
Metal-oxide-semiconductor field-effect transistor

4.1 Device Physics

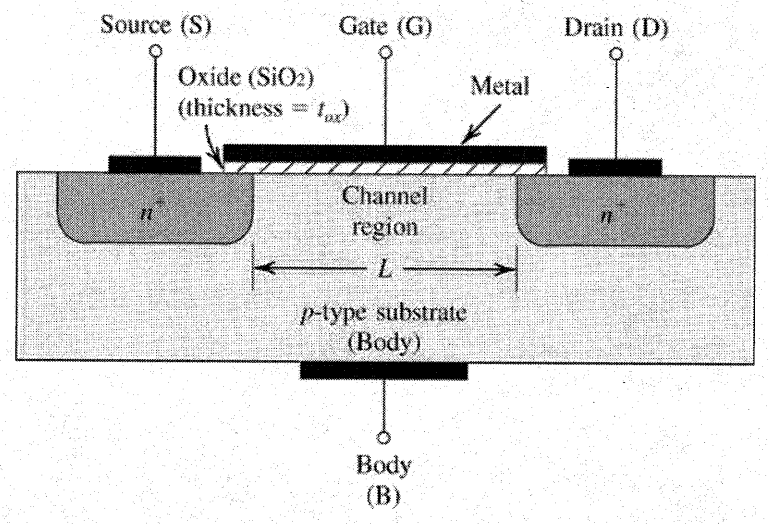
4.2 I – V Characteristics

DEVICE STRUCTURE

N-Channel



(a)



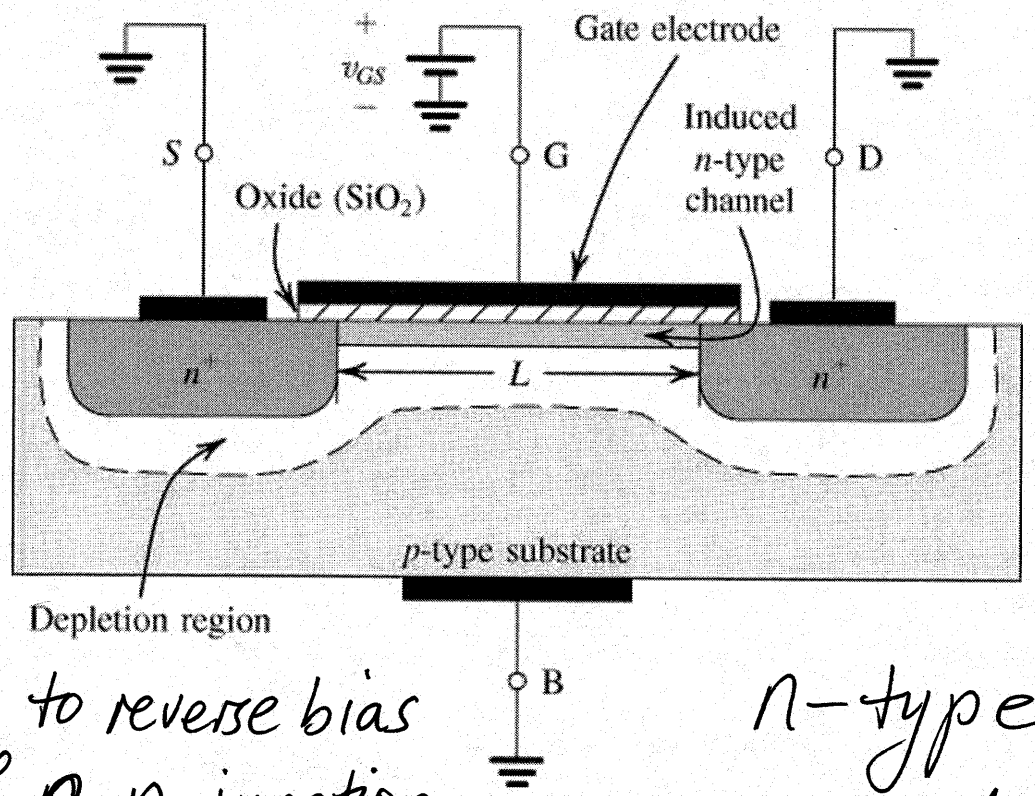
(b)

Symmetrical? Not always in practice — minimize C_{gd}

Figure 4.1 Physical structure of the enhancement-type NMOS transistor: **(a)** perspective view; **(b)** cross-section. Typically L = 0.1 to 3 μm, W = 0.2 to 100 μm, and the thickness of the oxide layer (t_{ox}) is in the range of 2 to 50 nm.

MOSFET as Capacitor

$C_{gate} \rightarrow C_{ox}$ per unit area

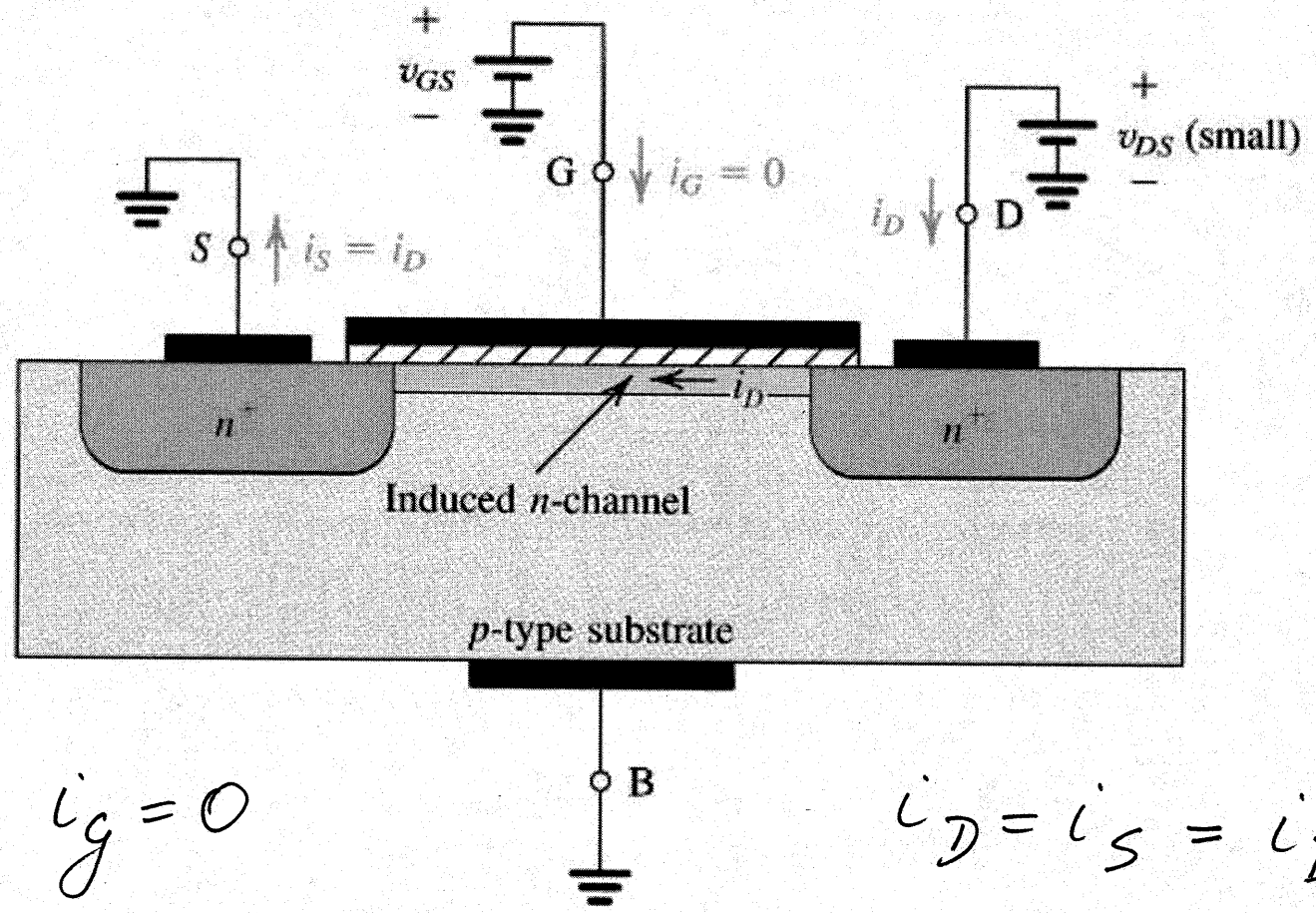


Due to reverse bias of p-n junction to substrate

n-type channel → electrons

Figure 4.2 The enhancement-type NMOS transistor with a positive voltage applied to the gate. An *n* channel is induced at the top of the substrate beneath the gate.

MOSFET as Resistor r_{DS}



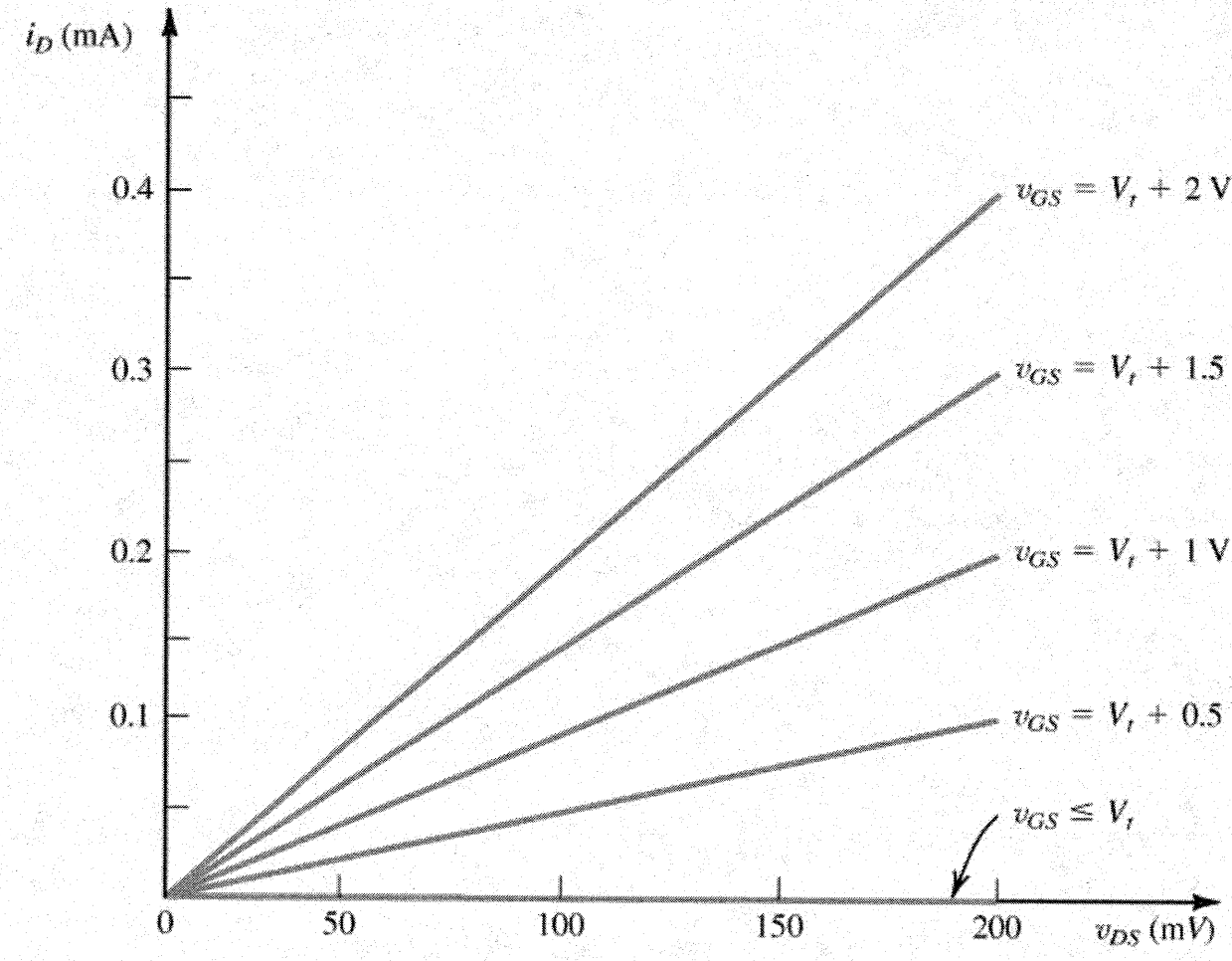
Note: $i_g = 0$

$i_D = i_S = i_{DS}$

$q_n = C_{gate} V_G$

Figure 4.3 An NMOS transistor with $v_{GS} > V_t$ and with a small v_{DS} applied. The device acts as a resistance whose value is determined by v_{GS}. Specifically, the channel conductance is proportional to $v_{GS} - V_t$, and thus i_D is proportional to $(v_{GS} - V_t)\, v_{DS}$. Note that the depletion region is not shown (for simplicity).

Characteristics for $v_{DS} \geq 0$

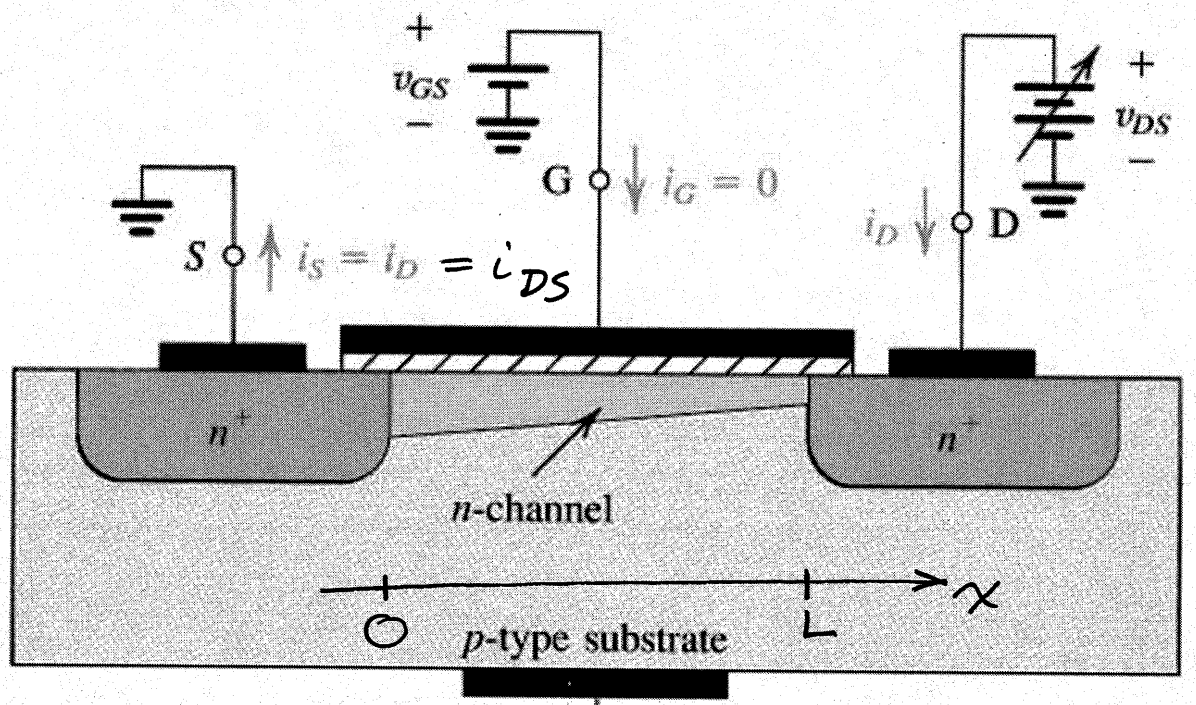


AGC applications as voltage (V_G) controlled resistance

But NOT actually linear!

Figure 4.4 The i_D–v_{DS} characteristics of the MOSFET in Fig. 4.3 when the voltage applied between drain and source, v_{DS}, is kept small. The device operates as a linear resistor whose value is controlled by v_{GS}.

Increasing $v_{DS} \longrightarrow$



$v_{gx} = v_{gs}$ at Source

$v_{gx} = v_{gD}$ $(< v_{gs})$ at Drain

$v_g - v(x)$ along channel

Figure 4.5 Operation of the enhancement NMOS transistor as v_{DS} is increased. The induced channel acquires a tapered shape, and its resistance increases as v_{DS} is increased. Here, v_{GS} is kept constant at a value > V_t.

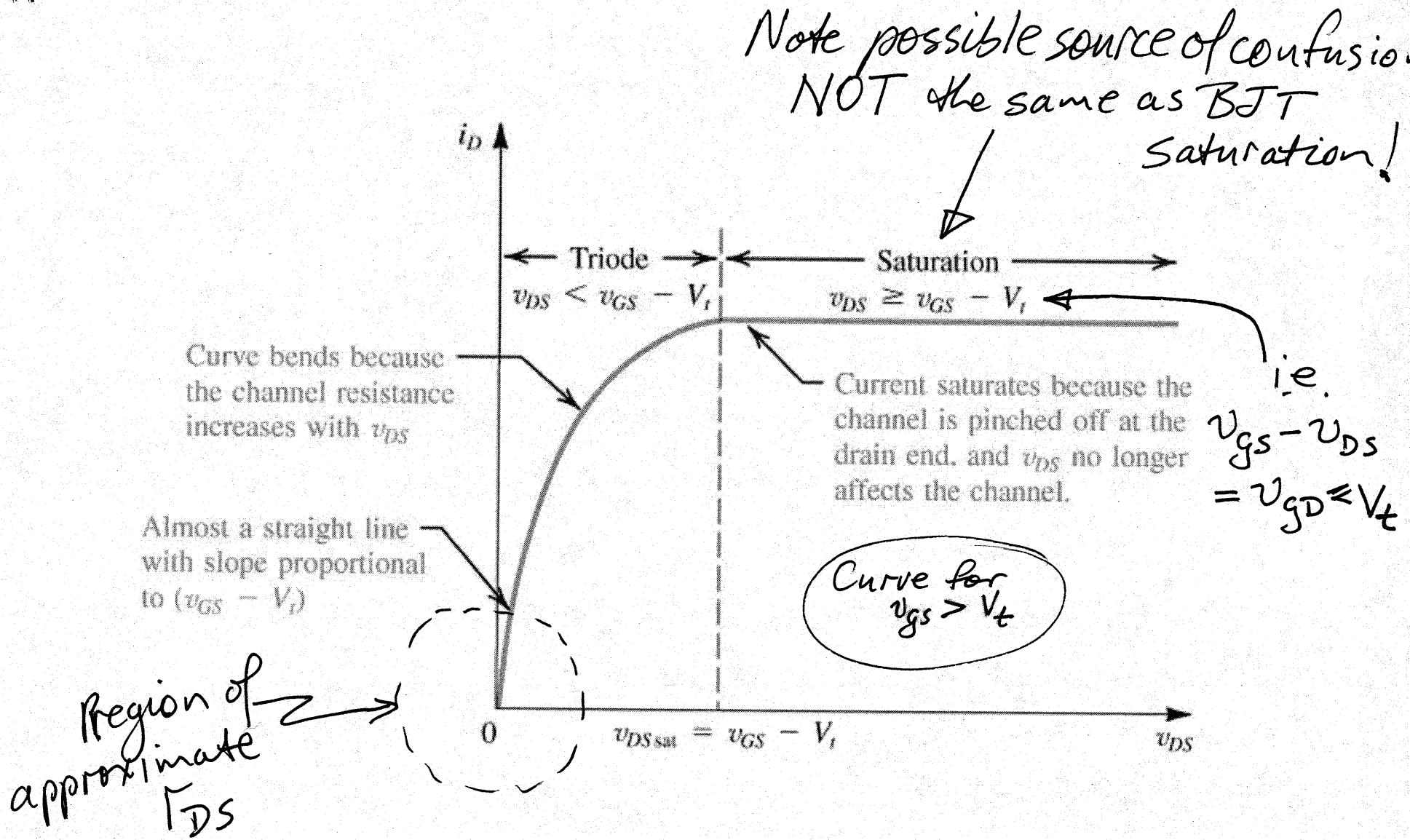
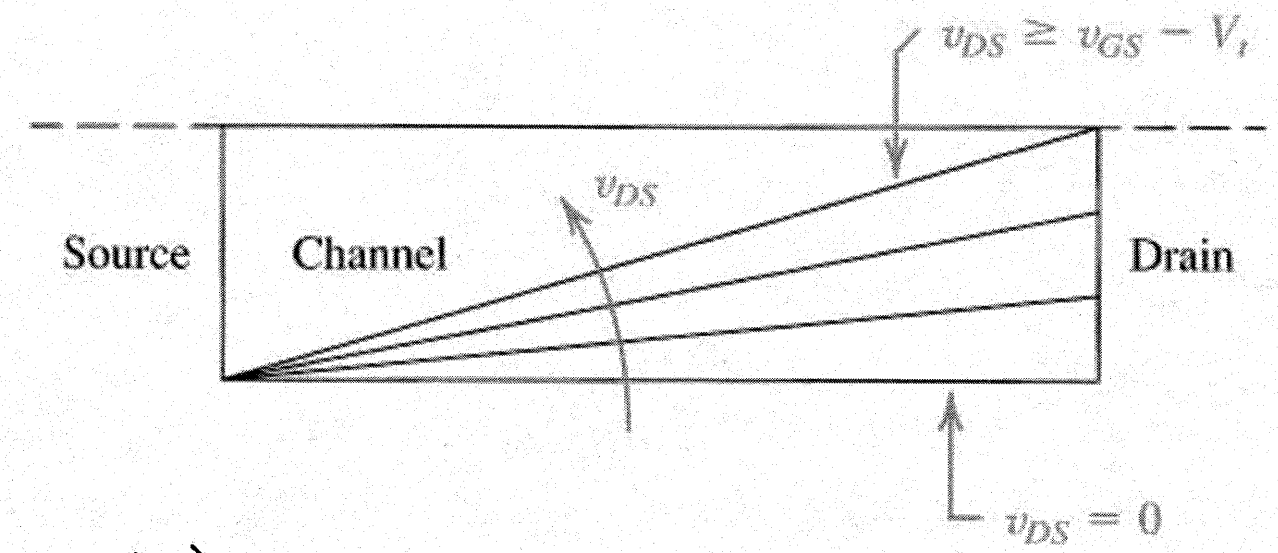


Figure 4.6 The drain current i_D versus the drain-to-source voltage v_{DS} for an enhancement-type NMOS transistor operated with $v_{GS} > V_t$.

$$v_{DS})_{sat} = v_{gs} - V_t$$



$v_{DS} > v_{DS})_{sat}$ $v_{DS} - v_{DS})_{sat}$ reverse bias extends across channel

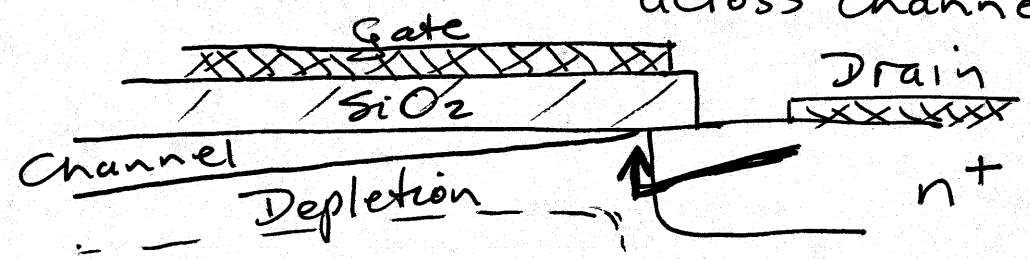


Figure 4.7 Increasing v_{DS} causes the channel to acquire a tapered shape. Eventually, as v_{DS} reaches $v_{GS} - V_t$ the channel is pinched off at the drain end. Increasing v_{DS} above $v_{GS} - V_t$ has little effect (theoretically, no effect) on the channel's shape.

(see later)

I_D vs V_{DS}

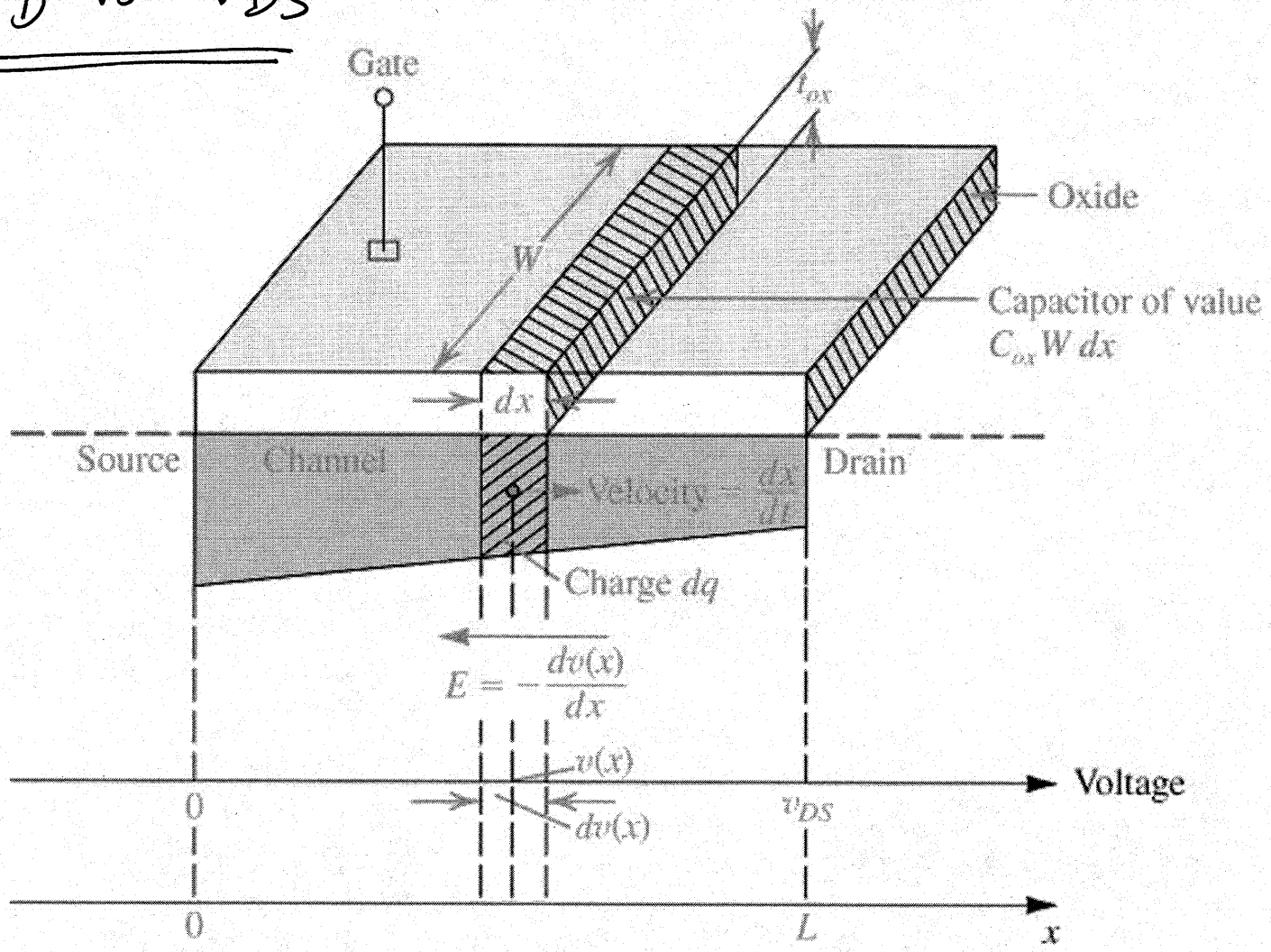


Figure 4.8 Derivation of the i_D–v_{DS} characteristic of the NMOS transistor.

I-V Characteristics

$C = \frac{\varepsilon A}{t} \Rightarrow C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}}$ /unit area

$\varepsilon_{ox} = 3.9\varepsilon_0$ for SiO_2

$= 3.9 \times 8.85 \times 10^{-12}$ F/m

$= 34.5 \times 10^{-12}$ F/m

For element $dx \Rightarrow$ Injected charge $dq_n(x) = -C_{ox}(W dx)(V_{GS} - v(x) - V_t)$

V_t = Threshold voltage (Surface states; ion implants)

Enhancement device $\longrightarrow V_t \geq 0$ No i_{DS} at $V_{GS} = 0$

Depletion device $\longrightarrow V_t \leq 0$ Finite $i_{DS}(v_{DS})$ at $V_{GS} = 0$

Enhancement: Typically need to exceed $v_{GS} > V_t \sim 1$ volt for i_{DS} to flow.

Depletion: Need to reduce v_{GS} below $V_t \sim -1$ volt or so to cut off i_{DS} flow.

Also:

Field along channel $E(x) = -dv(x)/dx$

& Drift electron current:

Electron velocity $\frac{dx}{dt} = -\mu_n E(x) = \mu_n \frac{dv(x)}{dx}$

(cont'd)

$$i(x) = \frac{dq_n(x)}{dt} = \frac{dq_n(x)}{dx}\cdot\frac{dx}{dt} = -\left[-C_{ox}W(v_{gs}-v(x)-V_t)\right]\left[\mu_n \frac{dv(x)}{dx}\right]$$

$$= i_{DS} = \mu_n C_{ox} W (v_{gs} - v(x) - V_t) \frac{dv(x)}{dx}$$

ie. $$i_{DS}\,dx = \mu_n C_{ox} W (v_{gs} - V_t - v(x))\, dv(x)$$

and $$\int_0^L i_{DS}\,dx = \mu_n C_{ox} W \int_0^L [v_{gs} - V_t - v(x)]\, dv(x)$$

$$i_{DS} L = \mu_n C_{ox} W \left[(v_{gs}-V_t)v(x) - \frac{1}{2}v(x)^2 \right]_0^L$$

$$i_{DS} = \mu_n C_{ox} \left(\frac{W}{L}\right) \left[(v_{gs}-V_t)v_{DS} - v_{DS}^2/2\right]$$

in the TRIODE region.

At saturation, when $v_{gs} - v_{DS} \leq V_t$ or $v_{DS} \geq v_{gs} - V_t$

$$i_D)_{sat} = \mu_n C_{ox}\left(\frac{W}{L}\right)\left[(v_{gs}-V_t)^2 - (v_{gs}-V_t)^2/2\right]$$

$$= \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)\left[v_{gs}-V_t\right]^2$$

Note:

TRIODE	$i_D = k_n'(W/L)\left[(v_{gs}-V_t)v_{DS} - v_{DS}^2/2\right]$
SATURATION	$i_D = \frac{1}{2}k_n'(W/L)(v_{gs}-V_t)^2$

where $k_n' = \mu_n C_{ox}$

$\frac{W}{L} \Rightarrow$ "aspect ratio"

Minimum channel length ~ 90nm in production.

Ex 4.3 $\quad i_D(\text{triode}) = k_n'\left(\frac{W}{L}\right)\left[V_{ov}\, v_{DS} - v_{DS}^2/2\right]$ where V_{ov} = "over-voltage" $= V_{gs} - V_t$

$$\frac{\partial i_D}{\partial v_{DS}} = k_n'\left(\frac{W}{L}\right)\left(V_{ov} - v_{DS}\right)$$

$$\approx k_n'\left(\frac{W}{L}\right) V_{ov} \qquad \text{if } v_{DS} \ll V_{ov}$$

$$\therefore r_{DS} = \frac{\partial v_{DS}}{\partial i_D} = \frac{1}{k_n'\left(\frac{W}{L}\right)V_{ov}}$$

(Note: reference to "saturation" in text exercise seems to be an error.)

Exercise 4.2

CMOS Structure

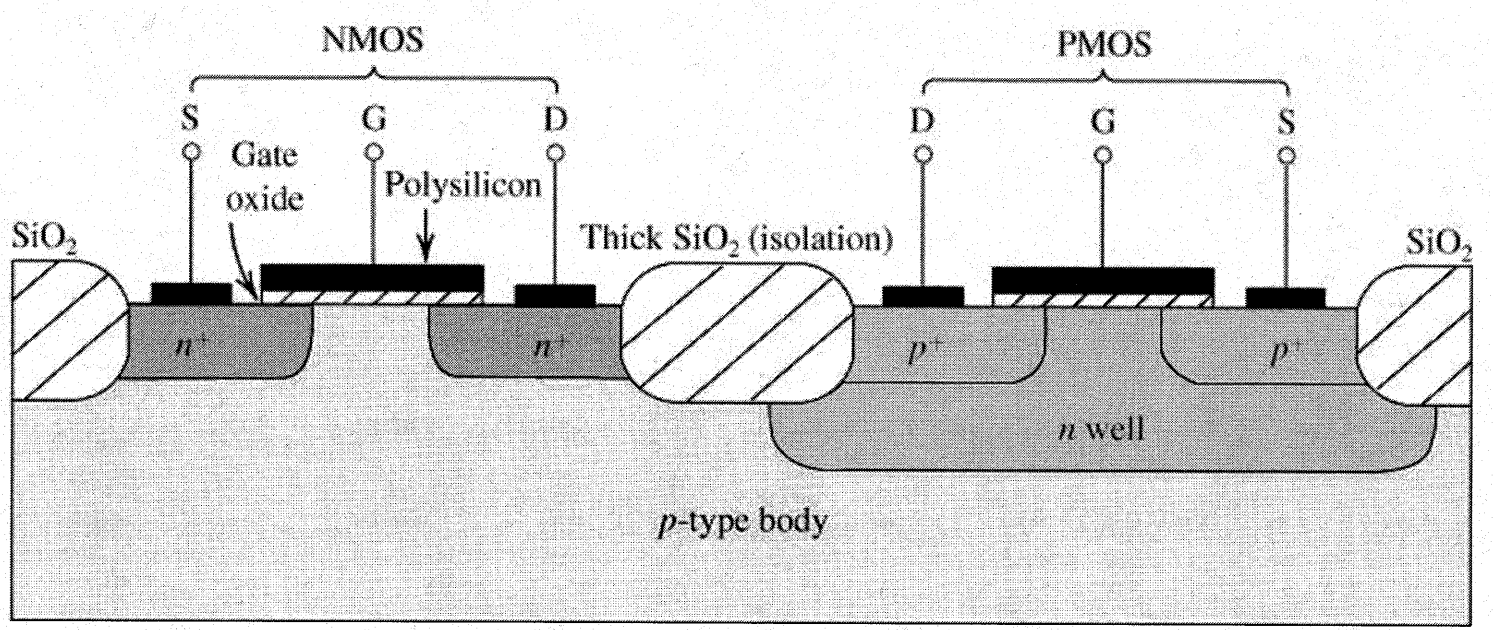
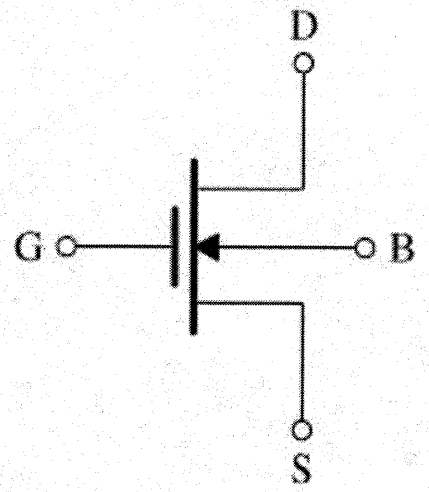
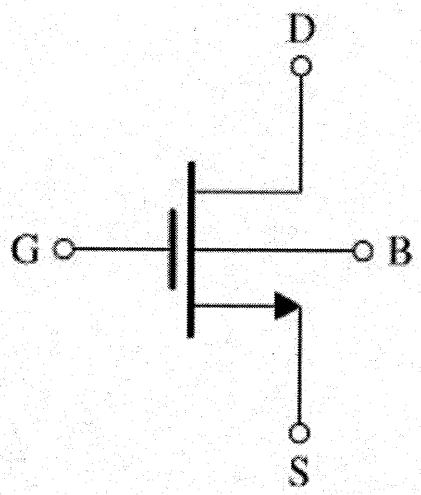


Figure 4.9 Cross-section of a CMOS integrated circuit. Note that the PMOS transistor is formed in a separate *n*-type region, known as an *n* well. Another arrangement is also possible in which an *n*-type body is used and the *n* device is formed in a *p* well. Not shown are the connections made to the *p*-type body and to the *n* well; the latter functions as the body terminal for the *p*-channel device.

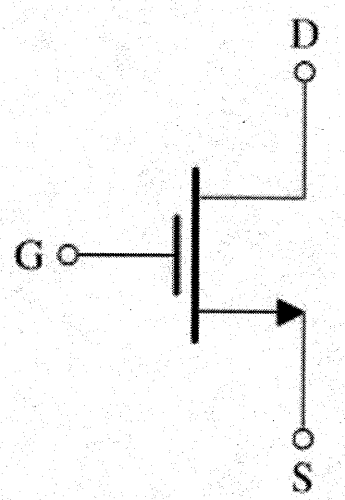
Symbols : NMOS / n-channel



(a)



(b)



(c)

Arrow shows :

p-substrate

Current flow
drain → source

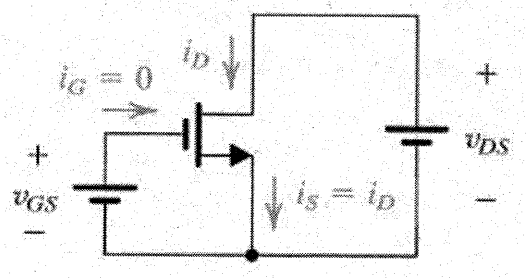
Conventional circuit symbol

S-B connection or B irrelevant

Figure 4.10 **(a)** Circuit symbol for the *n*-channel enhancement-type MOSFET. **(b)** Modified circuit symbol with an arrowhead on the source terminal to distinguish it from the drain and to indicate device polarity (i.e., *n* channel). **(c)** Simplified circuit symbol to be used when the source is connected to the body or when the effect of the body on device operation is unimportant.

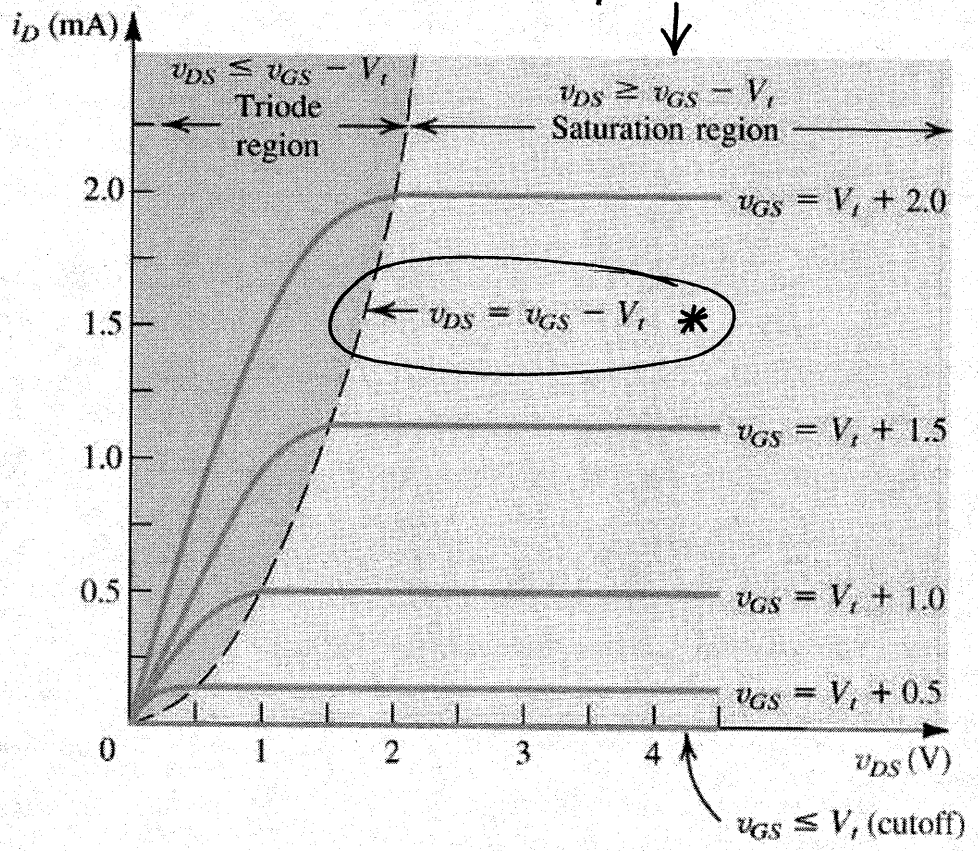
Characteristics

Amplifier applications



(a)

Defines polarities, etc



(b)

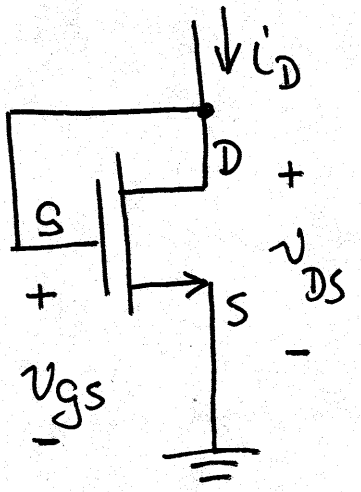
Figure 4.11 **(a)** An *n*-channel enhancement-type MOSFET with v_{GS} and v_{DS} applied and with the normal directions of current flow indicated. **(b)** The i_D–v_{DS} characteristics for a device with $k'_n(W/L) = 1.0$ mA/V^2.

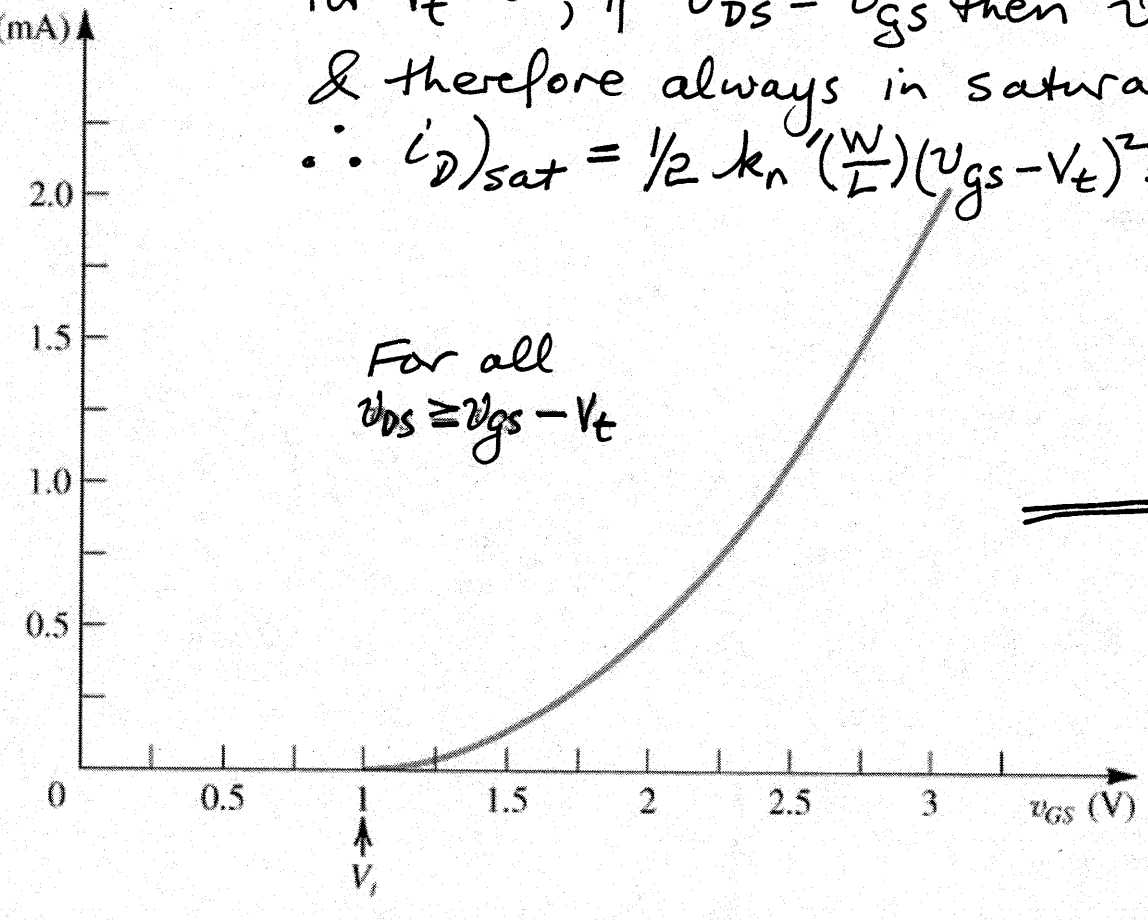
Saturation

Device is in saturation if $v_{DS} \geq v_{gs} - V_t$

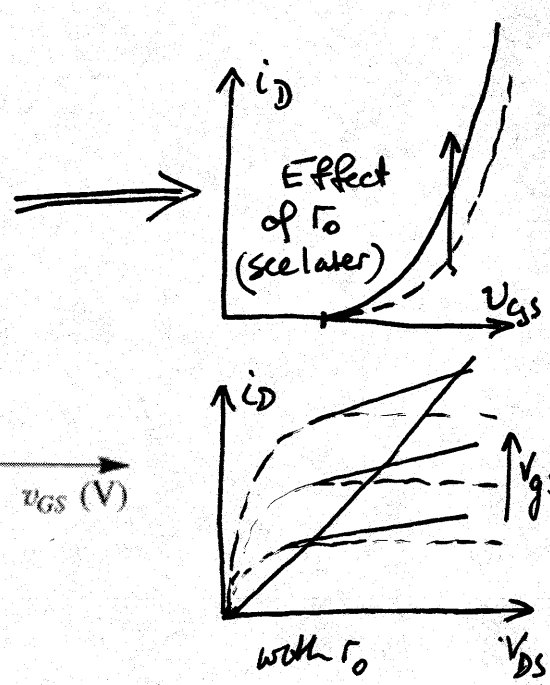
For $V_t \geq 0$, if $v_{DS} = v_{gs}$ then $v_{DS} \geq v_{gs} - V_t$
& therefore always in saturation.

$\therefore i_D)_{sat} = \frac{1}{2} k_n'' \left(\frac{W}{L}\right)(v_{gs} - V_t)^2 = \frac{1}{2} k_n' \left(\frac{W}{L}\right)(v_{DS} - V_t)^2$





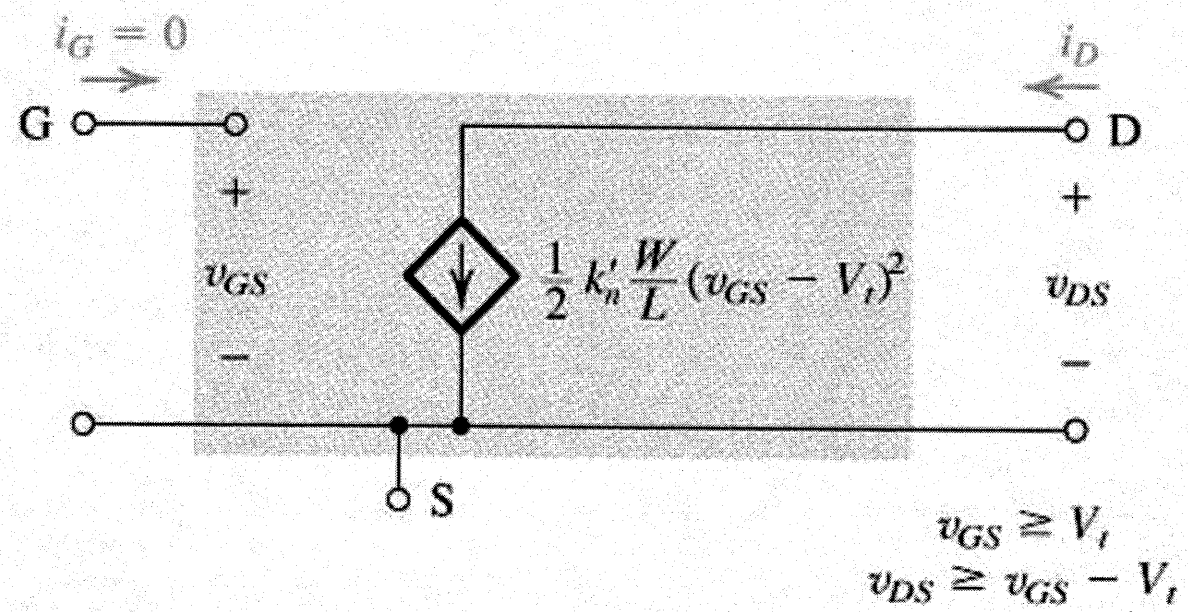
For all
$v_{DS} \geq v_{gs} - V_t$



Often used as measurement of V_t

Figure 4.12 The i_D–v_{GS} characteristic for an enhancement-type NMOS transistor in saturation (V_t = 1 V, $k'_n W/L$ = 1.0 mA/V^2).

Equivalent circuit : Saturation Region



$R_{in} = \infty$

Figure 4.13 Large-signal equivalent-circuit model of an *n*-channel MOSFET operating in the saturation region.

Summary of voltage ranges for operational modes

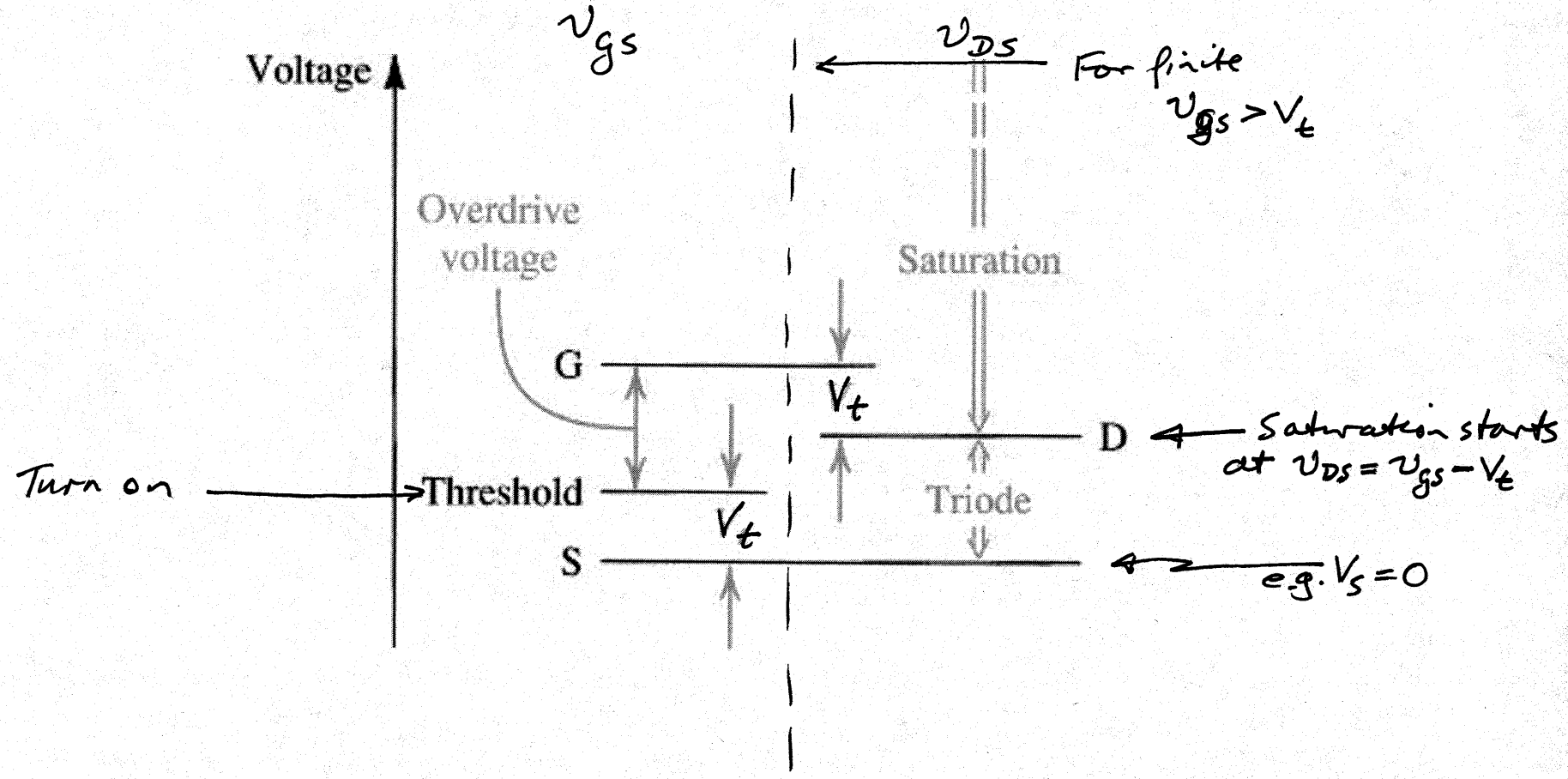


Figure 4.14 The relative levels of the terminal voltages of the enhancement NMOS transistor for operation in the triode region and in the saturation region.

Exercises

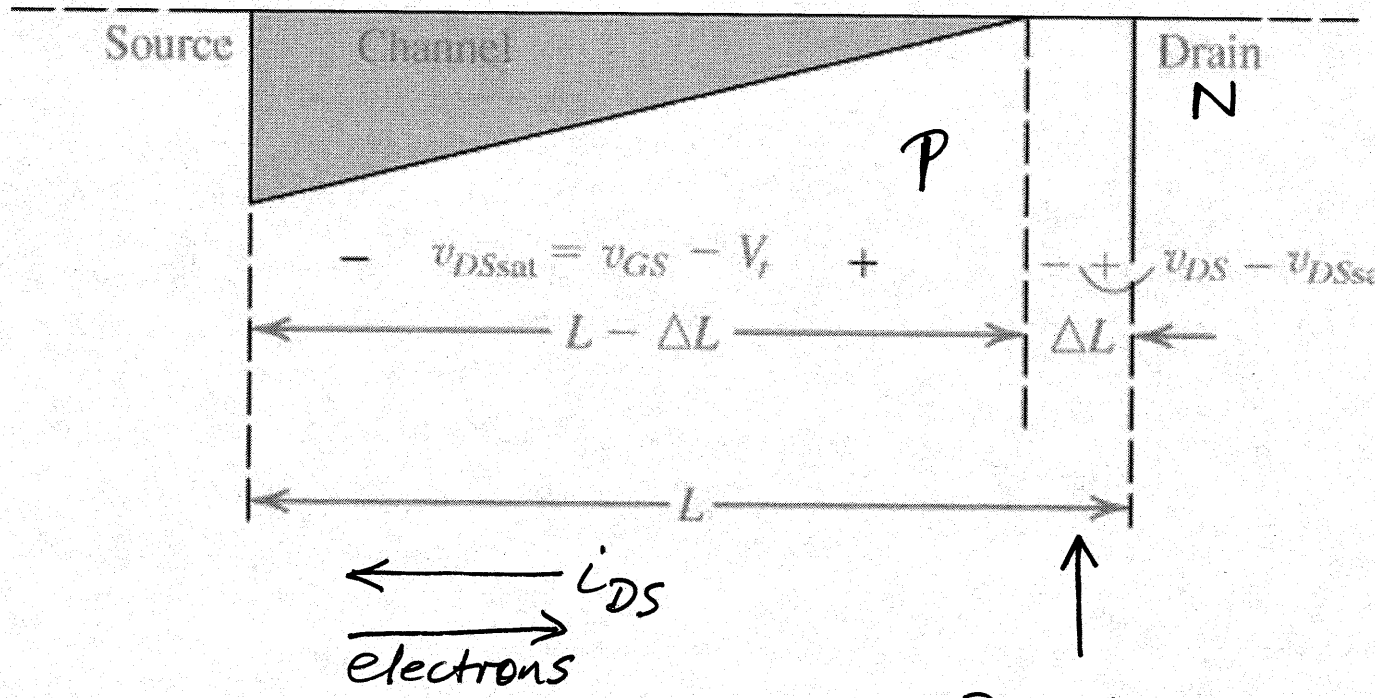
4.4

4.5

To

Channel-length Modulation

See Fig 4.2 again
Depletion region between S/channel/D and P-type substrate



Channel shortened by ΔL

Depletion region extends into channel-drain gap.

Electrons from channel accelerated by reverse bias across depletion region into drain

Figure 4.15 Increasing v_{DS} beyond v_{DSsat} causes the channel pinch-off point to move slightly away from the drain, thus reducing the effective channel length (by DL).

Channel-length Modulation & r_o $\quad L \longrightarrow L - \Delta L$

$$i_D)_{sat} = \frac{1}{2} k_n' \frac{W}{L - \Delta L} (v_{GS} - V_t)^2$$

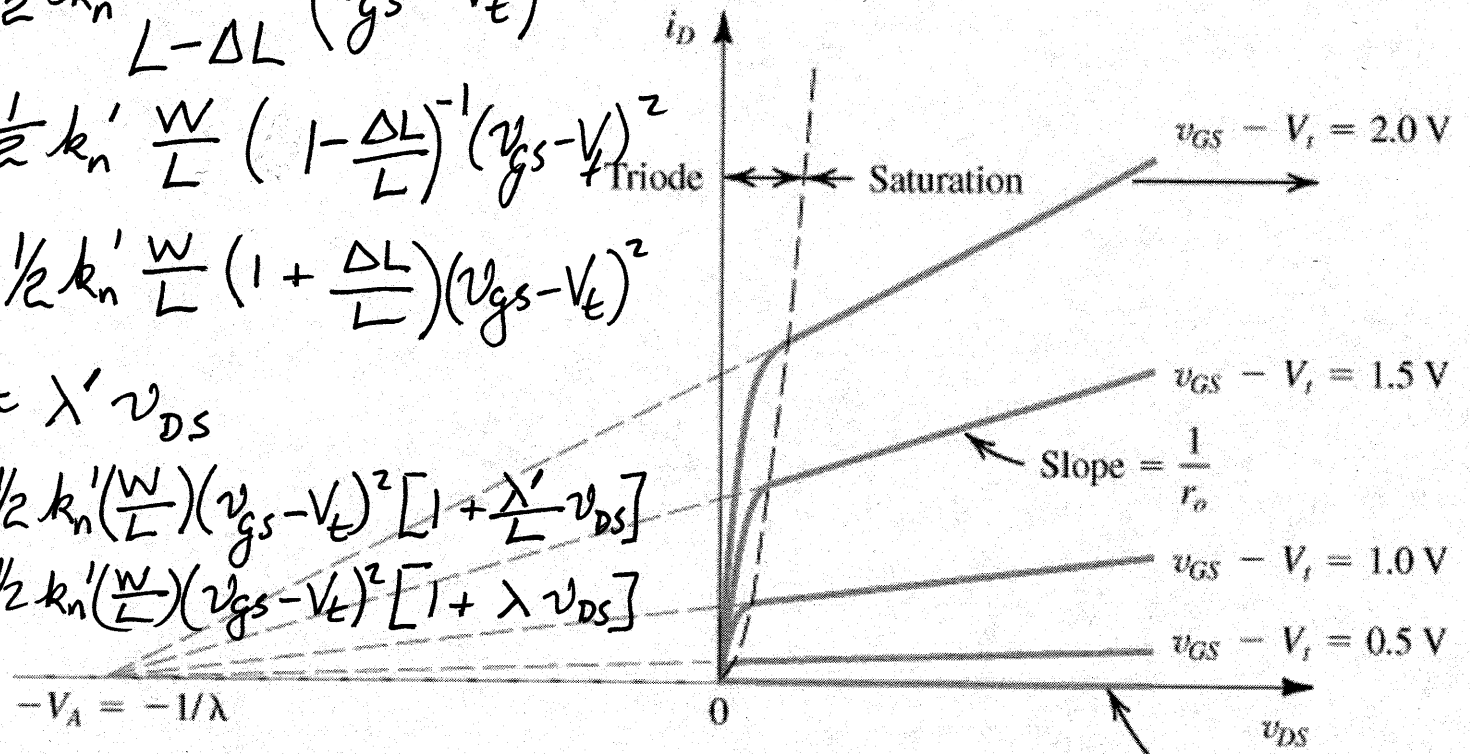
$$= \frac{1}{2} k_n' \frac{W}{L} \left(1 - \frac{\Delta L}{L}\right)^{-1} (v_{GS} - V_t)^2$$

$$\approx \frac{1}{2} k_n' \frac{W}{L} \left(1 + \frac{\Delta L}{L}\right) (v_{GS} - V_t)^2$$

& if $\Delta L \approx \lambda' v_{DS}$

$$i_D)_{sat} \approx \frac{1}{2} k_n' \left(\frac{W}{L}\right) (v_{GS} - V_t)^2 \left[1 + \frac{\lambda'}{L} v_{DS}\right]$$

$$= \frac{1}{2} k_n' \left(\frac{W}{L}\right) (v_{GS} - V_t)^2 \left[1 + \lambda v_{DS}\right]$$



Also define Early Voltage $V_A = 1/\lambda = L/\lambda' = V_A' L$

$$\lambda = \lambda'/L$$

Figure 4.16 Effect of v_{DS} on i_D in the saturation region. The MOSFET parameter V_A depends on the process technology and, for a given process, is proportional to the channel length L.

Exercise 4.6

Equivalent circuit with r_o

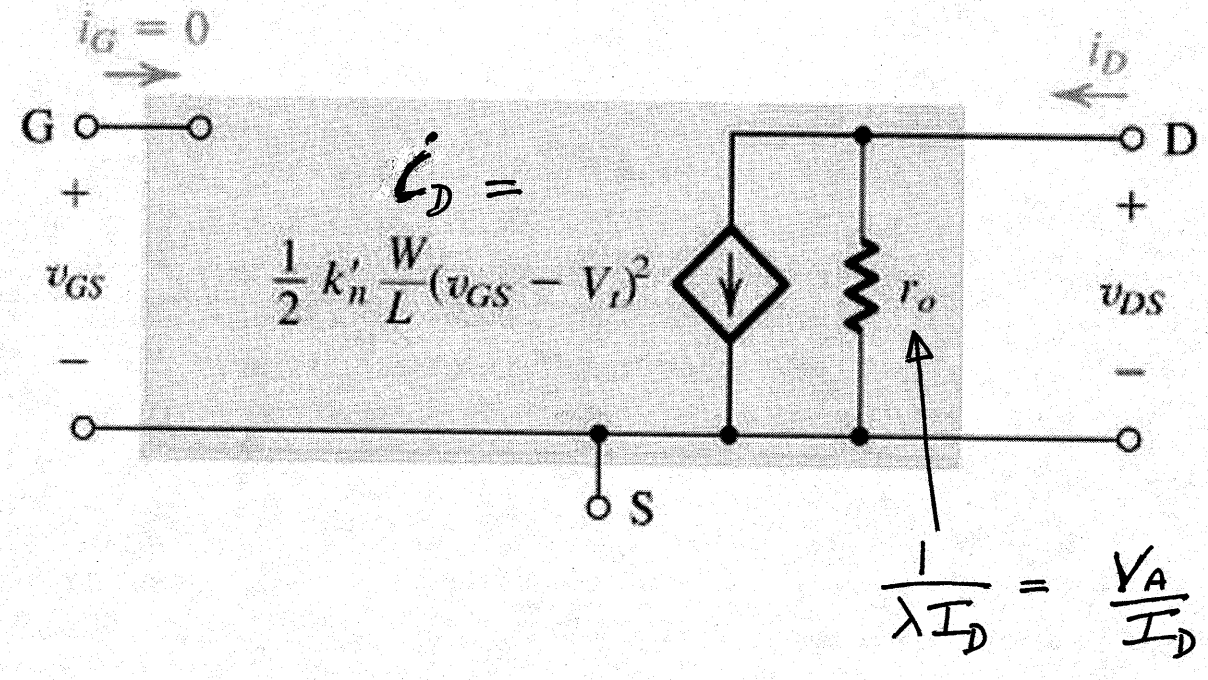
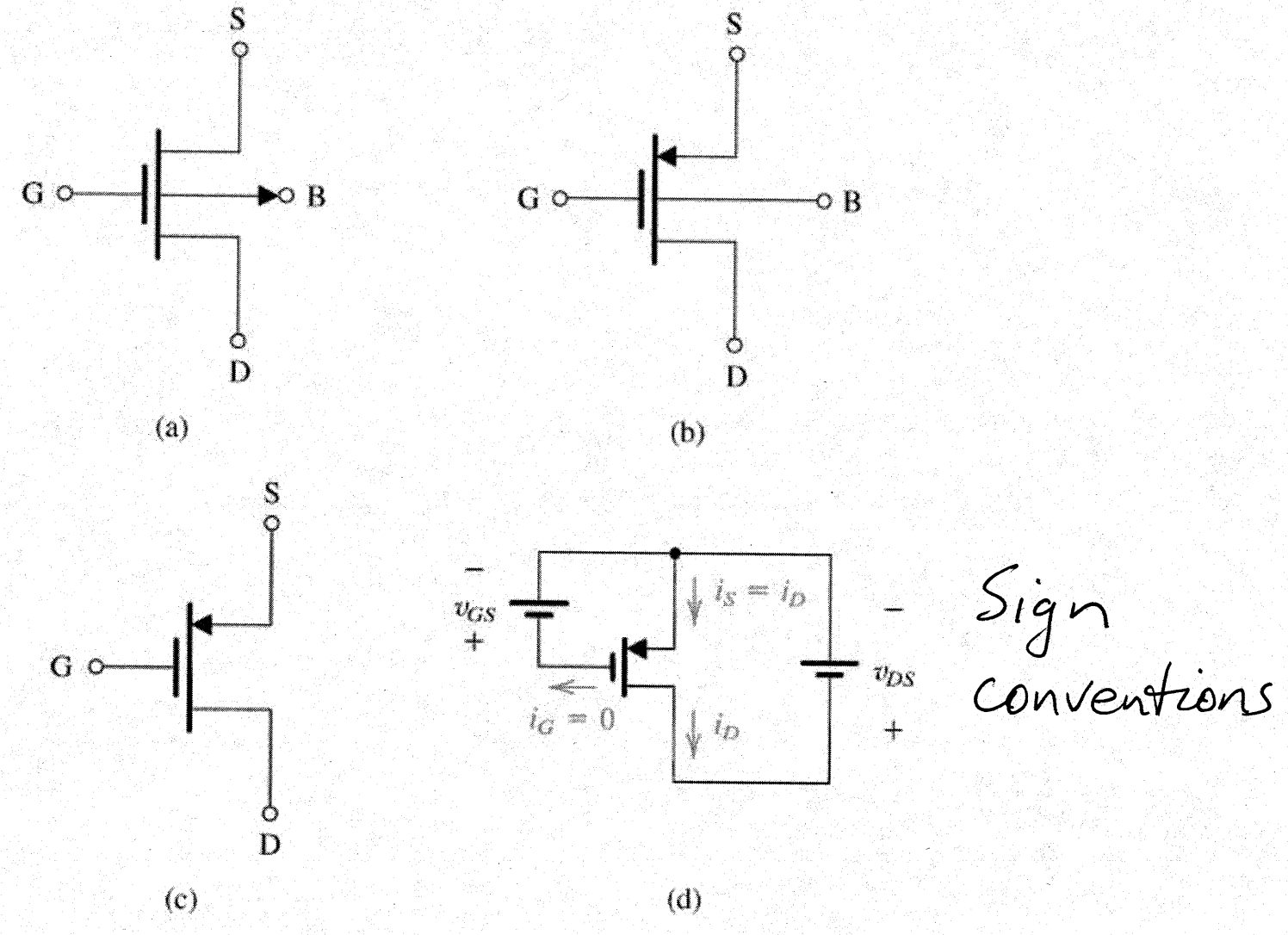


Figure 4.17 Large-signal equivalent circuit model of the *n*-channel MOSFET in saturation, incorporating the output resistance r_o. The output resistance models the linear dependence of i_D on v_{DS} and is given by Eq. (4.22).

P Channel, symbols, etc



Sign conventions

Figure 4.18 **(a)** Circuit symbol for the *p*-channel enhancement-type MOSFET. **(b)** Modified symbol with an arrowhead on the source lead. **(c)** Simplified circuit symbol for the case where the source is connected to the body. **(d)** The MOSFET with voltages applied and the directions of current flow indicated. Note that v_{GS} and v_{DS} are negative and i_D flows out of the drain terminal.

P channel

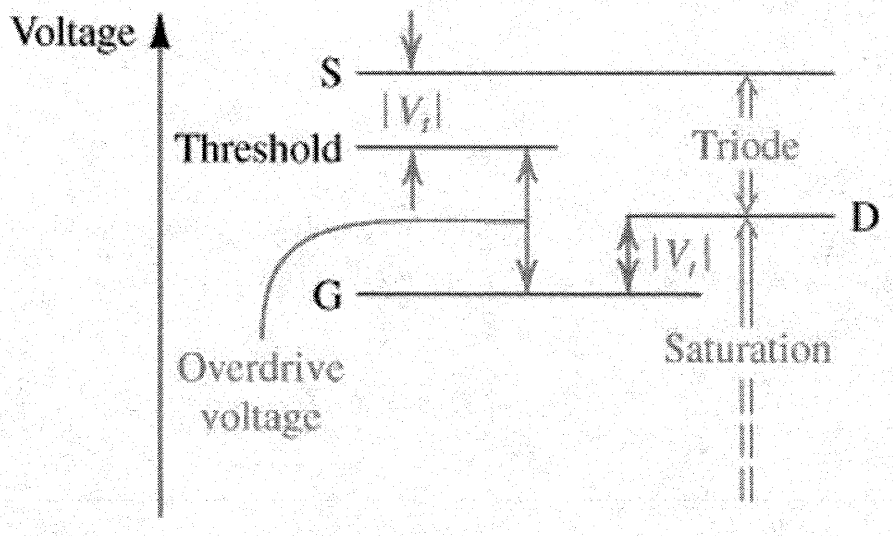
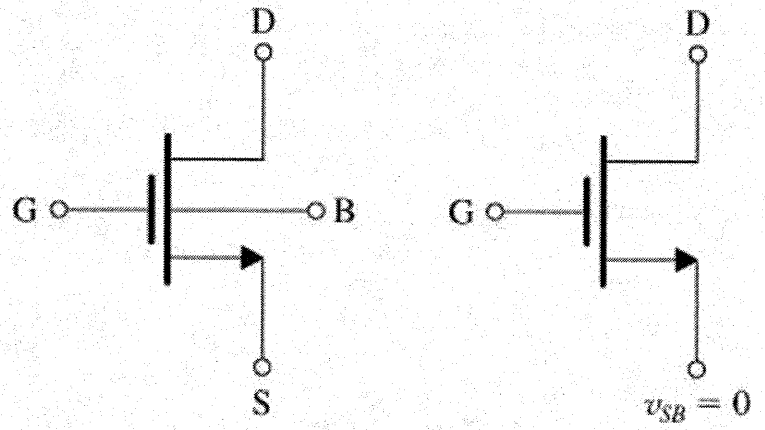
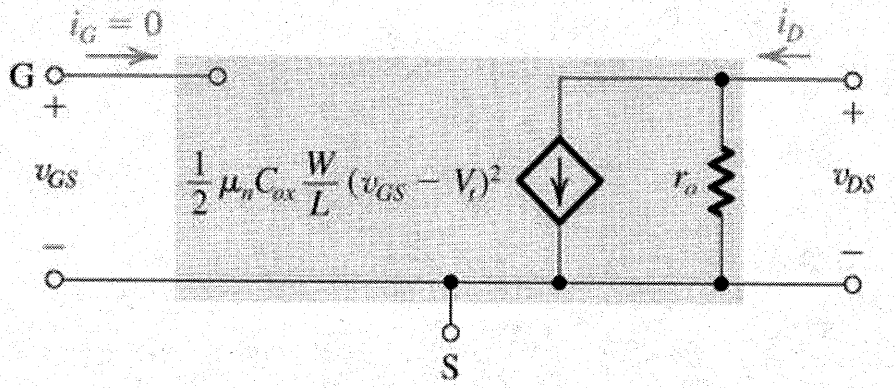


Figure 4.19 The relative levels of the terminal voltages of the enhancement-type PMOS transistor for operation in the triode region and in the saturation region.

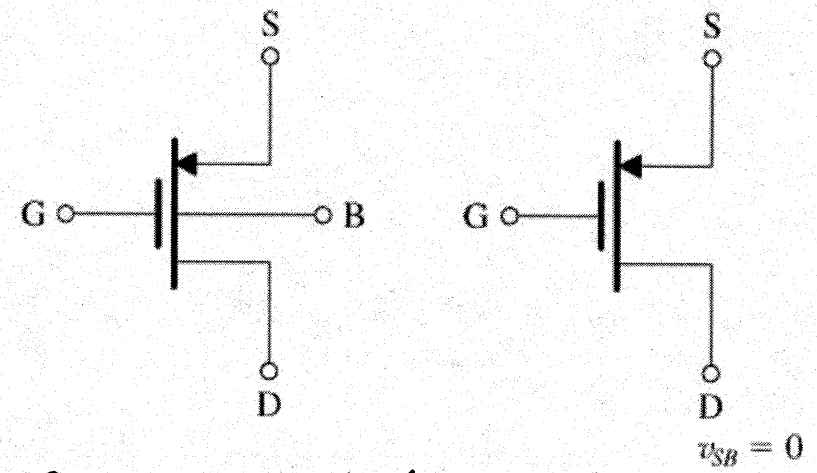
Exercise 4.8

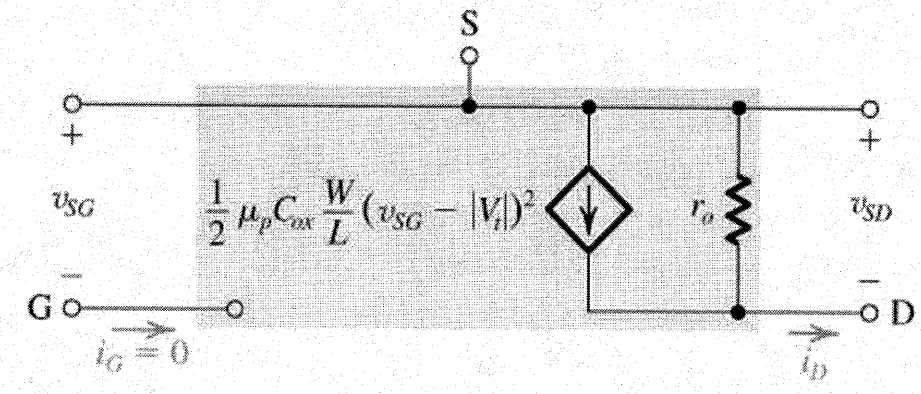
Summary





N-channel (NMOS)





P-channel (PMOS)

See equations pp 260-261 & PMOS variations pp 261-262

Table 4.1

Note (not covered): $V_t = V_{to} + \gamma\left(\sqrt{2\phi_f + |V_{SB}|} - \sqrt{2\phi_f}\right)$ (used in SPICE)

$\gamma = (2qN_A\varepsilon_s)^{1/2}/C_{ox}$ (volts$^{1/2}$)

ε_s = Si dielectric constant = $11.7\varepsilon_0$

Assignment #4

Problems:

3.115

3.120

4.17

4.23

4.33

Ex 4.2 NMOS $L = 0.8\,\mu m$ $t = 15\,nm$ $\mu_n = 550\,cm^2/V.s$ $\frac{W}{L} = 20$

For $i_D)_{SAT} = 0.2\,mA$, find C_{ox}, k_n', V_{ov}, & min v_{DS}

$$C_{ox} = \frac{34.5\,pF/m}{15\times10^{-9}\,m} = 2.3\times10^{-3}\,F/m^2 = 2.3\times10^{-15}\,F/\mu m^2 = 2.3\,fF/\mu m^2$$

(p.243)

$$k_n' = \mu_n C_{ox} = 550\times10^{-4}\,m^2/V.s \times 2.3\times10^{-3}\,F/m^2 = 1265\times10^{-7}\,F/V.s = 126.5\,\mu A/V^2$$

$[F] = [Q]/[V] = [I][T]/[V]$

$Q = CV$

So $F/V.s \rightarrow A.s/V.V.s = A/V^2$

$V_{ov} = V_{gs} - V_t$ for $I = 0.2\,mA$ in sat.^{n} $\rightarrow$ $i_D = \frac{1}{2} k_n' \frac{W}{L} (v_{gs} - V_t)^2$

ie. $V_{ov} = \left[\frac{2 i_D}{k_n'(\frac{W}{L})}\right]^{1/2} = \left(\frac{2\times2\times10^{-4}}{126.5\times10^{-6}\times20}\right)^{1/2} \approx \frac{2\times10^{-2}}{5\times10^{-2}}$

$\leq 0.4\,V$

For saturation $v_{DS} \geq v_{gs} - V_t = V_{ov}$ $\therefore$ Min $v_{DS} = 0.4\,V$.

Ex 4.4 NMOS $V_t = 0.7V$ $V_{GS} = 1.5V$

(a) $V_{DS} = 0.5V$ $\therefore$ $V_{GS} - V_{DS} = 1.5V - 0.5V = 1.0V > V_t$ $\therefore$ Triode region

(b) $V_{DS} = 0.9V$ $\therefore$ $V_{GS} - V_{DS} = 1.5V - 0.9V = 0.6V < V_t$ $\therefore$ Saturation

(c) $V_{DS} = 3V$ $\therefore$ $V_{GS} - V_{DS} = 1.5V - 3V = -1.5V < V_t$ $\therefore$ Saturation

Ex 4.5 For MOSFET in Ex 4.4 with $\mu_n C_{ox} = 100\mu A/V^2$

$W = 10\mu m$ $L = 1\mu m$

$$\mu_n C_{ox} \frac{W}{L} = 100 \times 10^{-6} \times \frac{10}{1} = 10^3 \mu A/V^2 = 1mA/V^2$$

(a) $I_D = \mu_n C_{ox} \frac{W}{L} \left[(V_{GS} - V_t) V_{DS} - V_{DS}^2/2 \right] = 1{,}000\mu A \left[(0.8 \times 0.5) - .5^2/2 \right] = 275\mu A$

(b) $I_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_t)^2 = 500\mu A \, (.8)^2 = 320\mu A$

(c) " " " = " = $320\mu A$

Ex 4.6 $V_t = 0.7\text{V}$ $i_D = 100\mu\text{A}$ at $v_{GS} = v_{DS} = 1.2\text{volt}$ (i.e. in saturation)

$$\therefore 100\mu\text{A} = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(v_{GS}-V_t)^2 = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(1.2-.7)^2$$

$$\therefore \mu_n C_{ox}\frac{W}{L} = \frac{200\mu\text{A}/\text{V}^2}{(0.5)^2} = 800\mu\text{A}/\text{V}^2$$

$$\left.\begin{array}{l} \therefore v_{GS} = 1.5 \\ v_{DS} = 3\text{V} \end{array}\right\} \longrightarrow v_G - v_D = -1.5 < V_t \quad \therefore \text{Saturation}$$

$$\therefore i_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(v_{GS}-V_t)^2 = 400\mu\text{A}(.8)^2 = 256\,\mu\text{A}$$

$$\left.\begin{array}{l} v_{GS} = 3.2\text{V} \\ v_{DS} \text{ small} \end{array}\right\} r_{DS} \approx \frac{1}{k_n'\frac{W}{L}V_{OV}} = \frac{1}{(800\times10^{-6})(3.2-0.7)} = \frac{10^6}{2.5\times800} = 500\,\Omega$$

$$r_o = \left[\frac{\partial i_D}{\partial v_{DS}}\right]^{-1} = \left[\frac{\partial}{\partial v_{DS}}\left(\frac{1}{2}k_n'\frac{W}{L}(v_{GS}-V_t)^2(1+\lambda v_{DS})\right)\right]^{-1}$$

$$= \left[\frac{\lambda}{2}k_n'\frac{W}{L}(v_{GS}-V_t)^2\right]^{-1} = \frac{1}{\lambda I_D}$$

I_D without channel length modulation

Ex 4.8 PMOS $V_t = -1V$ $k_p' = 60\mu A/V^2$ $W/L = 10$

(a) $V_{gs} < V_t \therefore V_g < V_t + V_s = -1V + 5V$, i.e. conducts for $V_g < +4V$

(b) Triode region $V_g - V_D \leq V_t$, i.e. $V_D \geq V_g - V_t = V_g + 1V$

(c) Saturation — following (b) $V_D \leq V_g + 1V$

(d) Saturation:

$$i_D = 75\mu A = \frac{1}{2} k_p' \frac{W}{L} (V_{ov})^2$$

$$= \tfrac{1}{2}\, 60\mu A \cdot 10 (V_{ov})^2$$

$$\therefore V_{ov} = \left(\frac{150}{600}\right)^{1/2} = 0.5V$$

$$\therefore V_{gs} = -V_{ov} + V_t$$

$$= -0.5 + (-1) = -1.5V$$

$$\therefore V_g = V_s + V_{gs}$$

$$= +5V - 1.5V = 3.5V$$

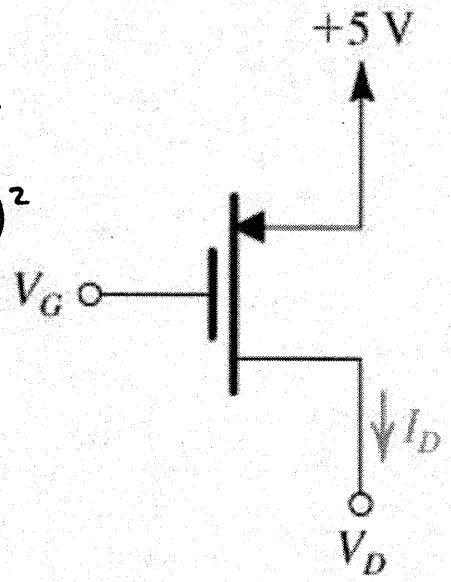


Figure E4.8

(e) $\lambda = -0.02/V \therefore r_o = 1/\lambda I_D$

$$i_D = \tfrac{1}{2} k_p' \frac{W}{L} (V_{ov})^2$$

$$= \tfrac{1}{2}\, 60\mu A\ 10\ (.5)^2 = 75\mu A$$

$$\therefore r_o = \frac{1}{.02 \times 75\mu A} = \frac{10^6}{1.5} = \frac{2}{3} M\Omega$$

(f) I_D at $V_D = +3V, 0V$ (Saturation check above)

$$I_D(3V) = \tfrac{1}{2} k_p' \frac{W}{L} (V_{ov})^2 (1 + \lambda V_{DS})$$

$$= 300\mu A\,(.5)^2 (1 - 0.02 \times (3-5))$$

$$= 300\mu A\,(.25)(1.04)$$

$$= 78\mu A$$

$$I_D(0V) = 300\mu A\,(.25)(1 - .02(-5))$$

$$= 82.5\mu A$$

$$\therefore -\frac{\Delta V}{\Delta I} = -\frac{(3-0)V}{(78-82.5)\times 10^{-6} A}$$

$$= \frac{3 \times 10^6}{4.5} = \frac{2}{3} M\Omega$$

(same as in (e))