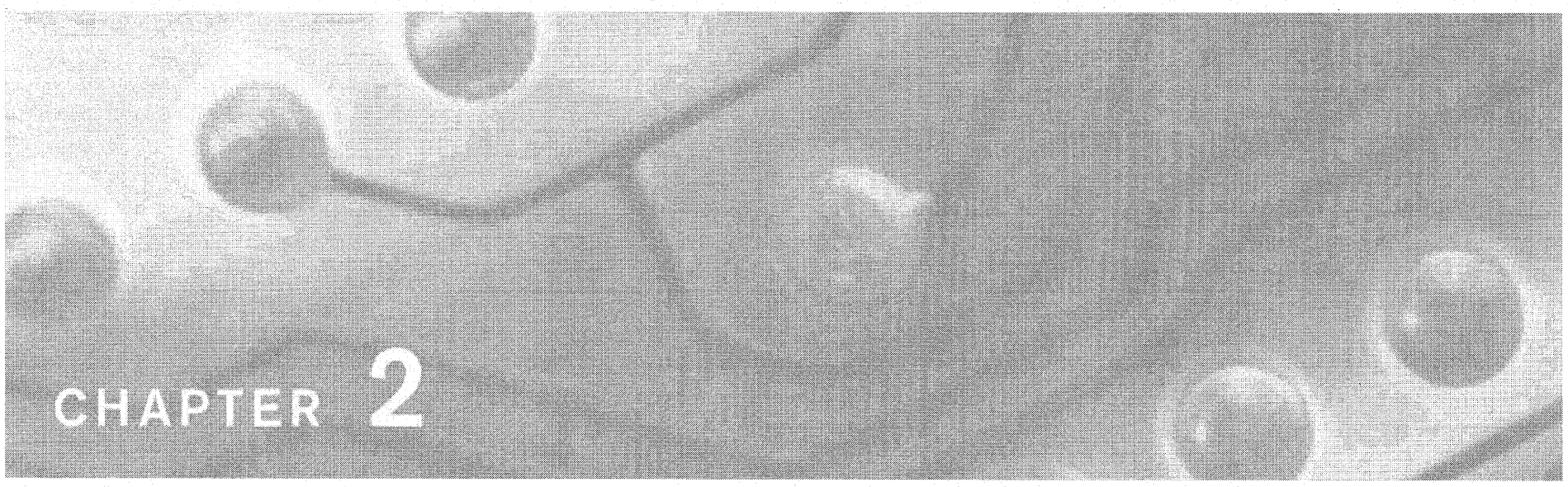
ECE321 Electronics I
Fall 2006

Professor James E. Morris

Lecture 4

5th October, 2006



Operational Amplifiers (Real)

2.7 DC Imperfections { Offset voltage/current; Bias current

2.8 Integration & Differentiation

2.9 SPICE ← OpAmp models

Offset Voltage

1. Origins
2. Typically ±mV
3. Temperature dependence (±μV/°C)
4. SC input → Output voltage
5. May saturate
6. Represent by V_{os}. (conventionally in V^+ input lead)

$$V_o = A V_{os}$$

7. Can zero out the output voltage by adding an input source, opposite to effective V_{os}

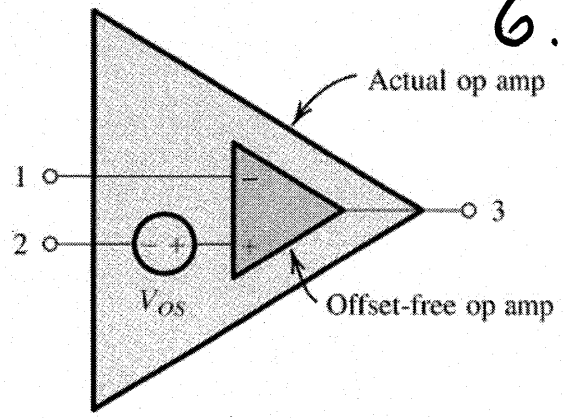
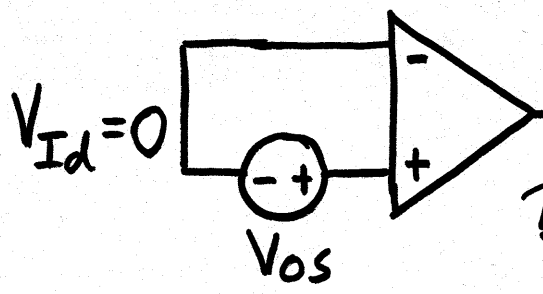


Figure 2.28 Circuit model for an op amp with input offset voltage V_{OS}.

Ex. 2.23 Sketch V_o vs V_{Id} for $A_o = 10^4$, $V_{os} = +5mV$, $V_{SAT} = \pm 10V$

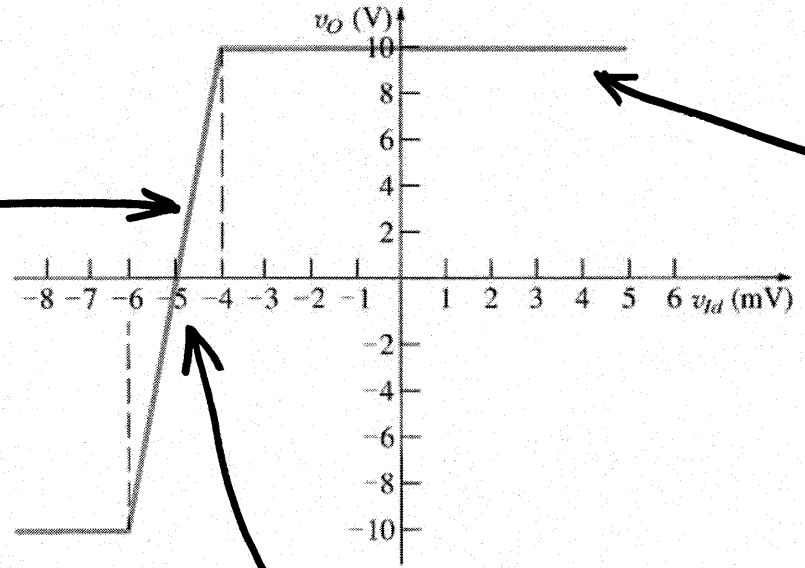
Ex 2.23



$V_o = A_o V_{os} = 10^4 \times 5mV \rightarrow 50V$

But saturates at $\pm 10V$

To offset $V_{os} = 5mV$, need $V_{Id} = -5mV$. Then $V_o = 0$



Gain $10^4 V/V$ ie. $10V/mV$

Saturates $\pm 10V$

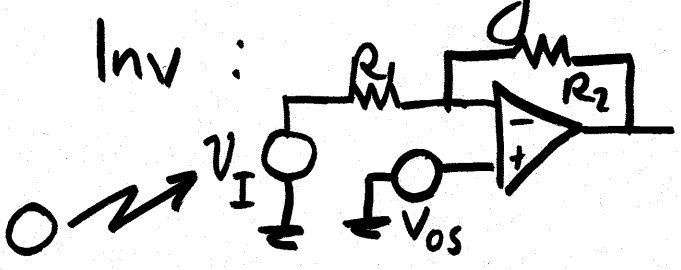
V_{Id} for $V_o = 0$

Figure E2.23 Transfer characteristic of an op amp with $V_{OS} = 5$ mV.

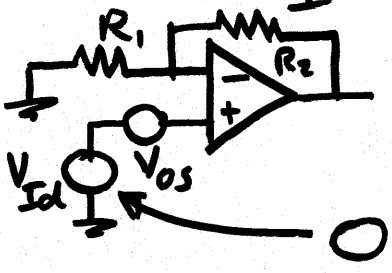
Effect of V_{os} on OpAmp Circuits

Superposition: Could consider V_{os} and V_I separately.
Only interested in V_{os} here, so set $V_I = 0$

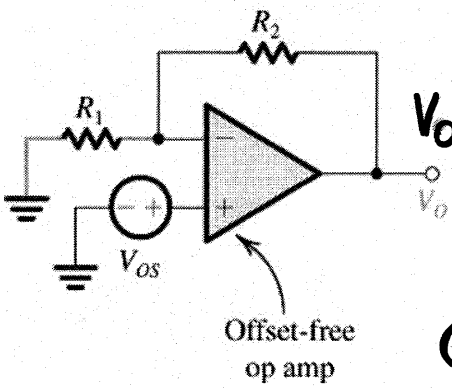
Inv:



Non-Inv:



This circuit covers both →



DC

$$V_O = V_{os}\left(1 + \frac{R_2}{R_1}\right)$$

For high gain, V_o may sat.

Or say $R_2 = 100R_1$, $V_{os} \sim 10mV$

DC $V_o = 1.001v$, and ac signal (or dc variation) about this average/dc value.

May limit signal swing

V_o due to V_{os}

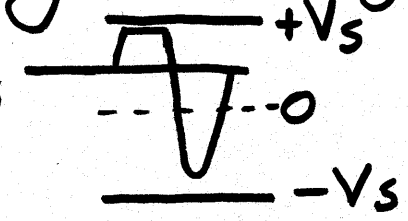
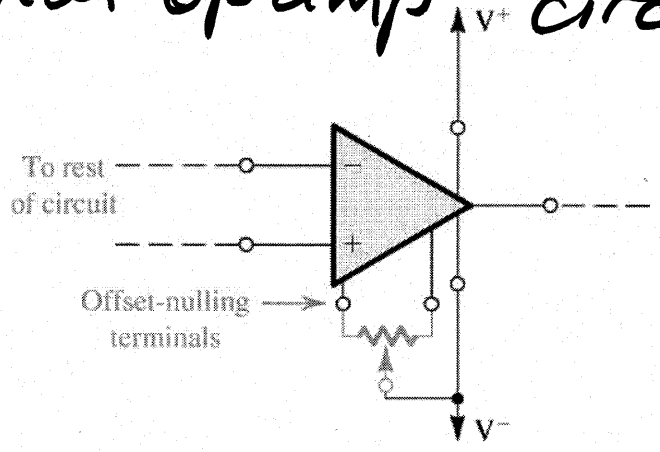


Figure 2.29 Evaluating the output dc offset voltage due to V_{OS} in a closed-loop amplifier.

Solution #1 : Offset null terminals

Pot connects to internal circuitry

Draws zero current at midpoint, or "balancing" current from one side or the other of the internal op amp circuitry.



Manually zero out! (Not good for low cost mass production)

Even at room temperature balance, thermal effects renew offset at other temperatures.

Figure 2.30 The output dc offset voltage of an op amp can be trimmed to zero by connecting a potentiometer to the two offset-nulling terminals. The wiper of the potentiometer is connected to the negative supply of the op amp.

Ex 2.24. Inv amp^r, gain $\equiv 1000$

$V_{os} = 3mV \quad V_{SAT} = \pm 10V$

(a) Find peak sinewave without clipping

$V_{os} \rightarrow V_o = -1000 \times 3mV = -3V$ $\therefore$ Min "distance" to $\pm 10V = 7V$

$\therefore$ Max input $V_m = 7V/1000 = 7mV$

(b) V_{os} nulled out at room temperature (RT) ie. 25°C

(i) Max input at RT? $10V/1000 = 10mV$

(ii) Max imput for 0-75°C temperature variations

if V_{os} temp. coeff. $= 10\mu V/°C$

Max $\Delta T = 75-25 = 50°C$ $\therefore \Delta V_{os} = 10 \times 10^{-6} V/°C \times 50°C$

$= 500\mu V = 0.5mV$

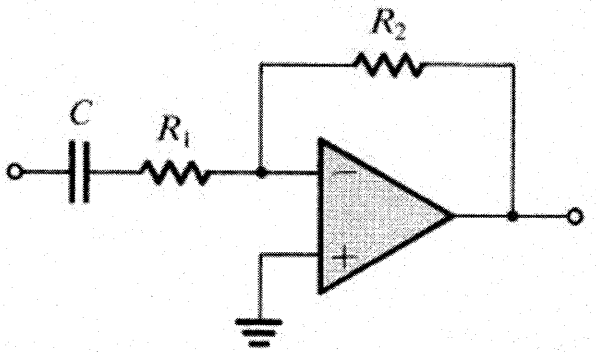
$\therefore V_o$ at $75°C = 0.5mV \times 1000 = 0.5V$

$\therefore$ Max input $V_m = 9.5mV \quad (9.5V/1000)$

Solution #2 Capacitor coupling: See ckt.

Only for ac signals v_i above the 3dB frequency

$f_L = 1/2\pi R_1 C$



(a)

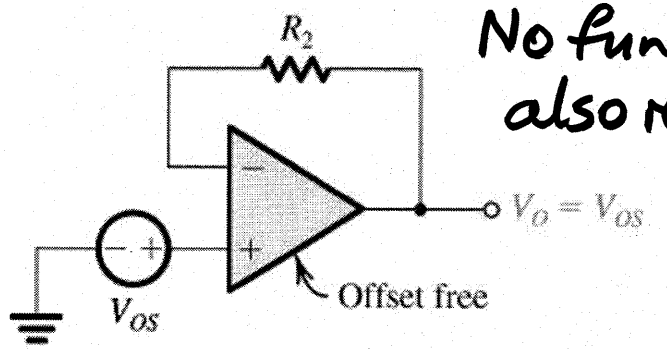
Blocks dc, $X_C \xrightarrow[f \to 0]{} \infty$

$\therefore$ DC gain $\to 0$

So —

For dc, replace C by open circuit (OC)

So R_1 has no dc current. No function, also remove



(b)

This circuit is now clearly a Voltage Follower (no current in R_2)

$\therefore$ $V_o = V_{os}$

Figure 2.31 **(a)** A capacitively coupled inverting amplifier, and **(b)** the equivalent circuit for determining its dc output offset voltage V_O.

Capac coupling → Eliminates the amplification of dc V_{os}.

Ex 2.25 Circuit as for Ex 2.24 (Gain = −1000, V_{os} = 3mV) but now capacitively couple.

(a) $V_o = 3mV$, ∴ Output swing to sat = 9.997V

∴ Max input $V_M = 9.997mV \approx 10mV$

(So no need for offset trimming)

(b) $R_1 = 1K\Omega$ $R_2 = 1M\Omega$, find C_1 for gain > 57dB down to 100Hz

ie. 3dB point at 100Hz (60dB for $f \gg 100Hz$)

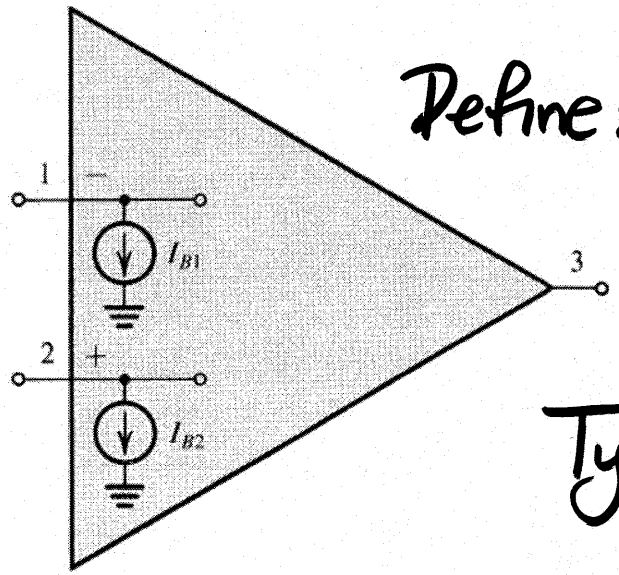
$$f_L = \frac{1}{2\pi R_1 C_1} \quad \therefore C_1 = \frac{1}{2\pi f_L R_1} = \frac{1}{2\pi\, 100\, 10^3}$$

$$\approx 1.6\mu F$$

Input Bias & Offset Currents

BJT OpAmps draw input bias currents, i.e. DC.
(Not related to v_I signal magnitudes)
MOSFET OpAmps draw much less.

Represent by
I_{B1}, I_{B2}



Define: Bias $I_B = \frac{I_{B1} + I_{B2}}{2}$

Offset $I_{OS} = |I_{B1} - I_{B2}|$

In general
$I_{B1} \neq I_{B2}$
(internal component differences)

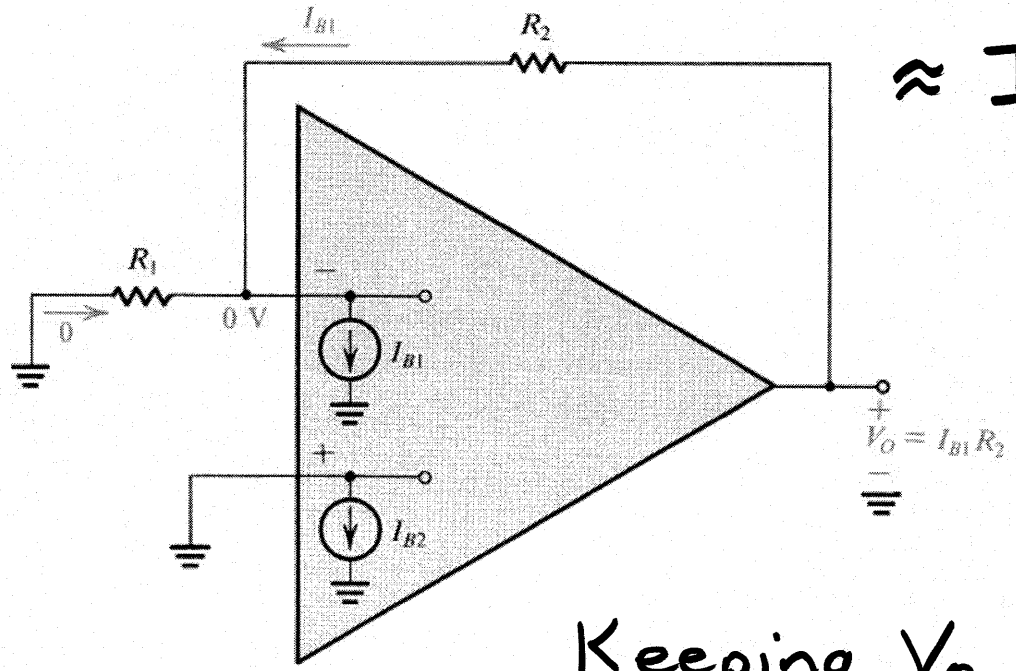
Typical values (BJT)
$I_B \sim 100\,nA$
$I_{OS} \sim 10\,nA$

Figure 2.32 The op-amp input bias currents represented by two current sources I_{B1} and I_{B2}.

Superposition: Consider I_B & I_{OS} separately.

Effect of I_B

$v^- = v^+ = 0\,V$ } $\therefore I_{R2} = I_{B1}$
so $I_{R1} = 0\,A$ } & $V_o = I_{B1} R_2$
$\approx I_B R_2$

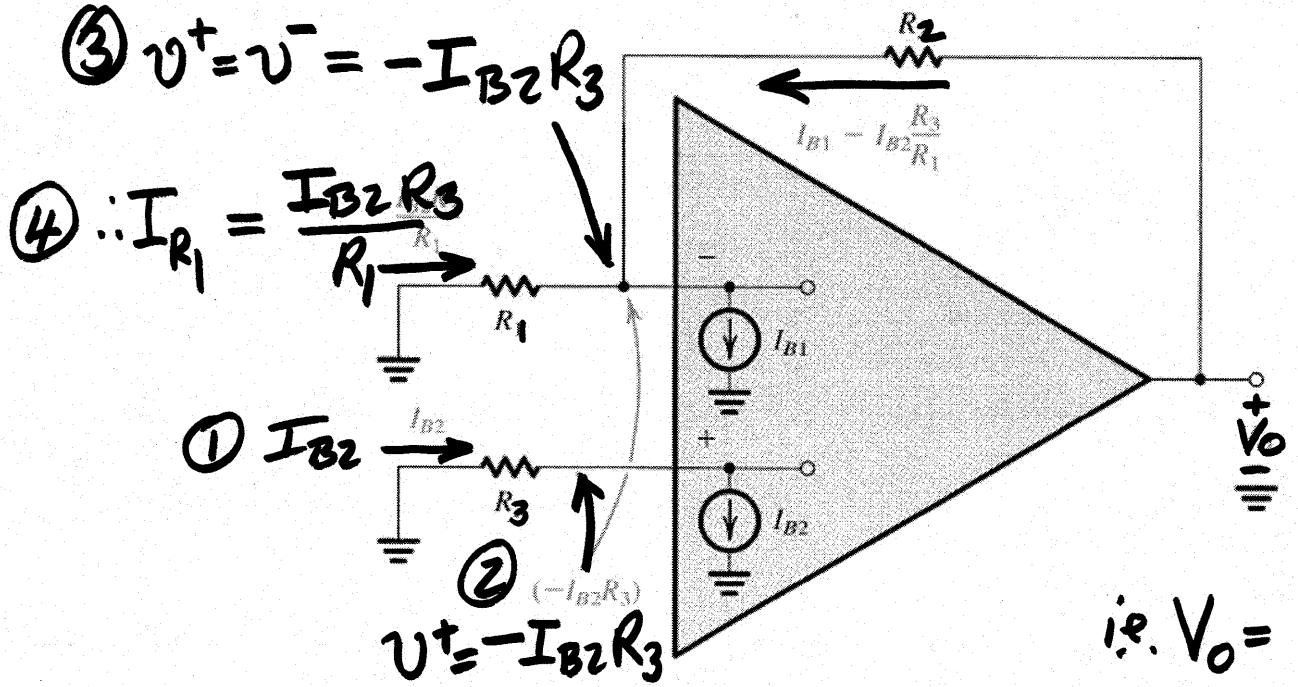


Keeping V_o down may limit R_2 and hence limits gain for specified (non-inv) $R_{in} = R_1$.

Figure 2.33 Analysis of the closed-loop amplifier, taking into account the input bias currents.

Solution

Add R_3



⑤ $\therefore I_{R2} = I_{B1} - I_{B2}\frac{R_3}{R_1}$

③ $v^+ = v^- = -I_{B2}R_3$

④ $\therefore I_{R_1} = \frac{I_{B2}R_3}{R_1}$

① I_{B2}

② $v^+ = -I_{B2}R_3$

⑥ $\therefore$

$V_o = V^- + I_{R2}R_2$

i.e. $V_o = -I_{B2}R_3 + R_2\left(I_{B1} - I_{B2}\frac{R_3}{R_1}\right)$

$= I_{B1}R_2 - I_{B2}R_3\left(1 + \frac{R_2}{R_1}\right)$

Figure 2.34 Reducing the effect of the input bias currents by introducing a resistor R_3.

Bias Current: Assume $I_{B1} = I_{B2} = I_B$, then $V_o \to 0$ if $R_2 = R_3(1 + R_2/R_1)$

i.e. if $R_3 = \frac{R_1R_2}{R_1 + R_2} = R_1 /\!/ R_2$

Offset Current: Check the effect of R_3 on I_{os}

Previous result: $V_o = I_{B1} R_2 - I_{B2} R_3 \left(1 + \frac{R_2}{R_1}\right)$

Set $I_{B1} = I_B + I_{os}/2$

$I_{B2} = I_B - I_{os}/2$

$\therefore V_o = (I_B + I_{os}/2) R_2 - (I_B - I_{os}/2) R_3 (1 + R_2/R_1)$

$= (I_B + I_{os}/2) R_2 - (I_B - I_{os}/2) \frac{R_1 R_2}{R_1 + R_2} \cdot \frac{R_1 + R_2}{R_1}$

$= (I_B R_2 - I_B R_2) + \frac{I_{os}}{2} (R_2 + R_2)$

$= I_{os} R_2$

Note: Must make R_3 in the "+" input lead equal to the DC resistance seen at the "−" input lead, i.e. $R_1 /\!/ R_2$ above

BUT $R_3 = R_2$ here, because DC impedance of R_1 & C $\rightarrow \infty$.

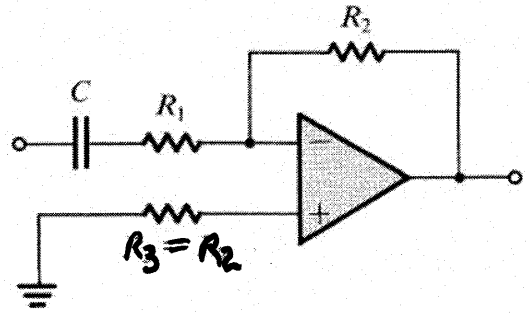
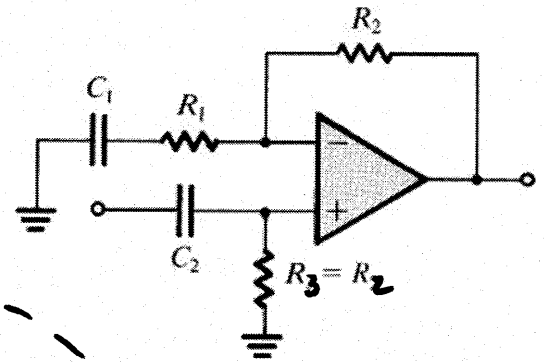


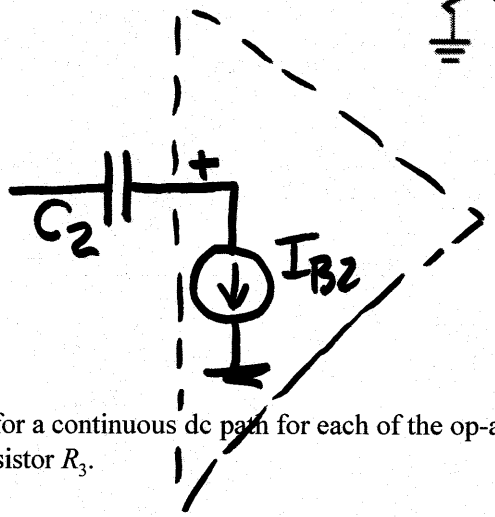
Figure 2.35 In an ac-coupled amplifier the dc resistance seen by the inverting terminal is R_2; hence R_3 is chosen equal to R_2.

Also: Always need a DC path to ground.

If AC couple v_I to v^+ through C_2, then need R_3 as shown to avoid C_2 charging



Without R_3



I_{B2} charges C_2, v^+ rises as $\frac{dv^+}{dt} = -I_{B2}/C_2$ & output saturates.

Figure 2.36 Illustrating the need for a continuous dc path for each of the op-amp input terminals. Specifically, note that the amplifier will *not* work without resistor R_3.

Ex. 2.26 Inv amp: → opamp & $R_1 = 10K\Omega$, $R_2 = 1M\Omega$

$I_B = 100nA$ $I_{os} = 10nA$

$$V_o = I_{B1} R_2 = \left(I_B + \frac{I_{os}}{2}\right) R_2 = 105nA \times 1M\Omega = 0.105V$$

Note: Text uses the approx value I_B

Actually, sign of I_{os} is not determined, so result COULD be 0.095v for $I_B - I_{os}/2$, so 0.1v might be the better answer. (0.105v is the MAX V_o!)

So need $R_3 = 10K \| 1M = \frac{1 \times 100}{1+100} 10K = 9.9K$ (use 10K)

Then $V_o = I_{os} R_2 = 0.01v$

Example 2.6

$$\frac{V_o}{V_i} = -\frac{1}{Y_2 Z_1} = \frac{-1}{R_1\left(1/R_2 + sC_2\right)} = \frac{-R_2/R_1}{1 + s R_2 C_2}$$

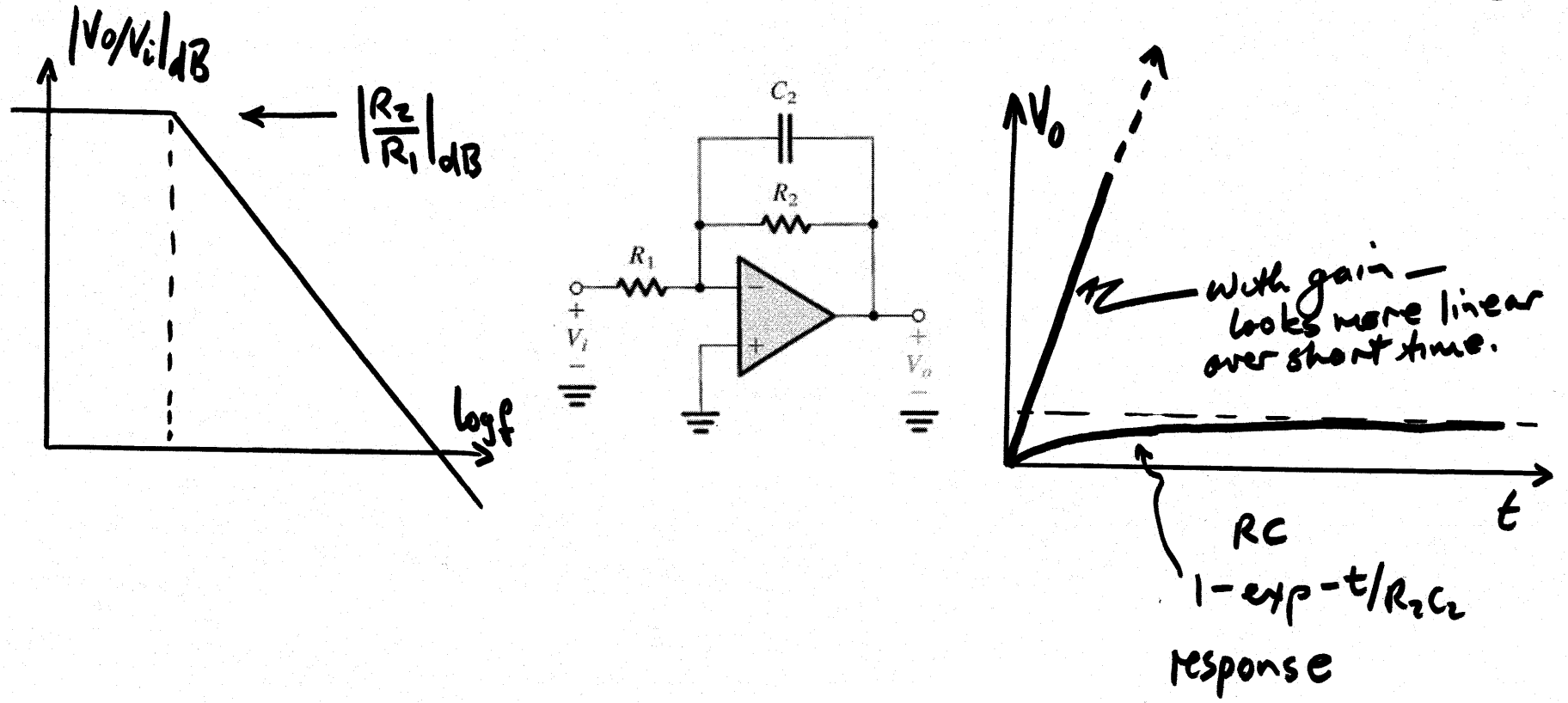
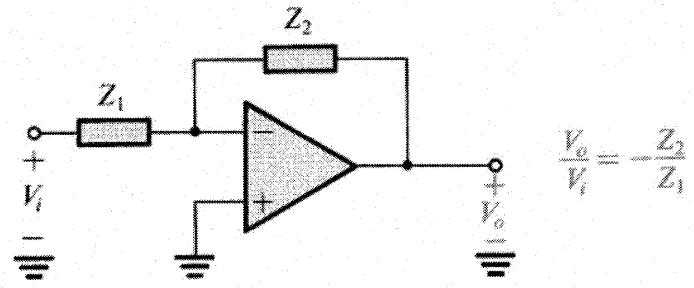


Figure 2.38 Circuit for Example 2.6.

Integration & Differentiation

$$\frac{V_o}{V_i} = -\frac{Z_2}{Z_1}$$



We are now looking at the time domain responses, having considered the frequency domain. Compare STC R-C circuits, frequency and time responses.

Figure 2.37 The inverting configuration with general impedances in the feedback and the feed-in paths.

Inverting (Miller) Integrator

$$\frac{V_o}{V_i} = -\frac{1/sC}{R} = \frac{-1}{sRC}$$

Frequency response

$$\phi = \tan^{-1}\frac{\omega RC}{0} = +90^\circ$$

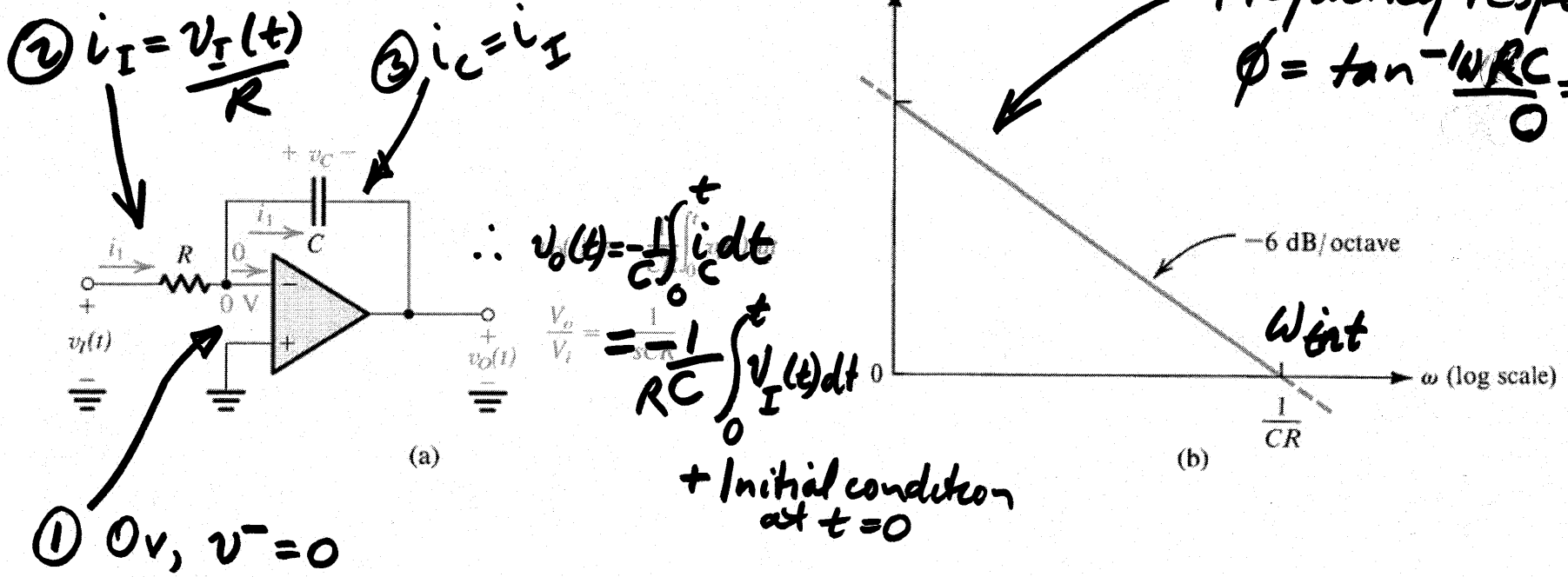


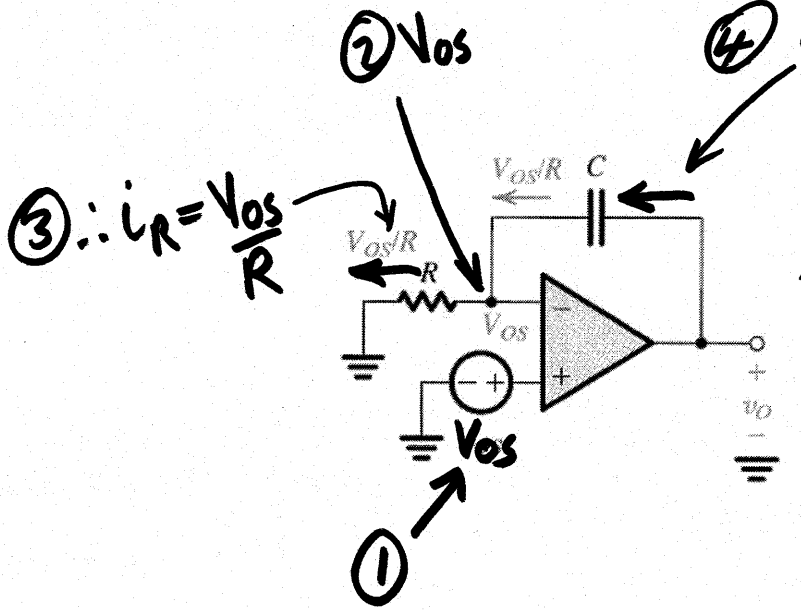
Figure 2.39 **(a)** The Miller or inverting integrator. **(b)** Frequency response of the integrator.

Miller integrator → See also Miller's theorem.
Relates to negative (capacitive) feedback

Integrator is a LP filter with $\omega_{dB} = 0$

No DC feedback

V_{os} effect:



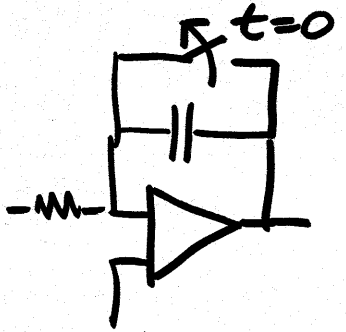
⑤ $\therefore$

$$v_O = V_{os} + \frac{1}{C}\int_0^t \frac{V_{os}}{R}\,dt = V_{os} + \frac{V_{os}}{RC}t$$

Initial DC condition

If $V_c(0) = 0$

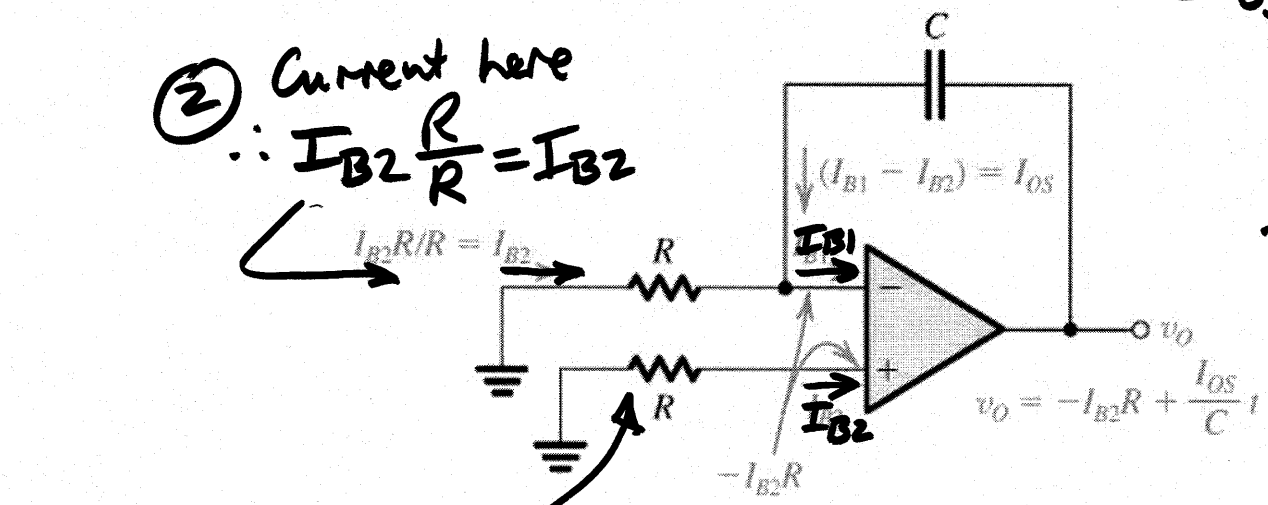
$V_o(0) = V_{os}$



Typical initial condition circuit

Figure 2.40 Determining the effect of the op-amp input offset voltage V_{OS} on the Miller integrator circuit. Note that since the output rises with time, the op amp eventually saturates.

I_{B1}, I_{OS} effects



② Current here
$\therefore I_{B2}\frac{R}{R} = I_{B2}$

③ $\therefore I_C = I_{B1} - I_{B2}$
$= I_{OS}$

④ $\therefore V_o = -I_{B2}R + \frac{I_{OS}}{C}t$

i.e. rises to saturation

① $v^- = v^+ = -I_{B2}R$

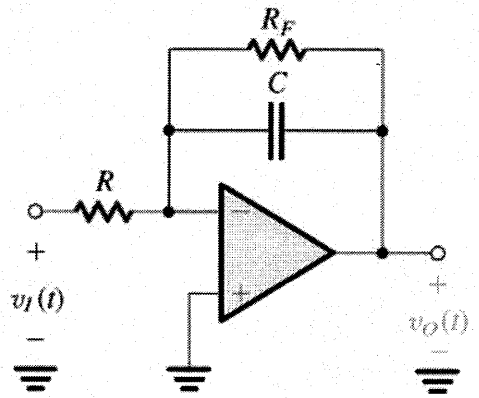
This R is $R \| \infty$ for DC
Compare R_3

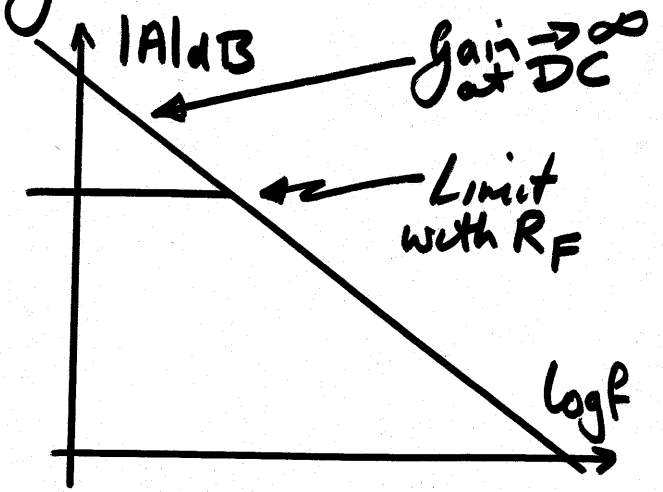
Figure 2.41 Effect of the op-amp input bias and offset currents on the performance of the Miller integrator circuit.

Solution;

Must add negative feedback for DC

→ finite DC gain





Operate at frequencies $> \frac{1}{2\pi R_F C}$

$$V_o)_{DC} = I_{os}R_F + V_{os}\left[1 + \frac{R_F}{R}\right]$$

Figure 2.42 The Miller integrator with a large resistance R_F connected in parallel with C in order to provide negative feedback and hence finite gain at dc.

Example 2.7

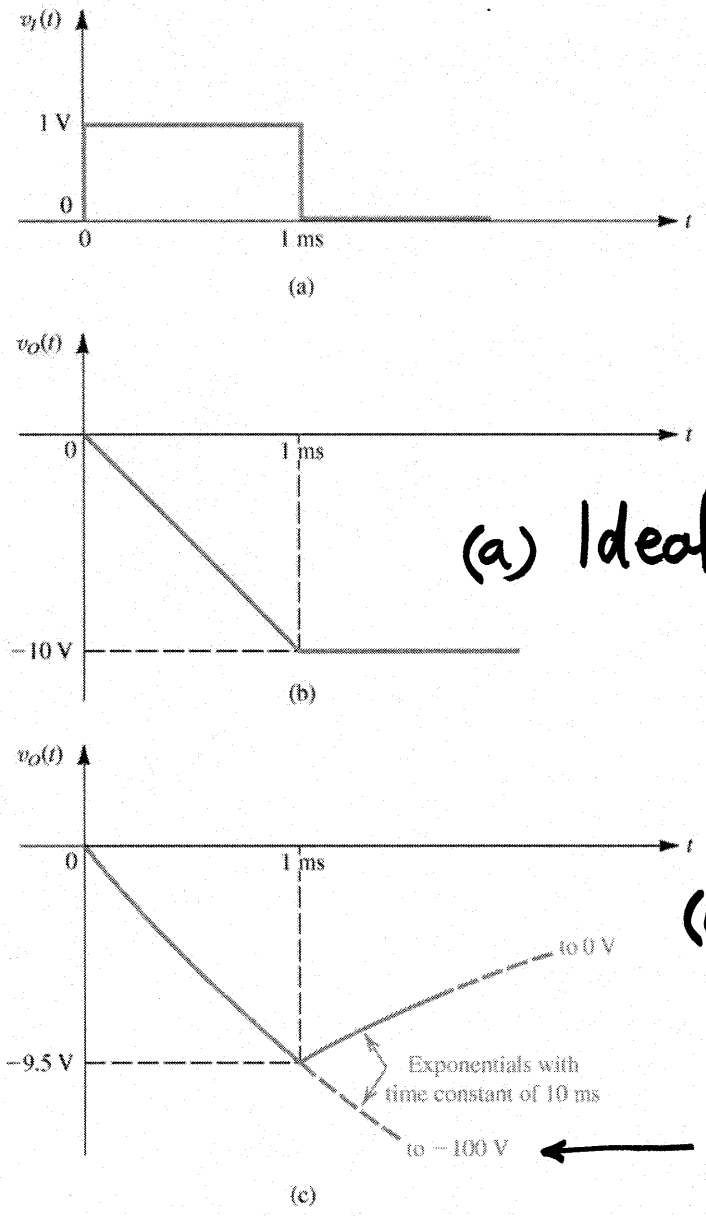
(a) $R = 10K$

$C = 10nF$

$\therefore RC = 10^{-4}s$

(b) $R_F = 1M\Omega$

$R_F C = 10ms$



(a) Ideal $-\frac{1}{C}\int_0^t \frac{V_I}{R}\,dt$

(b)

DC gain $-\frac{10^6}{10^4} = -100$

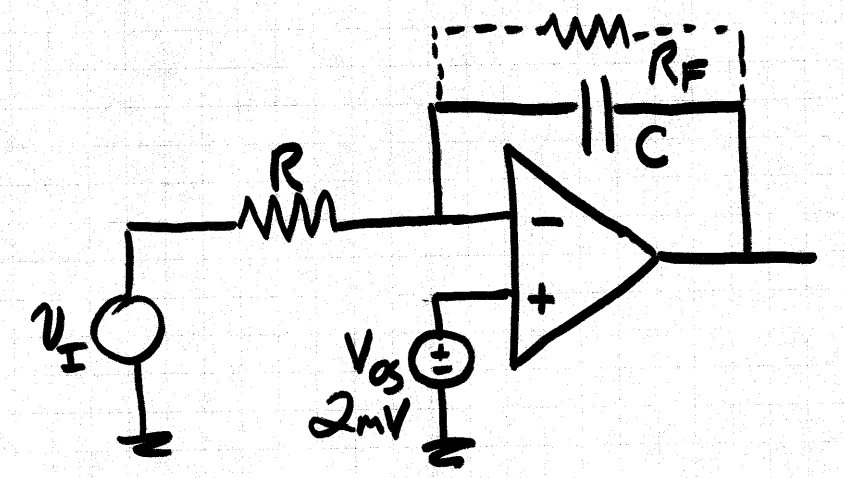
Figure 2.43 Waveforms for Example 2.7: **(a)** Input pulse. **(b)** Output linear ramp of ideal integrator with time constant of 0.1 ms. **(c)** Output exponential ramp with resistor R_F connected across integrator capacitor.

Ex 2.29

$\tau = 1ms$

$R_{id} = 10K$

$V_{sat} = \pm 12v$



$R = 10K$

& $C = \frac{10^{-3}s}{10^4\Omega} = 10^{-7}F = 0.1\mu F$

(a) $V_c(0) = 0$, time to saturation?

(b) Find max R_F so at least $\pm 10v$ output swing available

Corner freq?

(a) $v_0 = V_{os} + \frac{V_{os}}{RC}t$, so saturation

$12 = 2\times10^{-3} + \frac{2\times10^{-3}}{10^{-3}}t$

$\therefore t \approx 6$ sec.

(b) Retain 10v swing $\therefore V_0]_{max} = 2v$

$\therefore V_{os}(1 + R_F/R) + I_{os}R_F = 2v$ $\therefore R_F = R\left(\frac{2v}{2mV} - 1\right)$

$\approx 10^4 \times 10^3$

$= 10M\Omega$

↑ 0

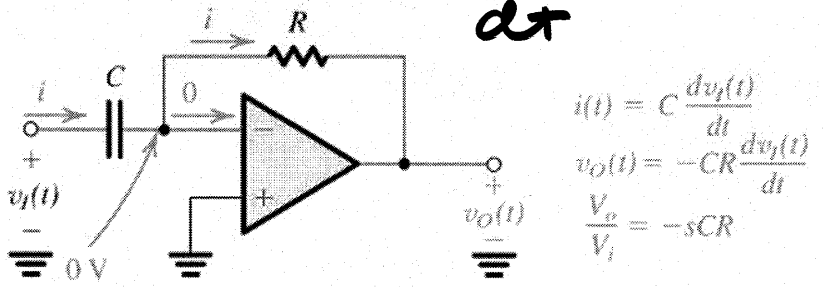
& $\omega_c = \frac{1}{R_F C} = 1/10^7\times10^{-7} = 1$ $\therefore f = \frac{1}{2\pi} = 0.16Hz$

Differentiator

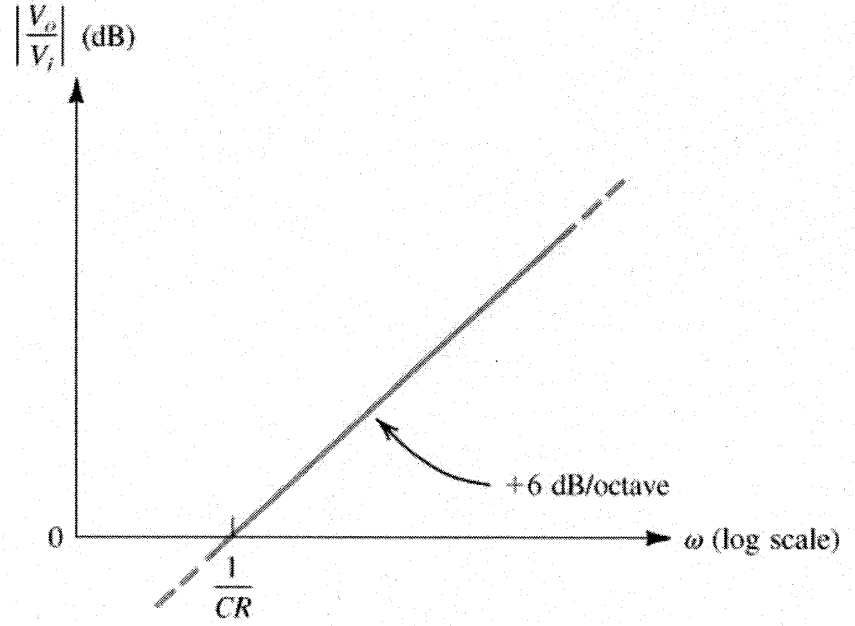
$$\frac{V_o}{V_i} = -\frac{R}{(j\omega C)^{-1}} = -j\omega RC$$

$$i_C = C\frac{dv_I}{dt}$$

$$v_o = -iR = -i_C R = -RC\frac{dv_I}{dt}$$



(a)



(b)

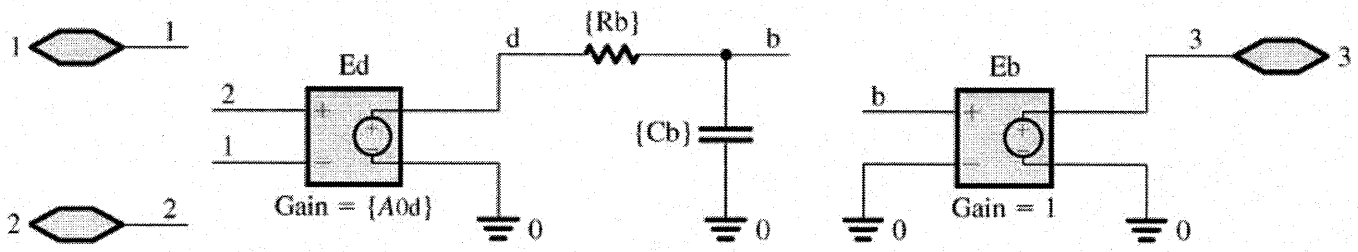
Noise problems! High gain at HF.
∴ Limit gain with R_S in series with C.

Figure 2.44 **(a)** A differentiator. **(b)** Frequency response of a differentiator with a time-constant *CR*.

Op Amp Macromodels

Less components in the model than if include all the opamp internal components.

"Functional" or "empirical" model — fit to terminal characteristics.



Finite gain

HF roll-off

$R_{in} = \infty$ $R_o = 0$ No offsets/bias

Figure 2.45 A linear macromodel used to model the finite gain and bandwidth of an internally compensated op amp.

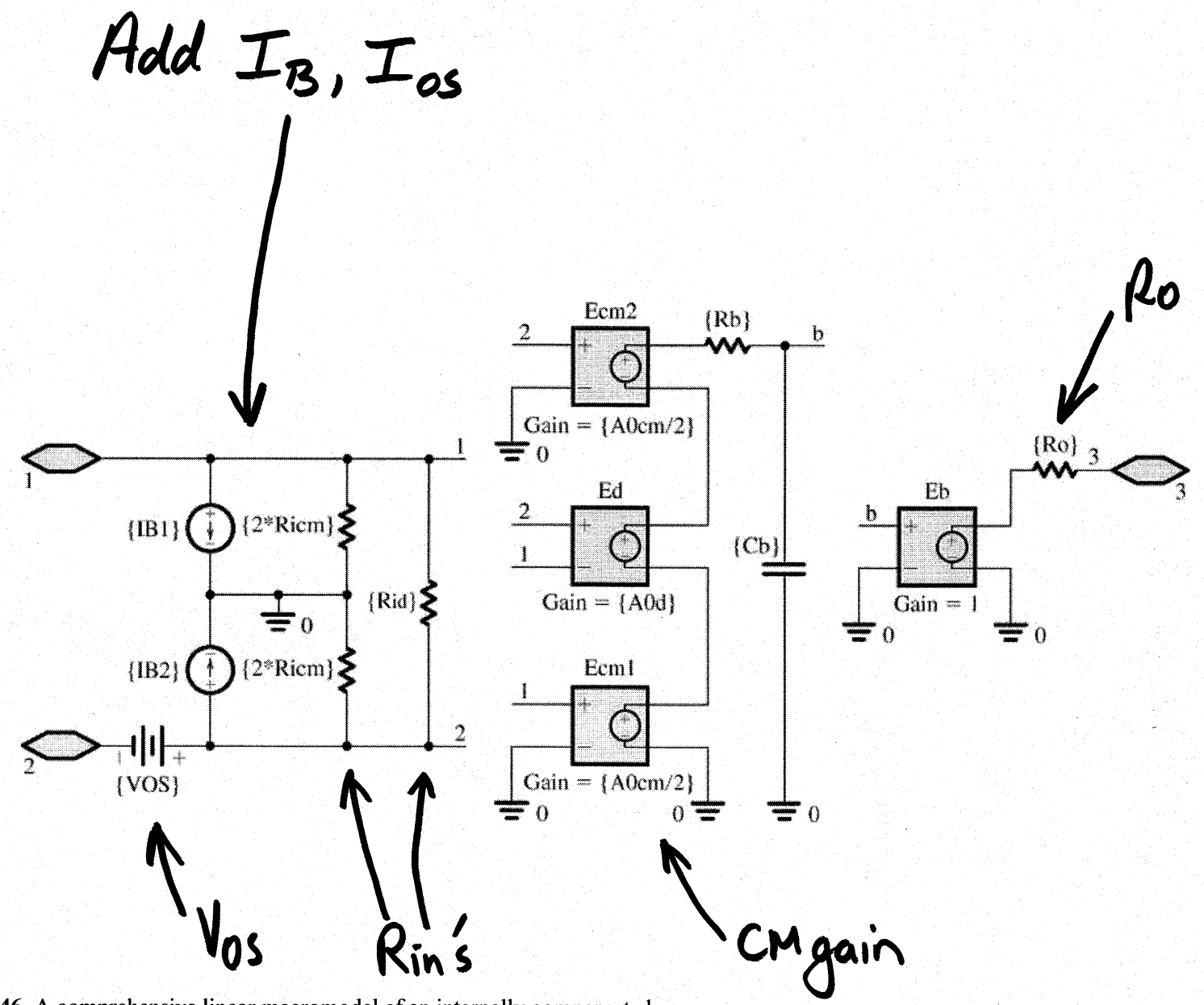


Figure 2.46 A comprehensive linear macromodel of an internally compensated op amp.

Example 2.8

$R_{id} = 2M\Omega$ $V_{os} = 1mV$ $A_0 = 100dB$ (i.e. 10^5)

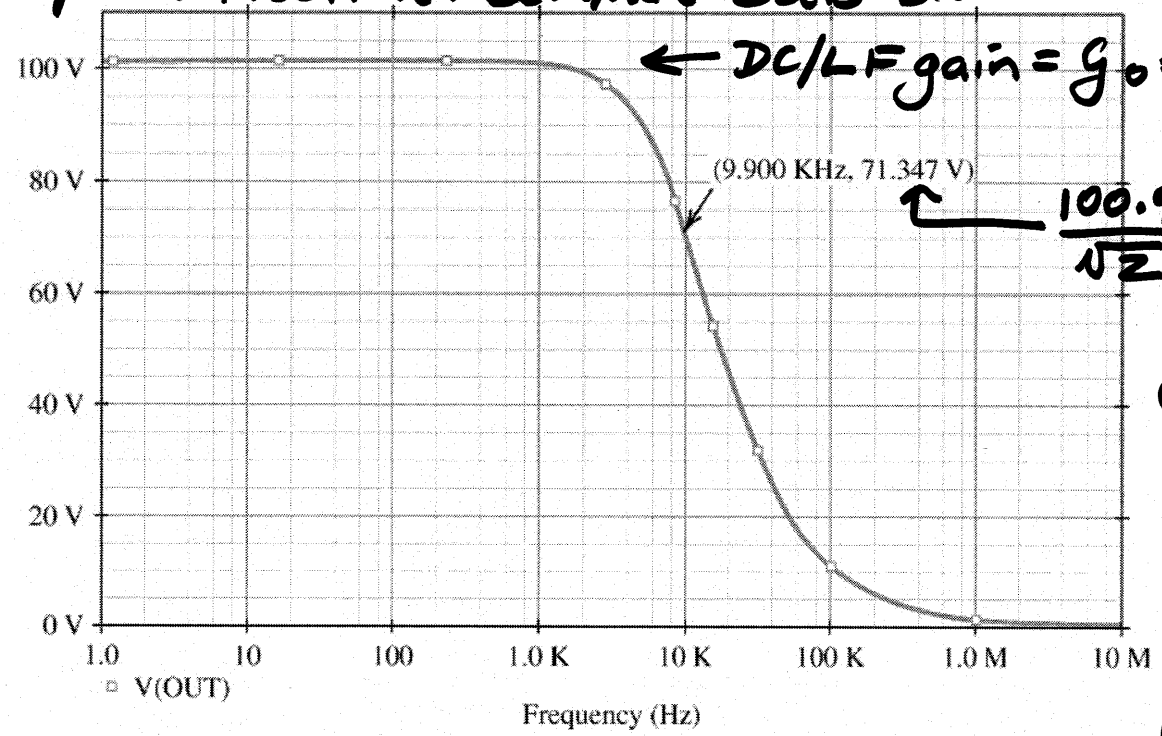
$R_o = 75\Omega$ $f_t = 1MHz$ ← Set $C_b = 1\mu F$, $R_b = 15.915K\Omega$

Assume $I_B = 0$ $I_{os} = 0$

(a) Create subckt

(b) CL non-inv amp: $R_1 = 1K\Omega$ $R_2 = 100K\Omega$. Find (i) 3dB BW (ii) R_{in} (iii) R_{out}

(c) Step response rise time. Compare 3dB BW



← DC/LF gain = $G_0 = 100.9$ (ideal 101)

Response to 1V AC input test voltage

← $\frac{100.9}{\sqrt{2}}$

∴ (i) 9.9KHz

(ii) $R_{in} = \frac{1V}{i_{in}}$ ← test at 0.1Hz (to avoid roll off effects & approx dc.)

$R_{in} = 2G\Omega$

(iii) R_{out} → SC input to ground

Put 1A ac into output; measure V_o

$R_{out} = 76m\Omega$

Figure 2.47 Frequency response of the closed-loop amplifier in Example 2.8.

Note: $R_{in} = 2G\Omega \sim 10^3 R_{id}$

$R_{out} = 76m\Omega \sim R_o/10^3$

} and $10^3 \approx A_0/A_f = (1+A_0\beta)$ General result; see later

Step response

$f_{3dB} = 9.9\text{KHz}$ from (b)(i)

$\tau = \frac{1}{2\pi \, 9.9\times10^{3}} \sim 35\mu s.$

Compare $(37 - 1.7)\mu s$ 10–90%.

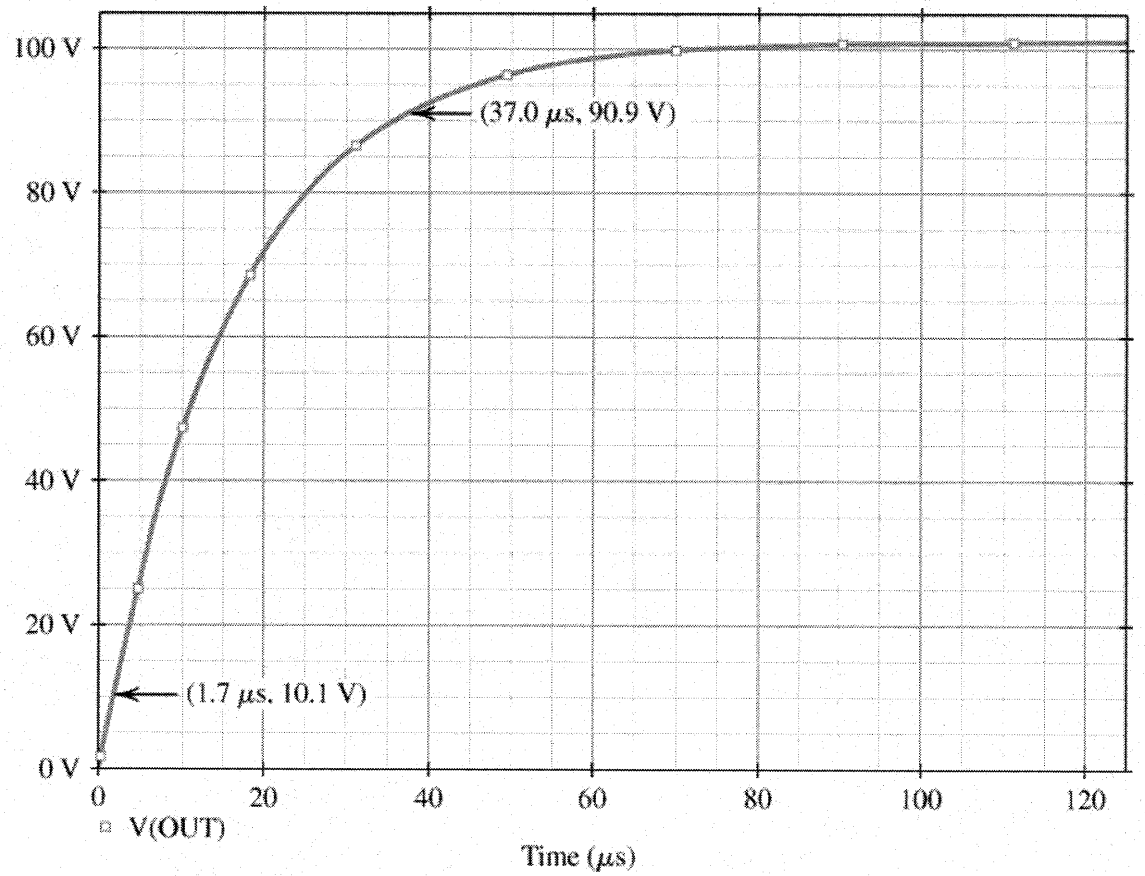


Figure 2.48 Step response of the closed-loop amplifier in Example 2.8.

Non-linear effects
Include the 741 model in PSpice library

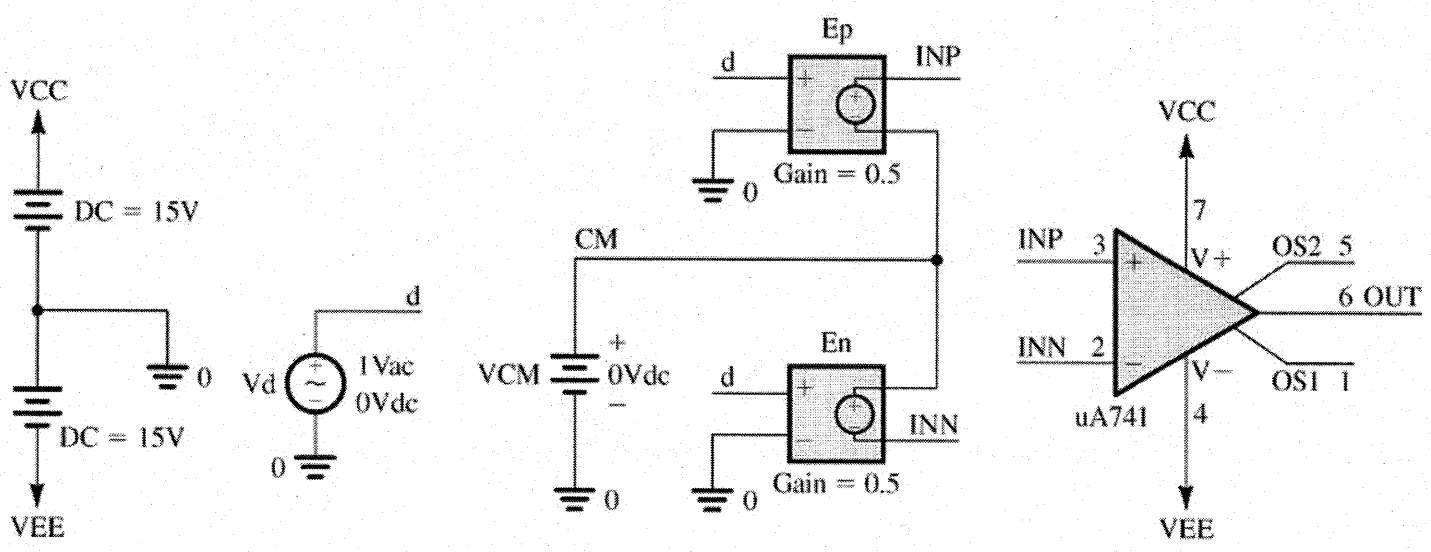


Figure 2.49 Simulating the frequency response of the μA741 op-amp in Example 2.9.

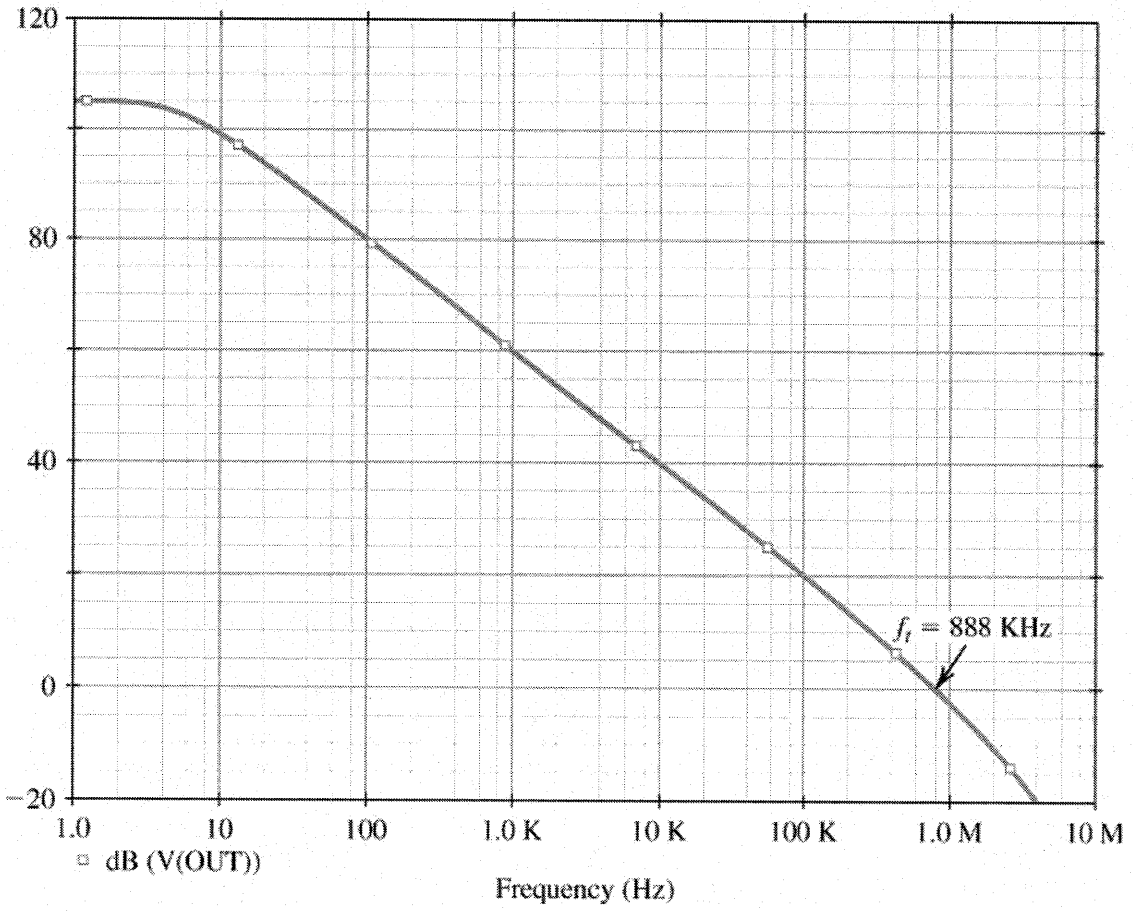
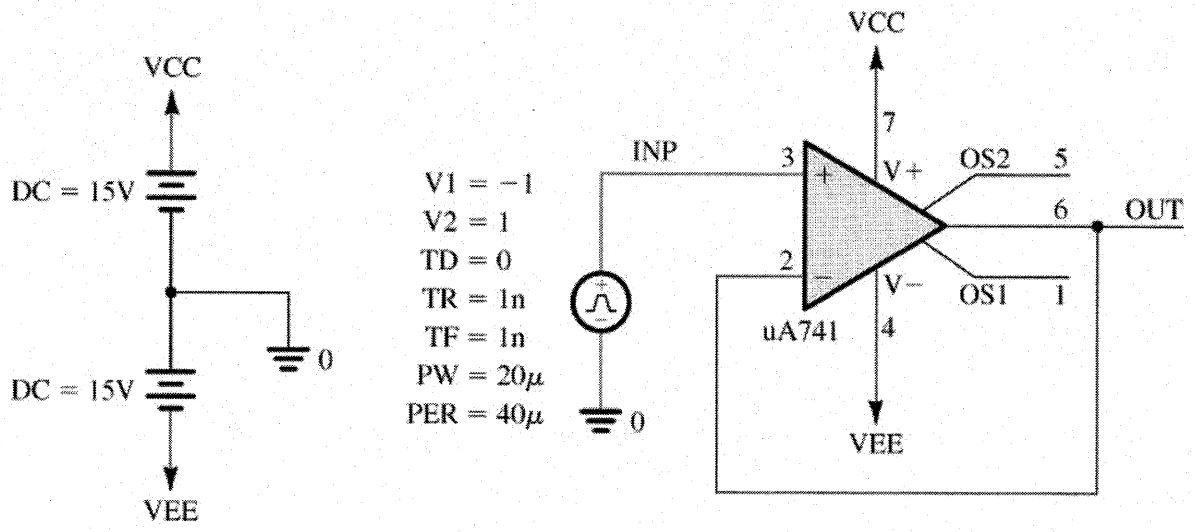


Figure 2.50 Frequency response of the μA741 op amp in Example 2.9.

Slew Rate



Delay = 0
Risetime = 1ns
Falltime = 1ns
Pulsewidth = 20μs
Period = 40μs

Voltage follower

Figure 2.51 Circuit for determining the slew rate of the uA741 op amp in Example 2.9.

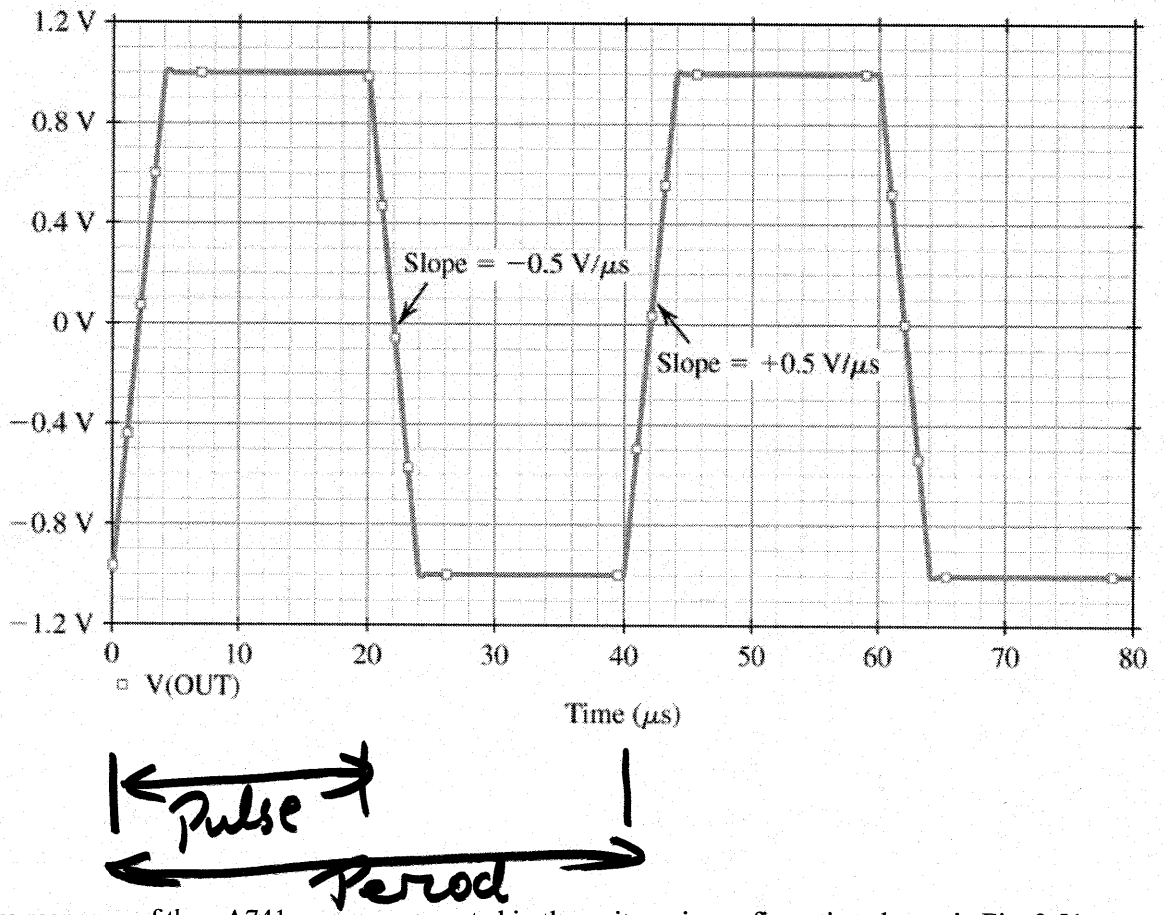


Figure 2.52 Square-wave response of the μA741 op amp connected in the unity-gain configuration shown in Fig. 2.51.

Summary

- Offset voltage
  - Offset null or capacitive coupling
- Bias current
  - $R_3=R_1||R_2$ (& capacitive coupling effects)
- Offset current
- Integrator
  - Bias/offset current effects
- Differentiator
- Op Amp macromodels

Assignment #2 (due Tues Oct 10th)

Problems:

2.64

2.86

2.95

2.104

2.116