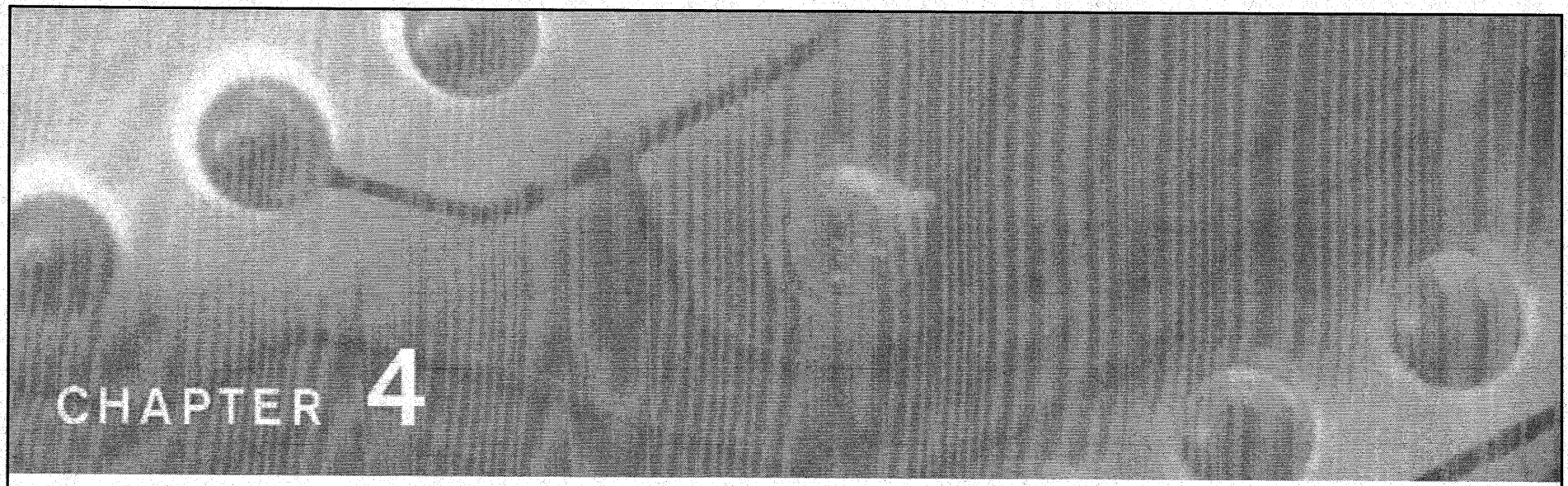
ECE321 Electronics I

Fall 2006

Professor James E. Morris

Lecture 17

28th November, 2006

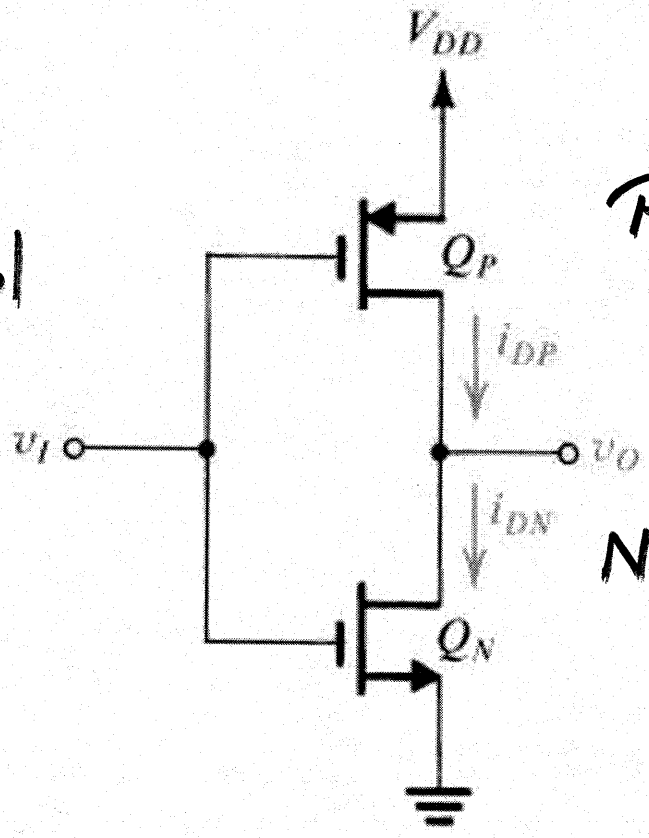


MOS Field-Effect Transistors (MOSFETs)

4.10 CMOS Inverter
4.11 Depletion MOSFET
4.12 SPICE (very brief)

CMOS Inverter : See also Example 4.7

Turns on when
$v_I < V_{DD} - |V_{tp}|$



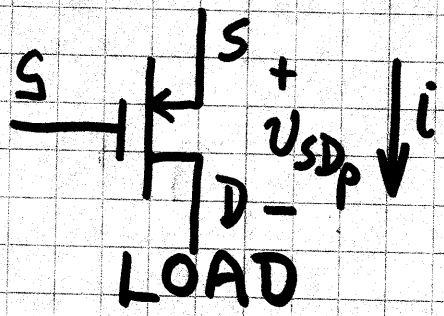
P-channel Load

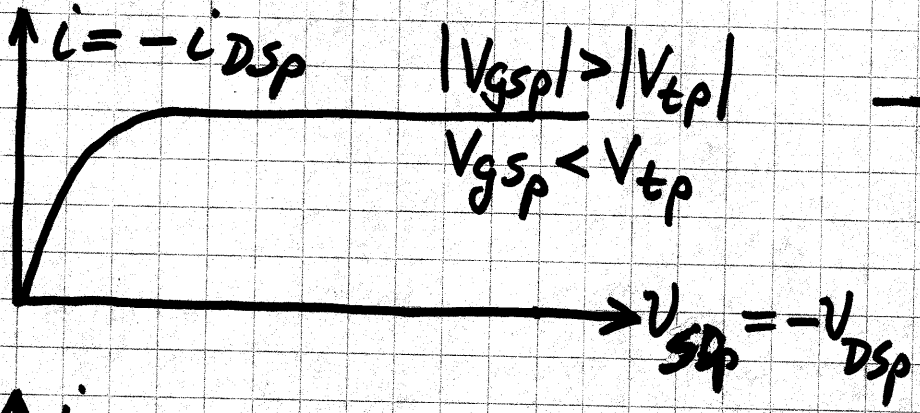
N-channel Driver

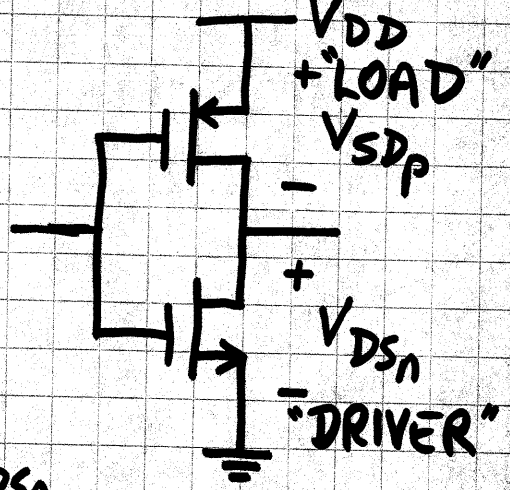
Turns on when
$v_I > V_{tn}$

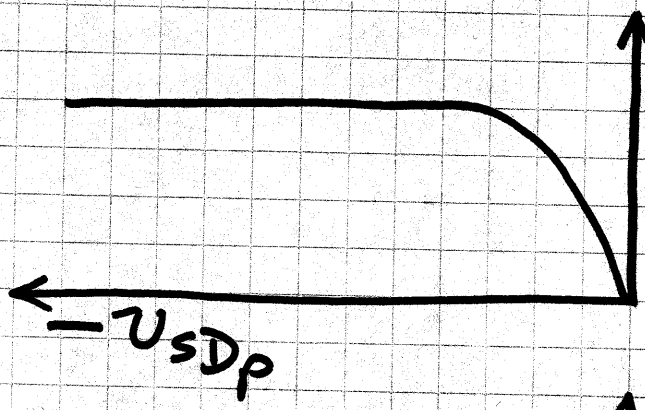
Figure 4.53 The CMOS inverter.

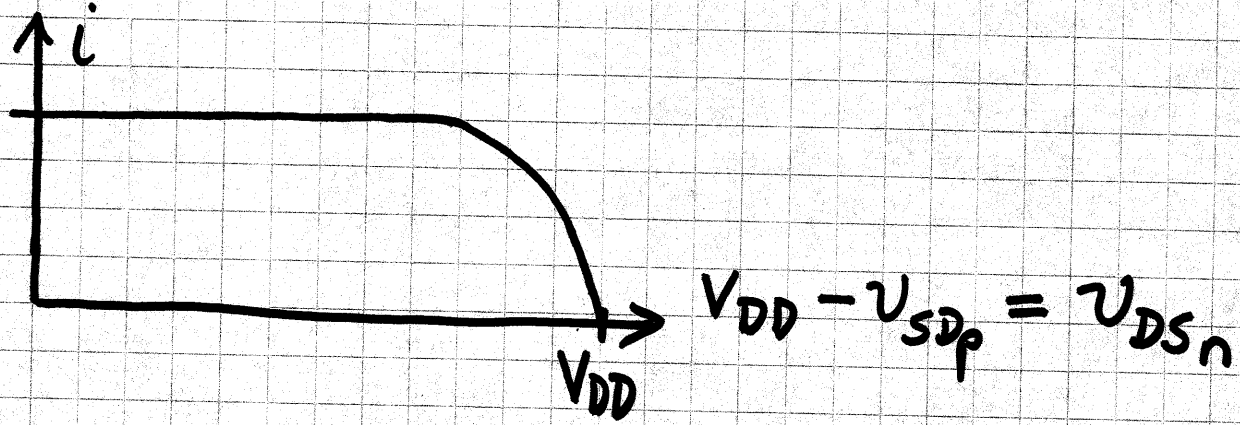
LOAD LINE CONSTRUCTION

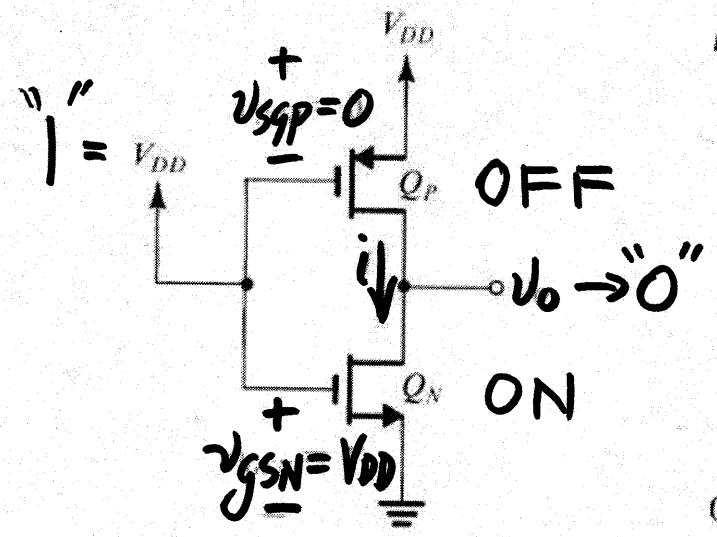




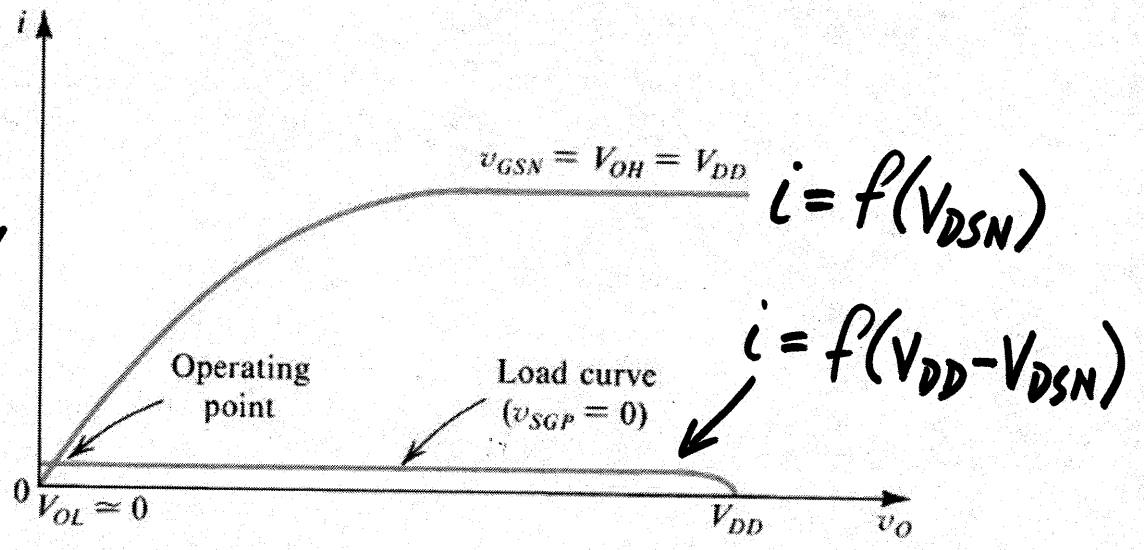








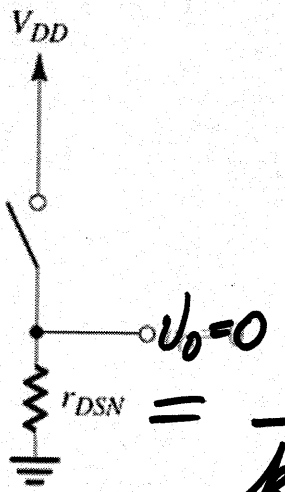
(a)



(b)

N channel – triode

P channel – cutoff (~ saturation)



(c)

$$r_{DSN} = \frac{1}{k_n'\left(\frac{W}{L}\right)_n (V_{DD} - V_{tn})}$$

V_{GS}

Figure 4.54 Operation of the CMOS inverter when v_I is high: **(a)** circuit with $v_I = V_{DD}$ (logic-1 level, or V_{OH}); **(b)** graphical construction to determine the operating point; **(c)** equivalent circuit.

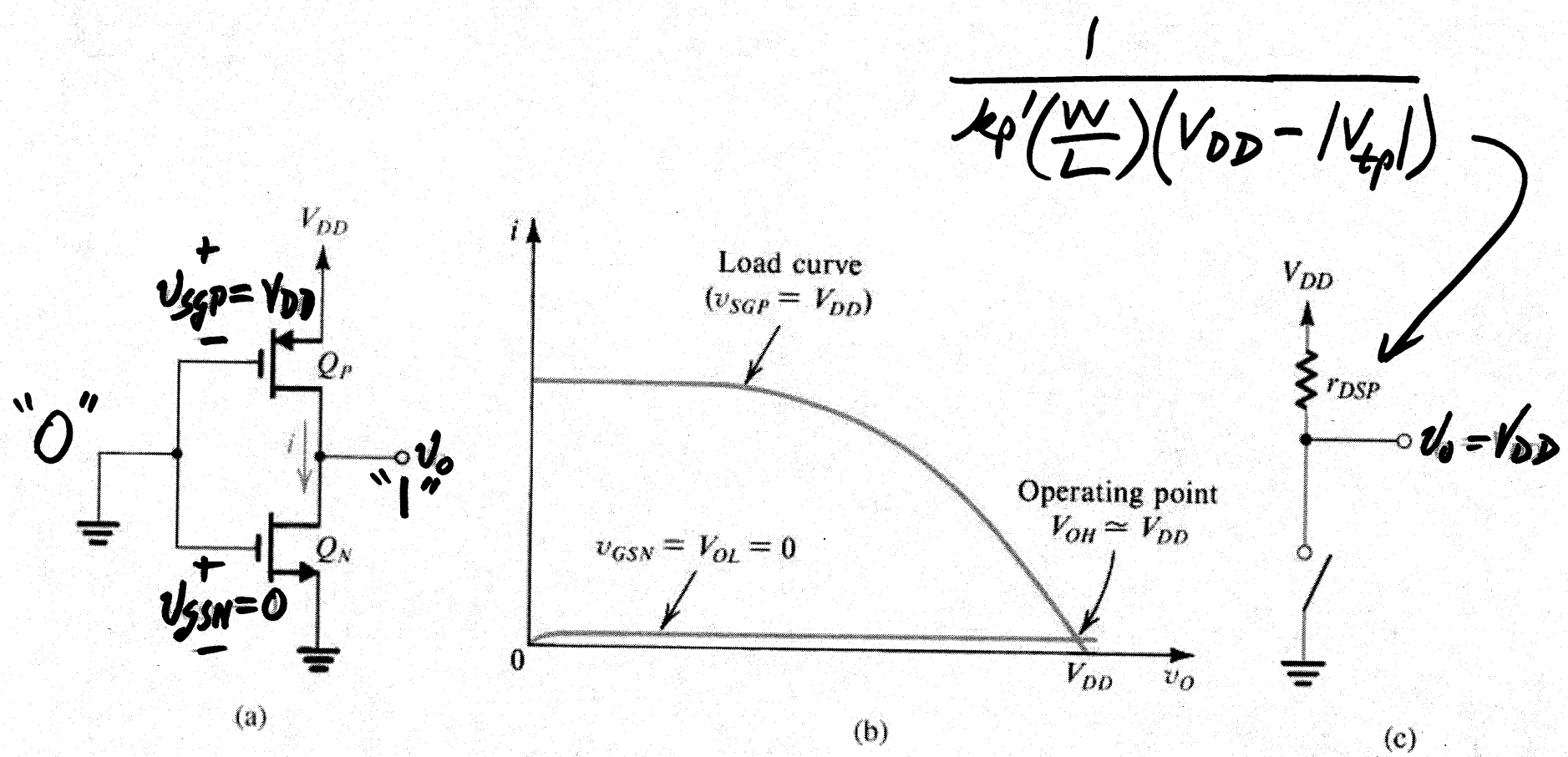
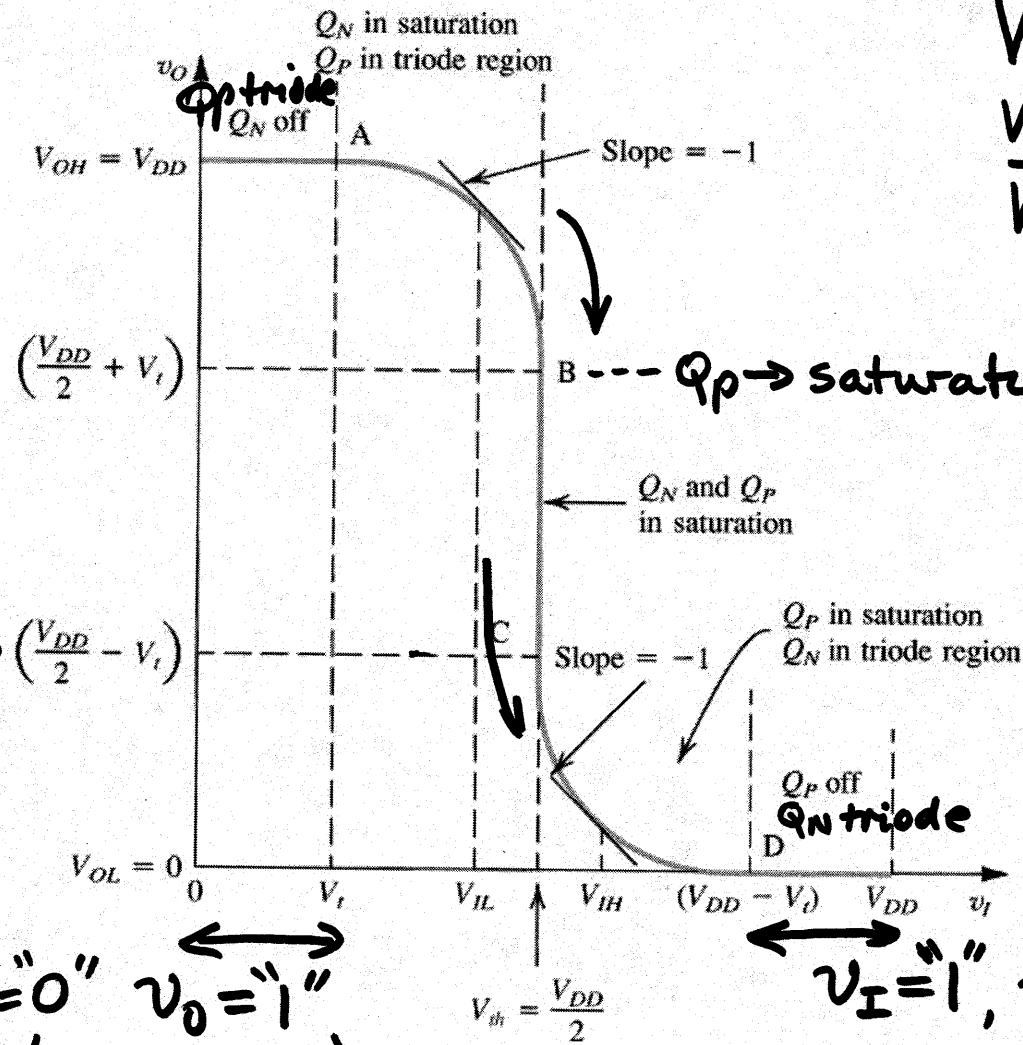


Figure 4.55 Operation of the CMOS inverter when v_I is low: **(a)** circuit with $v_I = 0$ V (logic-0 level, or V_{OL}); **(b)** graphical construction to determine the operating point; **(c)** equivalent circuit.

For symmetry

$V_{tn} = |V_{tp}|$

$\frac{W_p}{W_n} = \frac{\mu_n}{\mu_p}$



Q_n changes → saturation to triode

v_I = "0" v_O = "1"

$V_{GSN} < V_{tn}$

$|V_{GSP}| > |V_{tp}|$

Transfer characteristic

v_I = "1", v_O = "0"

$V_{GSN} > V_{tn}$

$|V_{GSP}| < |V_{tp}|$

Figure 4.56 The voltage transfer characteristic of the CMOS inverter.

See next

TRANSFER CHARACTERISTIC

Assume initial state $v_I < V_{tn}$ ie. $v_I = "0"$, Q_N off, $v_O = "1"$
$< V_{tp}$ $\therefore Q_P$ on, but $V_{SDp} = 0$
$\therefore Q_P$ in triode

As $v_I \rightarrow > V_{tn}$ Q_n in saturation Q_p in triode

$$i_{Dn} = \frac{1}{2} k_n' \left(\frac{W}{L}\right)_n (v_I - V_{tn})^2 \qquad i_{Dp} = k_p' \left(\frac{W}{L}\right)_p \left[\begin{array}{l}(V_{DD} - v_I - |V_{tp}|) \\ \times (V_{DD} - v_O) \\ -\frac{1}{2}(V_{DD} - v_O)^2\end{array}\right]$$

& $i_{Dn} = i_{Dp} = i$, $k_n' \left(\frac{W}{L}\right)_n = k_p' \left(\frac{W}{L}\right)_p$, $V_{tn} = |V_{tp}| = V_t$

$$\therefore \frac{1}{2}(v_I - V_{tn})^2 = (V_{DD} - v_I - |V_{tp}|)(V_{DD} - v_O) - \frac{1}{2}(V_{DD} - v_O)^2$$

$$(v_O - V_{DD})^2 + 2(v_O - V_{DD})((V_{DD} - V_t) - v_I) + (V_t - v_I)^2 = 0$$

Solve quadratic for $(v_O - V_{DD}) = f(v_I - V_t)$
Differentiate to find where slope $= -1$

Until $Q_p \longrightarrow$ saturation at $V_{Dp} = V_{Gp} + |V_t|$

$$v_O = v_I + V_t$$

When $v_o = v_I + V_t$

Substitute back for v_I

$$(v_o - V_{DD})^2 + 2(v_o - V_{DD})(V_{DD} - v_o) + (v_o - 2V_t)^2 = 0$$

i.e. $$(v_o - V_{DD})^2 = (v_o - 2V_t)^2$$

$$v_o - V_{DD} = \pm (v_o - 2V_t)$$

Either ~~$v_o - V_{DD} = v_o - 2V_t$~~ Not valid Or $v_o - V_{DD} = -v_o + 2V_t$

$$v_o = \frac{V_{DD}}{2} + V_t$$

& $\therefore$ $$v_I = v_o - V_t = \frac{V_{DD}}{2}$$

When Q_n, Q_p both saturated

$$i = \frac{1}{2} k_n' \left(\frac{W}{L}\right)_n (v_I - V_{tn})^2 = \frac{1}{2} k_p' \left(\frac{W}{L}\right)_p (V_{DD} - v_I - V_t)^2$$

i.e. $$(v_I - V_t)^2 = (V_{DD} - (v_I + V_t))^2$$

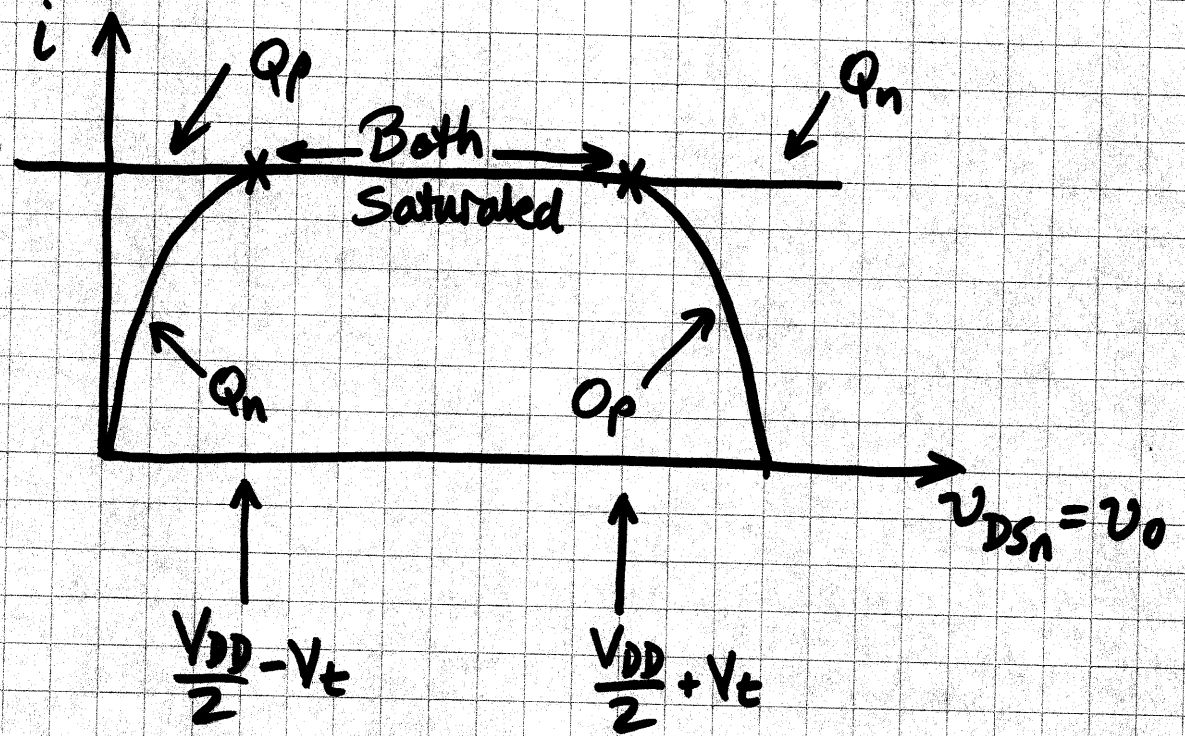
$$v_I - V_t = \pm (V_{DD} - (v_I + V_t))$$

Either $v_I - V_t = V_{DD} - (v_I + V_t)$ Or $v_I - V_t = v_I + V_t - V_{DD}$

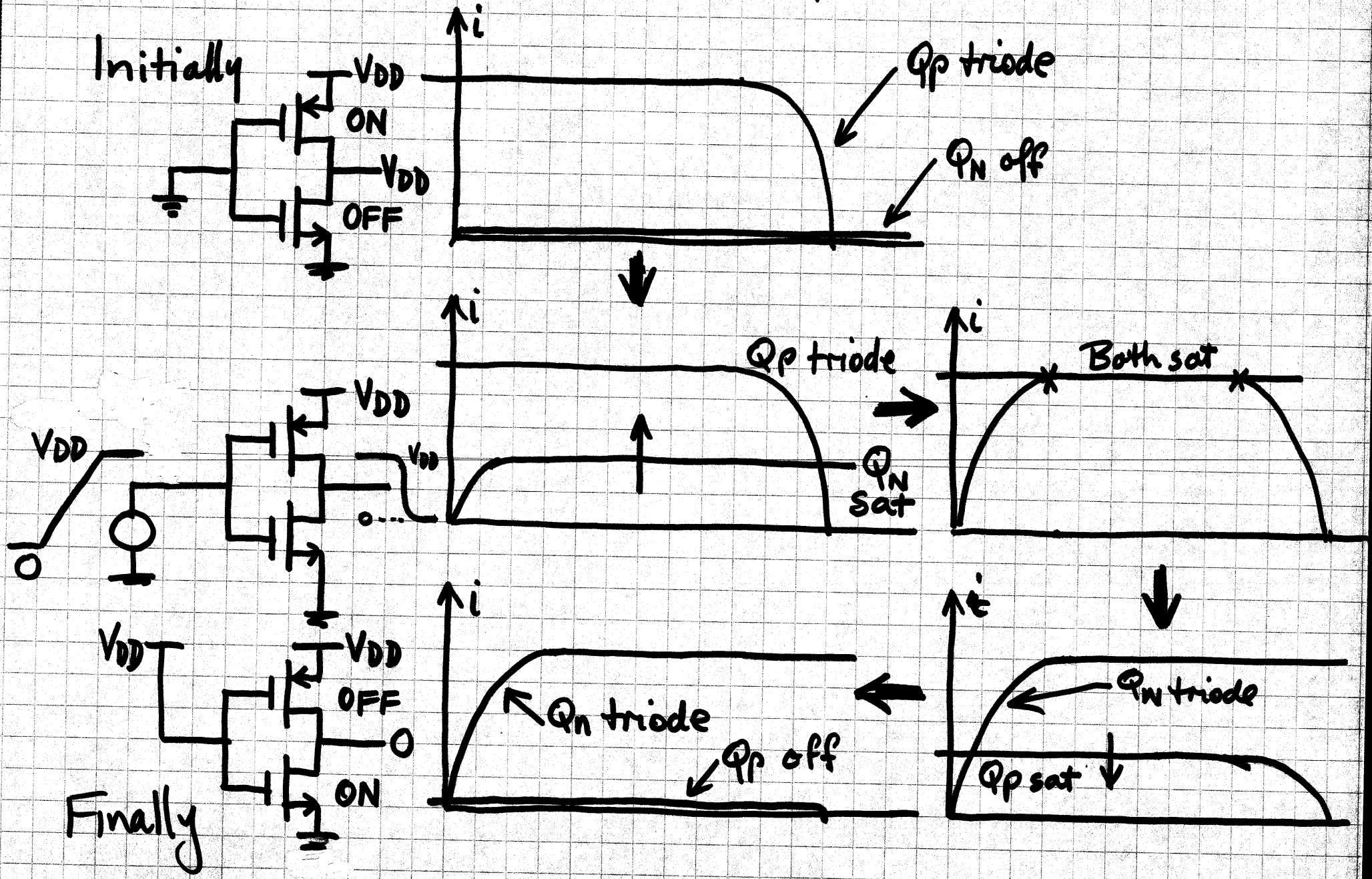
$v_I = V_{DD}/2$ Not valid.

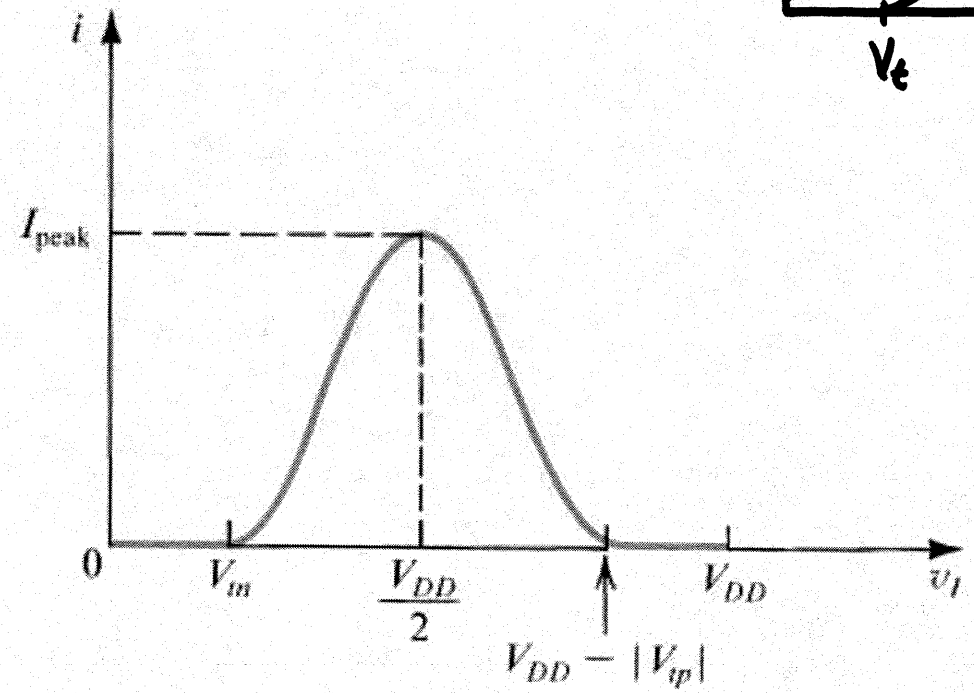
When Q_n, Q_p both saturated

& $i_n = i_p = i$



Transfer characteristic sweep





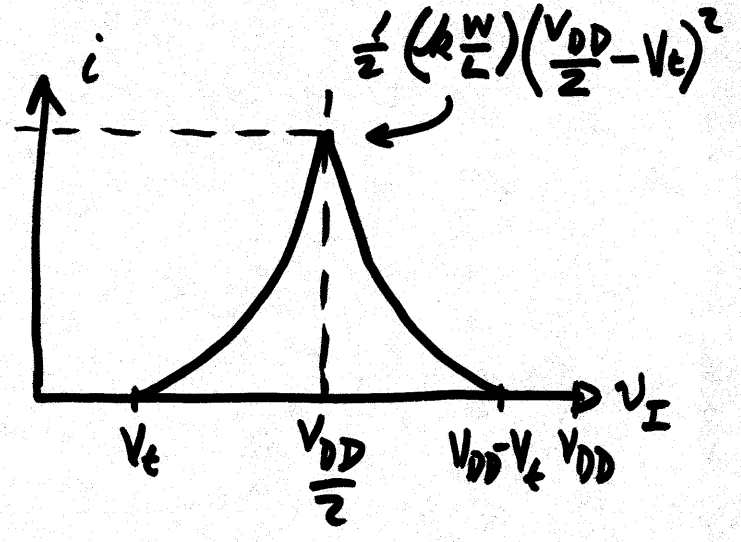


Figure 4.58 The current in the CMOS inverter versus the input voltage.

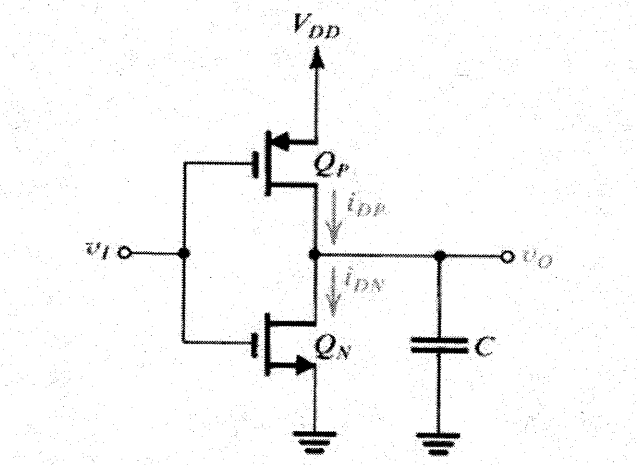
(Exercise 4.41)

Exercise 4.42

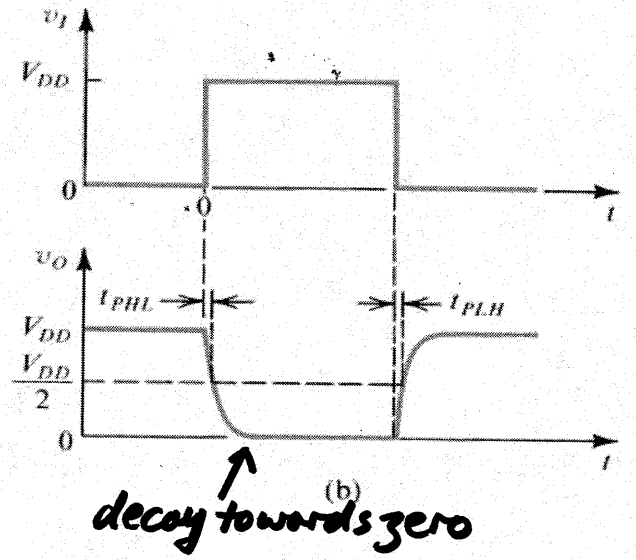
(Exercise 4.43)

Exercise 4.44

TRANSIENT RESPONSE

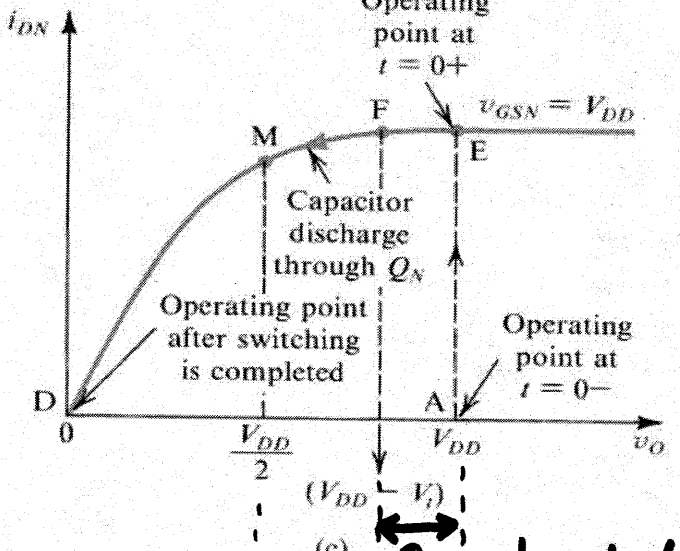


(a)



(b)

decay towards zero



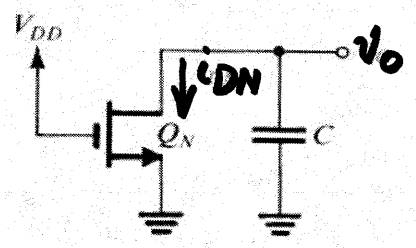
(c)

Q_n triode

Q_n saturated.

Evaluate t_{PHL} as $V_{DD} \rightarrow \frac{V_{DD}}{2}$

Q_n off



(d)

Figure 4.57 Dynamic operation of a capacitively loaded CMOS inverter: **(a)** circuit; **(b)** input and output waveforms; **(c)** trajectory of the operating point as the input goes high and C discharges through Q_N; **(d)** equivalent circuit during the capacitor discharge.

When Q_N saturated $i_{DN} = \frac{1}{2} k_n' \left(\frac{W}{L}\right)_n (V_{DD} - V_t)^2$

($V_{DD} - V_t$ ← V_{gsn})

ie. constant until $v_o = V_{DD} - V_t$

$$\therefore t_{pHL1} = \frac{C[V_{DD} - (V_{DD} - V_t)]}{\frac{1}{2} k_n' \left(\frac{W}{L}\right)_n (V_{DD} - V_t)^2}$$

(t_{pHL1} ← High → Low)

From $v_o = V_{DD} - V_t$ to $v_o = 0$ (or $V_{DD} - V_t$ for cutoff)

Q_N in triode region, $i_{DN} = k_n' \left(\frac{W}{L}\right)_n \left[(V_{DD} - V_t) v_o - \frac{1}{2} v_o^2\right]$

and $i_{DN}(t)\, dt = -C\, dv_o(t)$

$$\int_0^{t_{pHL2}} \frac{k_n' \left(\frac{W}{L}\right)_n}{C} dt = \int_{V_{DD}-V_t}^{V_{DD}/2} \frac{dv_o(t)}{(V_{DD} - V_t)\left[\frac{v_o^2}{2} - v_o\right]}$$

defining t_{pHL} as time to $V_{DD}/2$

$$\int \frac{dx}{ax^2 - x} = \ln\left(1 - \frac{1}{ax}\right) \longrightarrow$$

$$t_{pHL2} = \frac{C}{k_n' \left(\frac{W}{L}\right)_n (V_{DD} - V_t)} \ln\left(1 - \frac{2(V_{DD} - V_t)}{v_o}\right)\Bigg]_{V_{DD}-V_t}^{V_{DD}/2}$$

$$= \quad " \quad \ln(3 - 4V_t/V_{DD})$$

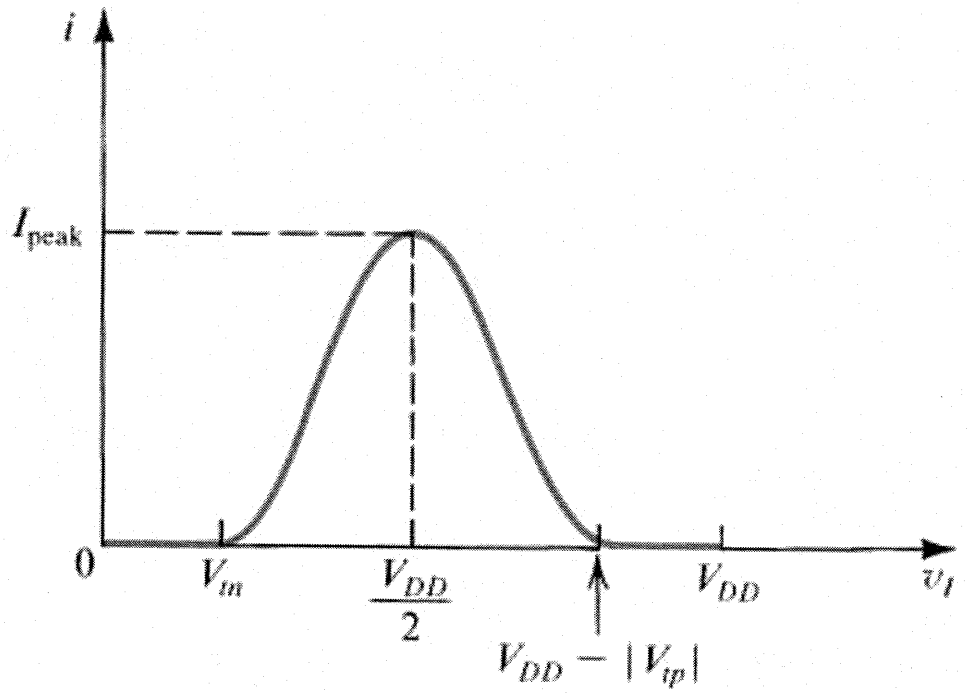
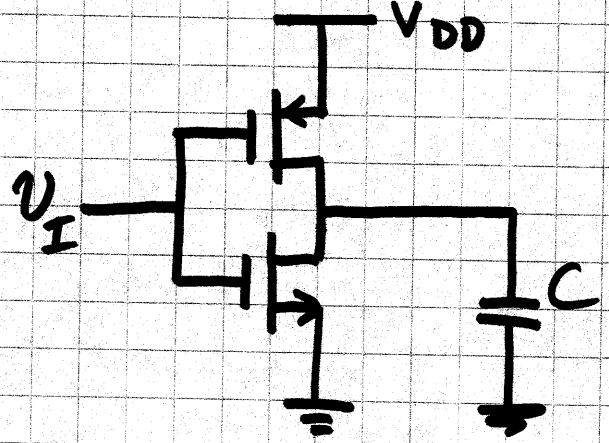
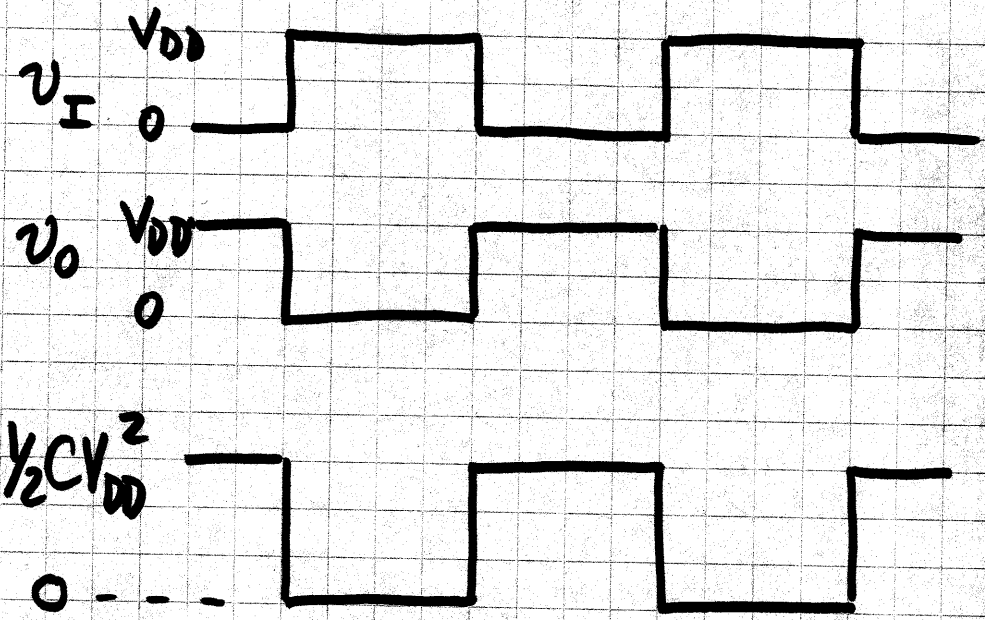


Figure 4.58 The current in the CMOS inverter versus the input voltage.

POWER DISSIPATION





Discharge through r_{DSN}

$\frac{1}{2}CV_{DD}^2$ dissipated in r_{DSN}

Charge through r_{DSP}

$\therefore \frac{1}{2}CV_{DD}^2$ dissipated in r_{DSP}

$\therefore$ Total energy dissipated/cycle $= CV_{DD}^2$

$\therefore \quad P_D = fCV_{DD}^2$

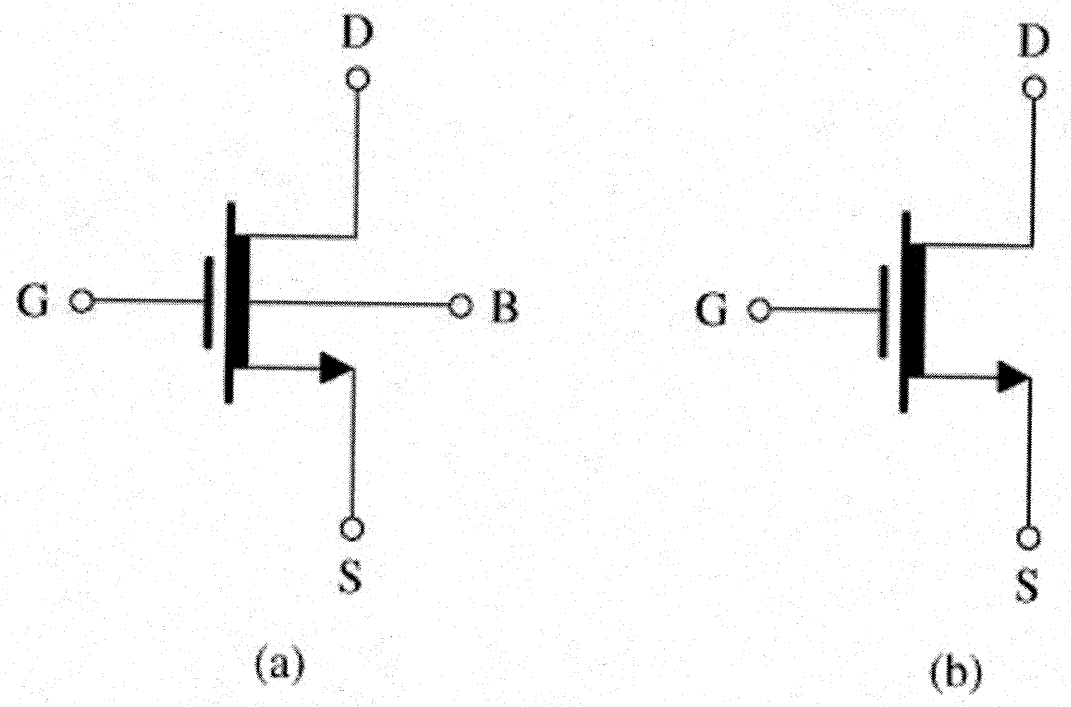
(Exercise 4.45)

(Exercise 4.46)

Exercise 4.47/48

Exercise 4.49

DEPLETION MOSFET



Also N-channel

Figure 4.59 **(a)** Circuit symbol for the *n*-channel depletion-type MOSFET. **(b)** Simplified circuit symbol applicable for the case the substrate (B) is connected to the source (S).

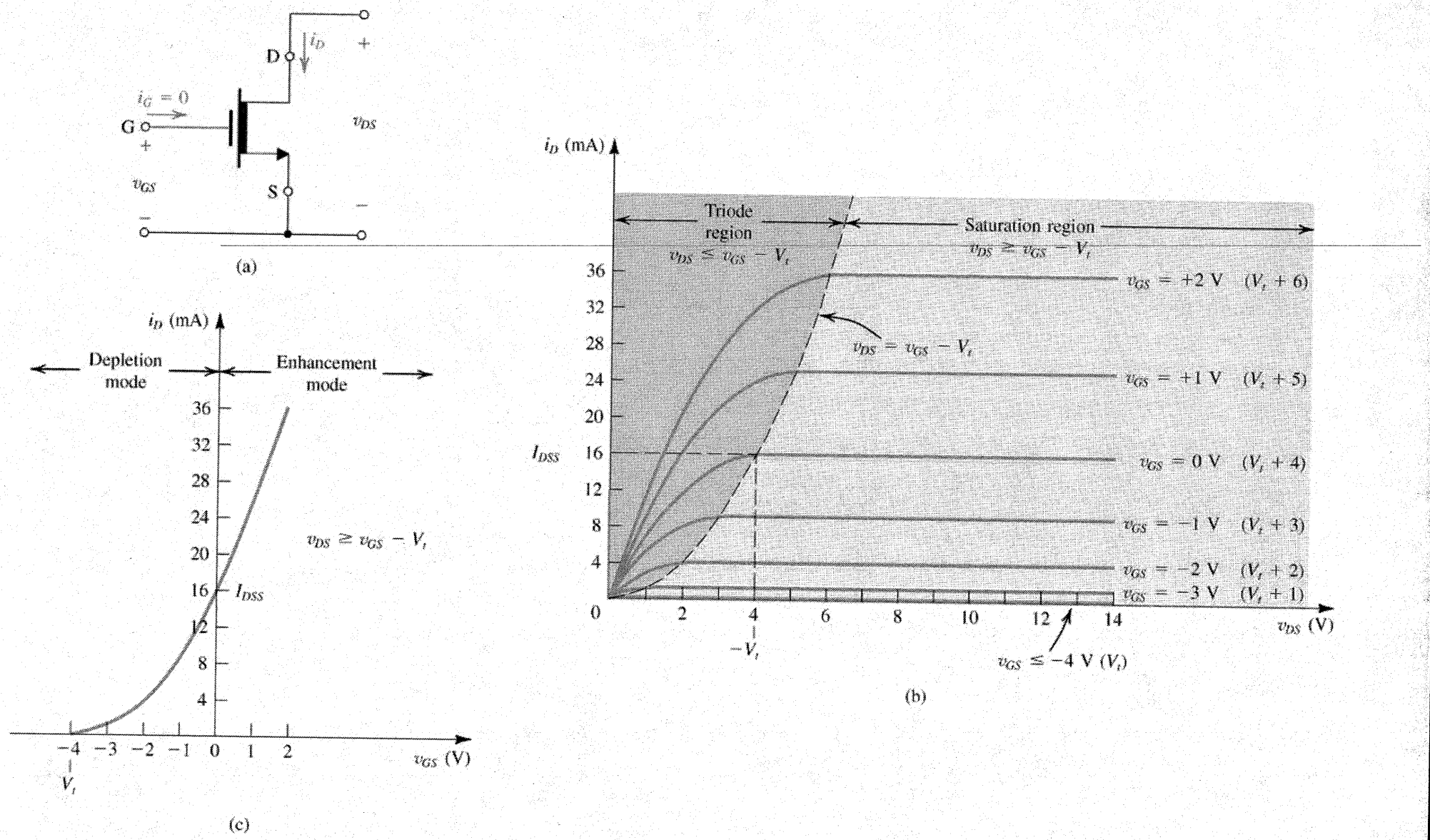


Figure 4.60 The current-voltage characteristics of a depletion-type *n*-channel MOSFET for which $V_t = -4$ V and $k'_n(W/L) = 2$ mA/V^2: **(a)** transistor with current and voltage polarities indicated; **(b)** the i_D–v_{DS} characteristics; **(c)** the i_D–v_{GS} characteristic in saturation.

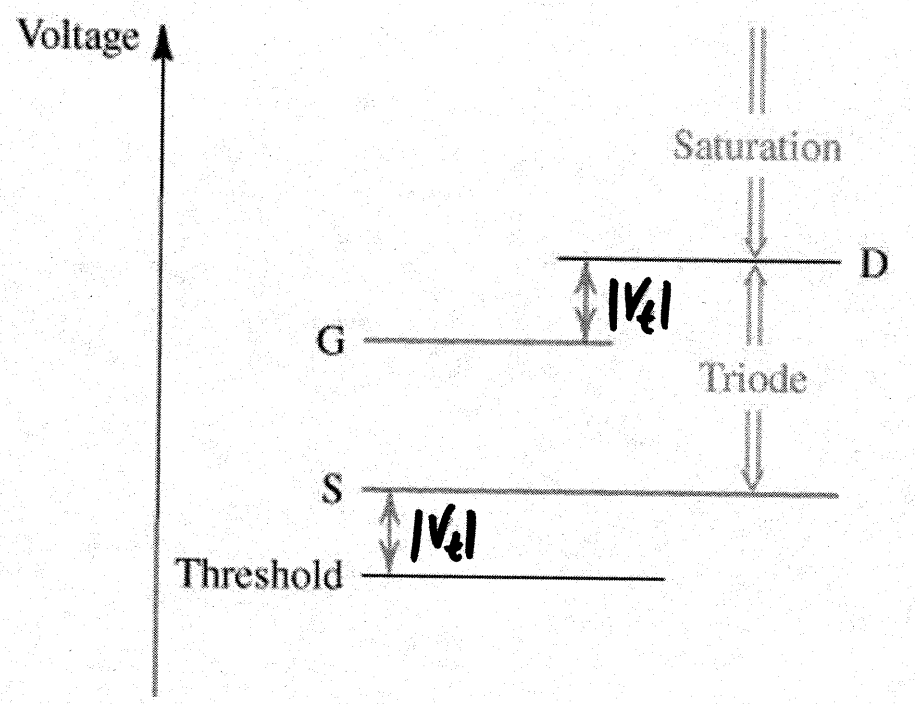


Figure 4.61 The relative levels of terminal voltages of a depletion-type NMOS transistor for operation in the triode and the saturation regions. The case shown is for operation in the enhancement mode (v_{GS} is positive).

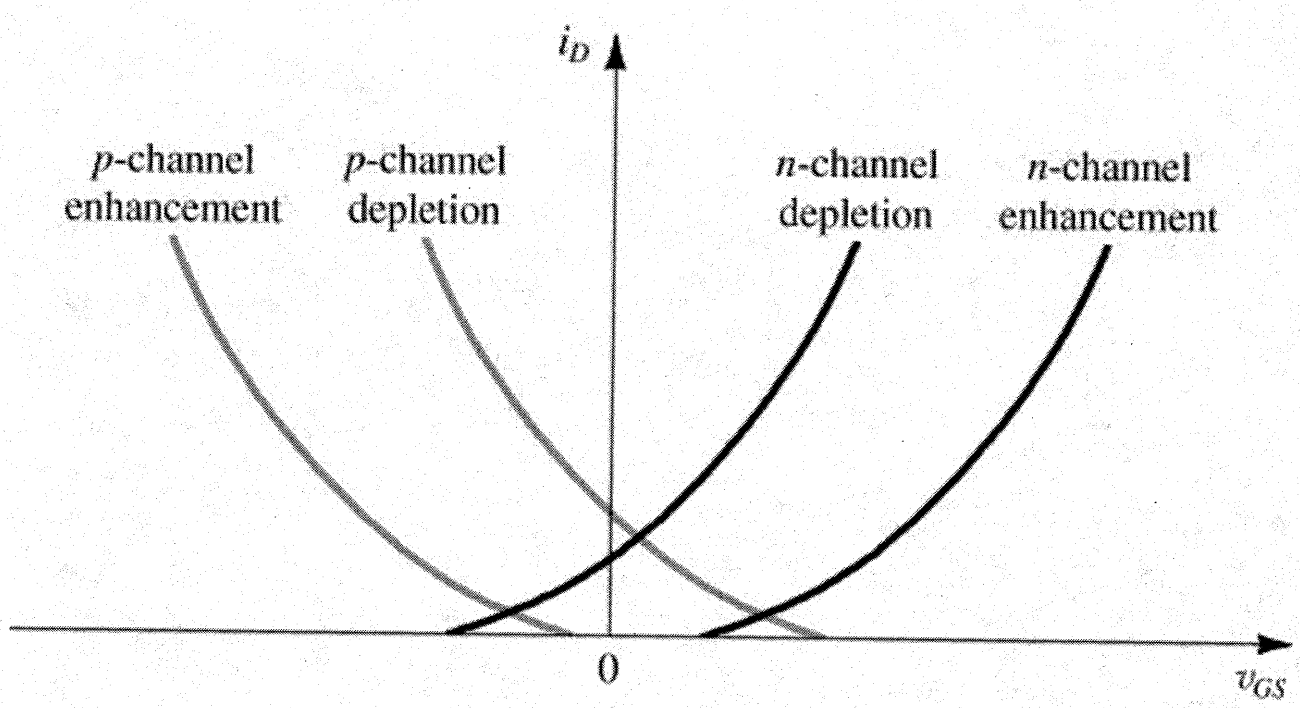


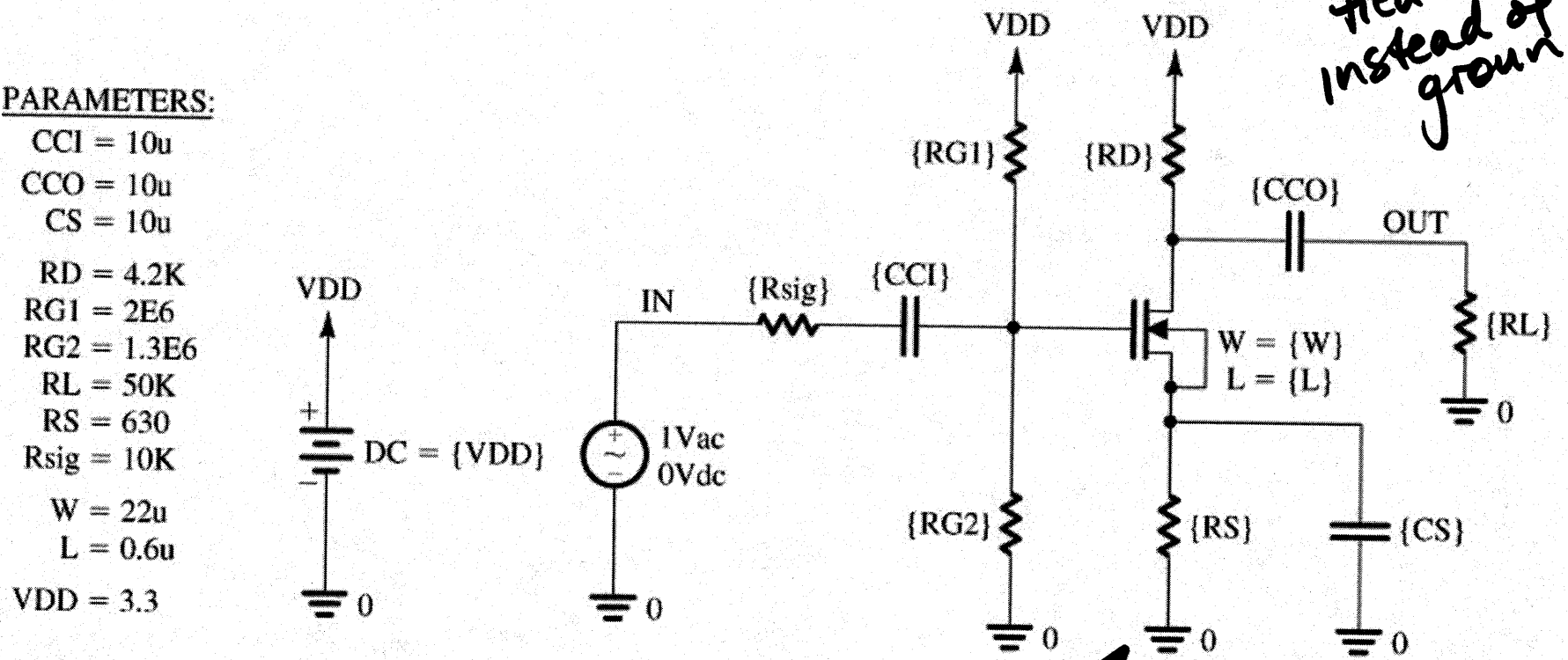
Figure 4.62 Sketches of the i_D–v_{GS} characteristics for MOSFETs of enhancement and depletion types, of both polarities (operating in saturation). Note that the characteristic curves intersect the v_{GS} axis at V_t. Also note that for generality somewhat different values of $|V_t|$ are shown for *n*-channel and *p*-channel devices.

Exercise 4.50

Exercise 4.51

Exercise 4.52

SPICE Example



Note Body tied to source instead of ground.

Note R_S instead of constant current bias. We did a similar BJT case including R_E.

Figure 4.63 Capture schematic of the CS amplifier in Example 4.14.

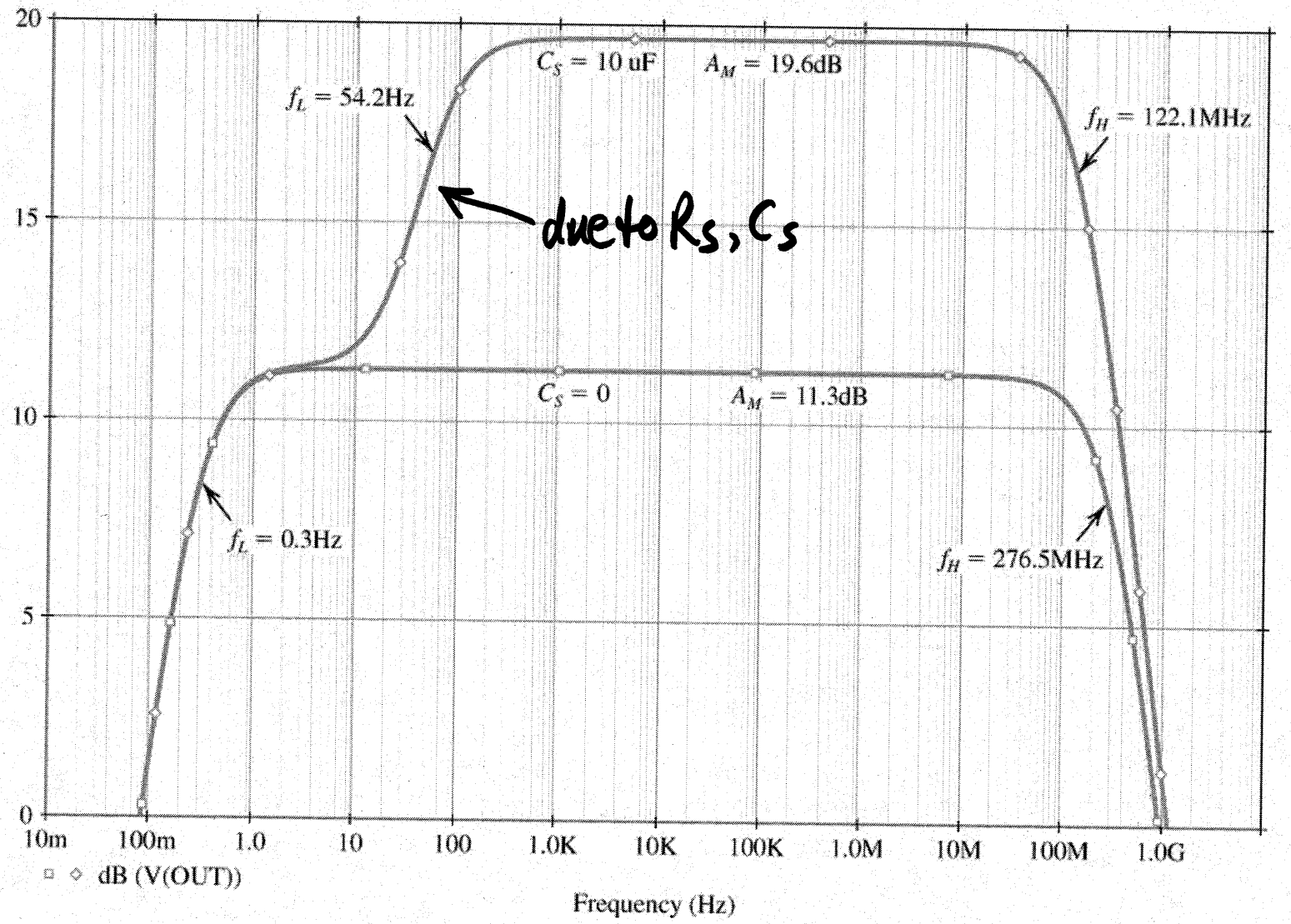


Figure 4.64 Frequency response of the CS amplifier in Example 4.14 with $C_S = 10\ \mu F$ and $C_S = 0$ (i.e., C_S removed).

Ex 4.41 Substitute into formulae

* Ex 4.42 CMOS inverter $V_{tn} = |V_{tp}| = 2V$ $\left(\frac{W}{L}\right)_n = 20$ $\left(\frac{W}{L}\right)_p = 40$

$V_{DD} = 10V$ $\mu_n C_{ox} = 2\mu_p C_{ox} = 20\mu A/V^2$

For $v_I = V_{DD}$, find max current inverter can sink for $v_O \leq 0.5V$

Ex 4.43 Exercise in matching $\mu \frac{W}{L}$ values for N and P.
Then use formula for r_{DS}

* Ex 4.44 For non-matched $\mu W/L$ values, $r = \sqrt{\frac{k_p'(W/L)_p}{k_n'(W/L)_n}}$

Show $V_{th} = \frac{r(V_{DD} - |V_{tp}| + V_{tn})}{1+r}$

Ex 4.42

$V_{tn} = 2V$

$\mu_n C_{ox}\left(\frac{W}{L}\right)_n = 20 \times 20\mu A/V^2 = 400\mu A/V^2$

$\mu_p C_{ox}\left(\frac{W}{L}\right)_p = 40 \times 10\mu A/V^2 = 400\mu A/V^2$

$\therefore$ Equal, but don't need

$v_I = V_{DD} = 10V$ $\therefore$ Q_p off Q_n in triode region ← Only need Q_n

$\therefore i_{O)max} = 400\mu A\left((V_{GS} - V_t)V_{DS} - \frac{1}{2}V_{DS}^2\right)$

$= 400\mu A\left[(10-2)0.5 - \frac{1}{2}0.5^2\right]$

$= 400\mu A\left[4 - .125\right] = 1.55mA$

$(1600\mu A - 50\mu A)$

Use results in 4.47/48

Ex 4.44 At $V_I = V_{th}$ both Q's in sat'n

$$\therefore \frac{1}{2} k_n' \left(\frac{W}{L}\right)_n (V_{th} - V_{tn})^2 = \frac{1}{2} k_p' \left(\frac{W}{L}\right)_p (V_{DD} - V_{th} - |V_{tp}|)^2$$

$$r = \sqrt{\frac{k_p' (W/L)_p}{k_n' (W/L)_n}} = \frac{V_{th} - V_{tn}}{V_{DD} - V_{th} - |V_{tp}|}$$

$$r (V_{DD} - V_{th} - |V_{tp}|) = V_{th} - V_{tn}$$

$$V_{th} (1 + r) = r V_{DD} + V_{tn} - r |V_{tp}|$$

$$V_{th} = \frac{r (V_{DD} - |V_{tp}|) + V_{tn}}{1 + r}$$

Ex 4.45 Conditions match the requirement for equation 4.157
Substitute $\longrightarrow t_{pHL}$. Symmetrical $\therefore t_{PLH} = t_{PHL}$
& $t_p = \frac{1}{2}(t_{pHL} + t_{PLH}) =$ same

Ex 4.46 Uses equation 4.157 again

Ex 4.47 & Ex 4.48

For the inverter of Ex. 4.42:

4.47 Find peak current during switching

4.48 $C_{load} = 15pF$. Find P_D at 2MHz

Find average power supply current

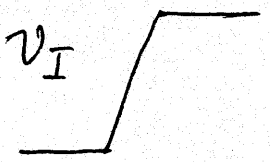
Ex 4.49 CMOS VLSI chip has 100,000 gates fabricated in 1.2μm technology
Load capacitance is 30fF/gate. Operate at 100MHz & 5volt supply.
Find (a) P_D/gate (b) P_{TOT} if only 30% of gates switch at once.

Ex 4.47

Peak current at $v_I = V_{th} = \frac{V_{DD}}{2} = 5V$
& Q_n, Q_p sat'd

$$\therefore i_{peak} = \frac{1}{2} 400\mu A (5-2)^2 = 1.8mA$$

(400 μA: 4.42; $(5-2)^2$: $V_{gs_n} = V_I = \frac{V_{DD}}{2}$; $(5-2)^2$: 4.42)



Gate input capac
Cannot switch v_I
instantly.

Ex 4.48

$$P_D = fCV_{DD}^2 = 2\times10^6 \times 15\times10^{-12}\ 100$$
$$= 3mW$$

$$I_{AV} = \frac{3mW}{10V} = 0.3mA$$

Ex 4.49

$$P_D/gate = fCV_{DD}^2$$
$$= 10^8 \times 30\times10^{-15}\ 5^2$$
$$= 75\mu W$$

$$P_{tot} = 0.3 \times 10^5 \text{ gates} \times 75\times10^{-6}$$
$$= 2.25 \text{ watts}$$

Ex 4.51 $k_n'(W/L) = 4\,mA/V^2$ $V_t = -2V$ $I_{DSS} = ?$

Neglect effect of v_{DS} on i_D in saturation, (i.e. $r_o = \infty$)
find V_S.

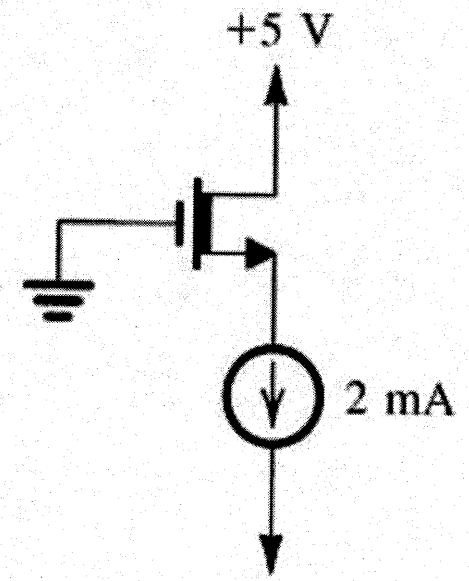


Figure E4.51

Ex 4.50 Depletion NMOS $V_t = -2V$

$k_n' \frac{W}{L} = 2\,mA/V^2$

Find minimum v_{DS} for saturation at $v_{GS} = +1V$
& corresponding i_D

4.50

$V_t = -2V \qquad k_n' \frac{W}{L} = 2mA/V^2 \qquad v_{GS} = +1V$

For saturation $v_{DS} \geq v_{GS} - V_t$

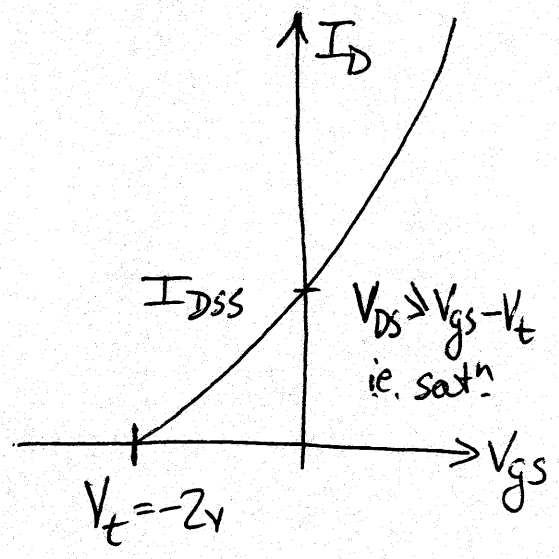
$\geq 1V - (-2V)$

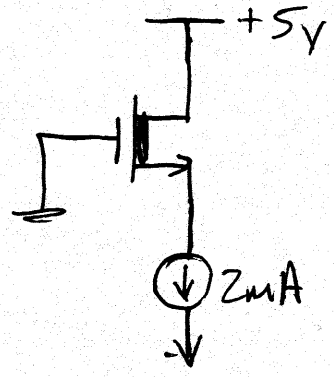
$\geq 3V$

& $i_D = \frac{1}{2} k_n' \frac{W}{L} (v_{GS} - V_t)^2$

$= 1mA\,(3)^2 = 9mA$

Ex 4.51





Assume saturation

$$I_D = \frac{1}{2} k_n' \frac{W}{L} (V_{GS} - V_t)^2$$

$$I_{DSS} = \frac{1}{2} 4mA \left(0 - (-2)\right)^2$$

$$= 8mA$$

$$2mA = \frac{1}{2} 4mA (V_{GS} - V_t)^2$$

$$\therefore V_{GS} - V_t = \pm 1$$

$$V_{GS} = -2 \pm 1 = -3, -1 \text{ V}$$

$I_D = 0$ $\therefore V_{GS} = -1V$

$$\therefore V_S = +1V$$

Ex 4.52 Find i as a function of v

Neglect effect of v_{DS} on i_D in saturation

(i.e. $r_o = \infty$)

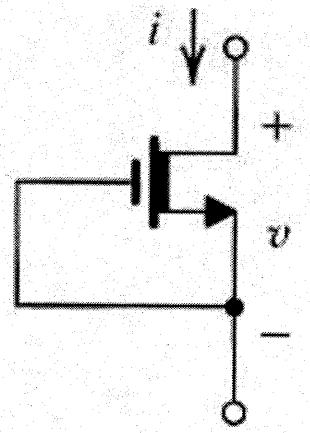
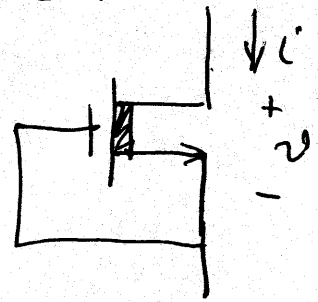


Figure E4.52

Ex 4.52



$V_{gs} = 0$

For $v < V_t$

$$i = k_n' \frac{W}{L} \left[(V_{gs} - V_t) v_{DS} - \tfrac{1}{2} v_{DS}^2 \right]$$
$$= k_n' \frac{W}{L} \left[-V_t v - \tfrac{1}{2} v^2 \right]$$

For $v > V_t$

$$i = \tfrac{1}{2} k_n' \frac{W}{L} (V_{gs} - V_t)^2$$
$$= \tfrac{1}{2} k_n' \frac{W}{L} V_t^2$$