ECE321 Electronics I
Fall 2006

Professor James E. Morris

Lecture 1

25th September, 2006

SYLLABUS
ECE321 Electronics I

Fall 2006

Catalog Introduction to solid state electronics, leading to the physical properties and characteristics of solid state electronic devices: diodes, bipolar junction transistors and field effect transistors. Analysis and design of analog systems and operational amplifier based amplifiers, active filters, oscillators and rectifier topologies. Application of a computer-aided design (CAD) tool, such as SPICE. Prerequisite: ECE222.

Coordinator:

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Office hours	Tu/Th 10:00 - 11:00

Credits: 4

Textbook(s): **Microelectronic Circuits (5th Edition)**, Adel Sedra & Kenneth Smith Oxford University Press, (2004) ISBN: 0-19-514251-9, (required); [including supplementary problems]

Reference(s): **The Spice Book**, *Andrei Vladimirescu*, Wiley, 1994, ISBN 0-471-6926-9, 1st Ed. **SPICE**, *G.W.Roberts & A.S.Sedra*, OUP, 1997, (designed to supplement the text.) Other similar Spice support text, e.g. Tuinenga, Banzhaf, Rashid, Keown, Hambley "Electrical Engineering, 3e" Appendix D, (all P-H) [Optional]

Prerequisites:

By course number:

- ECE223

By topic:

- Linear circuit analysis: Norton/Thevenin, node/mesh analysis
- Ideal operational amplifiers and circuits
- Transfer functions and circuit responses in the time and frequency domains
- Spice, (or similar circuit simulator)

Corequisites: By course number:

- ECE301 (Tues 15.00-17.50; Wed 16.00-18.50)

Structure

- Two 110 minute lecture periods per week.
- Weekly homework and reading assignments
- One mid-term test and one final exam
- (Occasional in-class "pop" quizzes)
- ECE301 lab (separate registration) grades included

Grading

- Eight weekly assignments (8 x 5% = 40%)
- One mid-term test (20%) & one final exam (20%)
- Eight ECE301 experiments (8 x 2.5% = 20%)

Grading Scale

Letter Grade	Range
A	90+
A-	85 - 90
B+	80 - 85
B	75 - 80
B-	70 - 75
C+	65 - 70
C	60 - 65
C-	55 - 60
D+	50 - 55
D	45 - 50
D-	40 - 45
F	40-

Course Outcomes

- Ability to analyze and design ideal OPAMP-based amplifiers & other circuits.
- Ability to analyze and design non-ideal OPAMP-based circuits.
- Understand the principles of solid-state material properties (energy band structures, conductivity through drift and diffusion, PN-junctions)
- Ability to analyze and design diode circuits for power conversion and wave-shaping.
- Understand the semiconductor principles of Bipolar Junction Transistor (BJT) and Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET) operation.
- Ability to analyze and design single-BJT amplifiers (in all three topologies) and switches (including biasing.)
- Ability to analyze and design single-MOSFET amplifiers (in all three topologies) and switches (including biasing.)
- Ability to use circuit simulation tools for the design and analysis of OPAMP, diode, BJT, and MOS circuits.

Course/Program outcome mapping

Topics

I. **Introduction to Electronics.** Signal classification & spectrum; amplifiers, circuit models, & frequency response; digital logic inverter; ideal op-amp review.
(2 hours)

II. **Operational Amplifiers.** Op-amp circuits; non-ideal op-amps; frequency response of op-amps; large-signal limitations; integration & differentiation; macro-modeling. (6 hours)

III. **Solid-state Electronics.** Semiconductors: drift & diffusion currents; covalent bonds, doping, & energy band models; mobility & resistivity; PN junction; MOSFET structure & operation; BJT structure & operation. (6 hours)

IV. **Diodes.** Diode characteristics; diode models; zener diodes ; rectification ; clipping & clamping; op-amp superdiode. (4 hours)

V. **Bipolar Junction Transistors.** BJT characteristics & operation regions; BJT switch & inverter; single-stage amplifier topologies; DC analysis & biasing; small signal operation & models; high-frequency effects & CE frequency response; Spice model. (11 hours)

VI. **MOSFETS.** MOSFET characteristics & operation regions; MOSFET switch & amplifier; DC analysis & biasing; small signal operation & models; single-stage amplifier topologies; high-frequency effects & CS frequency response; CMOS inverter, Spice model. (7 hours)

Assignments

Week	Reading	ECE301 Lab & Homework problems
1	1.1 – 1.7 2.1 – 2.3	Lab organization meeting Problems 1:
2	2.4 – 2.6 2.7 – 2.9	Expt 1: PSpice Introduction Problems 2:
3	3.1 – 3.3 3.4 - 3.6	Expt 2: Opamp Circuits Problems 3:
4	3.7 - 3.9 4.1 – 4.2	Expt 3: Audio Equalizer Problems 4:
5	4.3 – 4.5 4.6 – 4.7	Expt : Diode Characteristics Problems 5:
6	4.8 – 4.9 5.1 – 5.2	Expt 5: Diode Circuits Problems 6:
7	Mid-term test: first 10 lectures 5.3 – 5.4	Expt 6: MOSFETs
8	5.5 – 5.6 5.7	Problems 7: Expt 7: BJT Biasing
9	.5.8 – 5.9 Thanksgiving	Problems 8: Expt 8: BJT Amplifiers
10	4.10 - 4.12, 5.10 – 5.11 Review	

Note: Problems: 1-6 assigned Thur, 7-8 assigned Tues; due following Tuesday lecture at noon, returned in Thur lecture.
Final exam: Thur 7th Dec 10.15 – 12.05pm
Course information (outline, assignments, textbook figures) at: http://www.ece.pdx.edu/~jmorris/ece321
Lecture streaming videos available from:

LT-SPICE

Lab next week

Prelim assignment — work through beforehand

Assignment grading

Each problem:

0	Not attempted, or no idea
50%	Not right, but reasonable effort
100%	Right, or "nearly there"

One problem reviewed in more detail

On-line lectures: Password ece321jem

Teaching Assistants

ECE321:

Hui She

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ECE301 (Tues 15.00-17.50):

Tony Muilenburg

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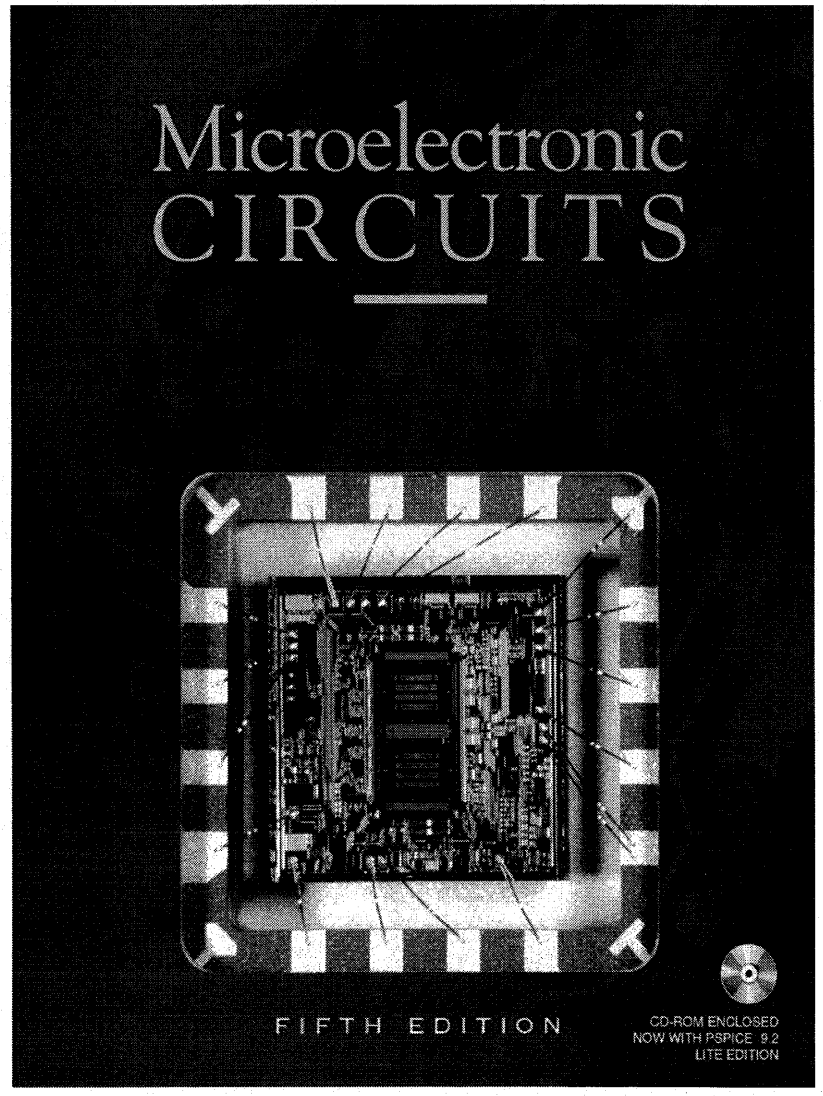
	Tuesday 14.00-14.50 (before lab)

ECE301 (Wed 16.00-18.50):

Ping Xu

FAB	WebCT or pingxu@cecs.pdx.edu
Office hours:	FAB 60-01
	Wednesday 15.00-15.50 (before lab)



www.ece.pdx.edu/~jmorris

On-line (as pdf files)

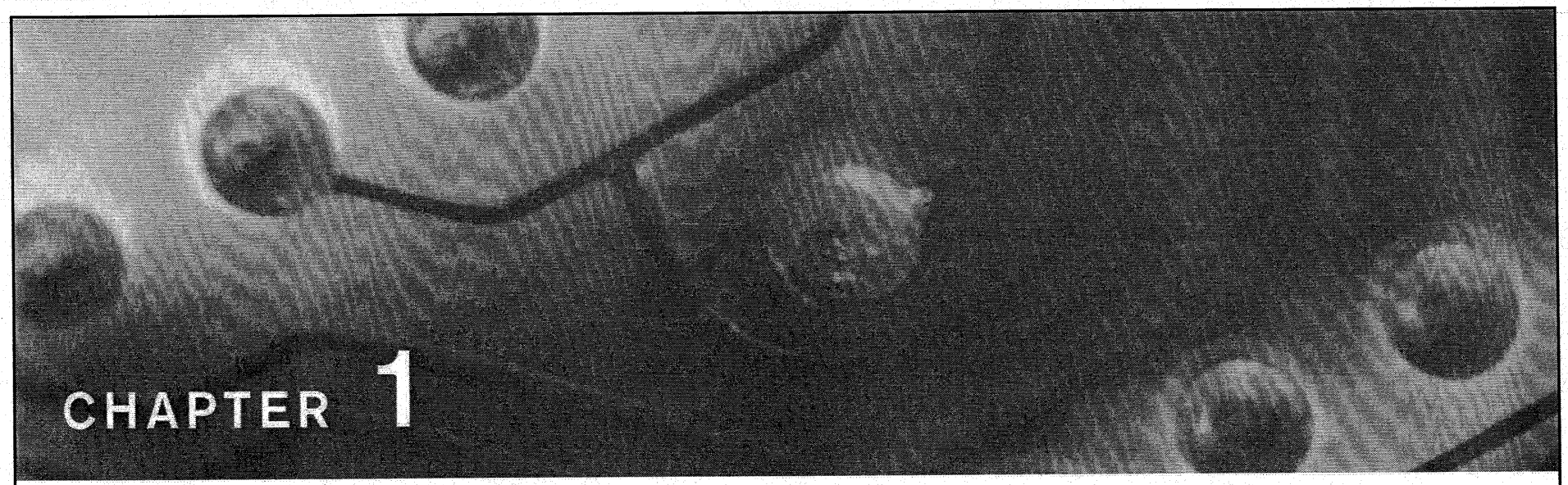
Download
PowerPoint Overheads for

Sedra/Smith
Microelectronic Circuits 5/e

Lectures 1-18
2 slides/page

Use for note-taking in lectures
(Figures already drawn)

Also syllabus (separate file)



Introduction to Electronics

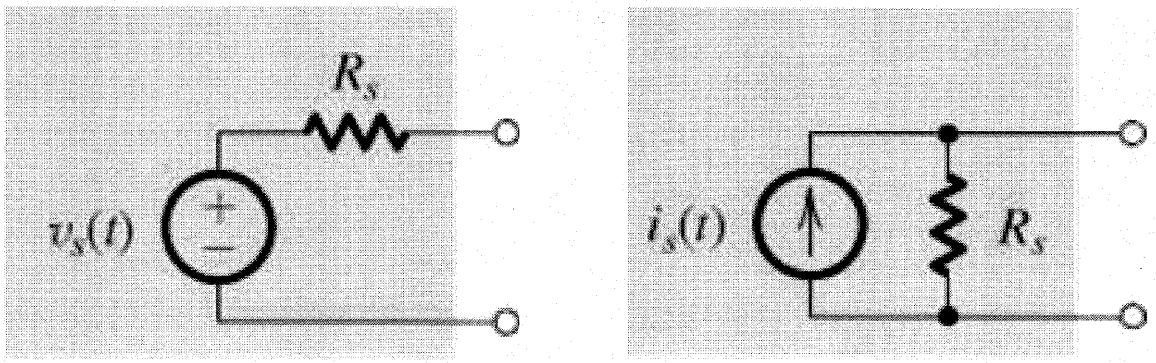
1.1 Signals / 1.2 Spectrum / 1.3 Analog & Digital

1.4 Amplifiers / 1.5 Amplifier Models

1.6 Amplifier Frequency Response

1.7 Logic Inverters / (1.8 SPICE)

You should be fully familiar with network theorems & circuit analysis techniques : Norton/Thévenin, node & mesh analysis, complex impedances, etc.



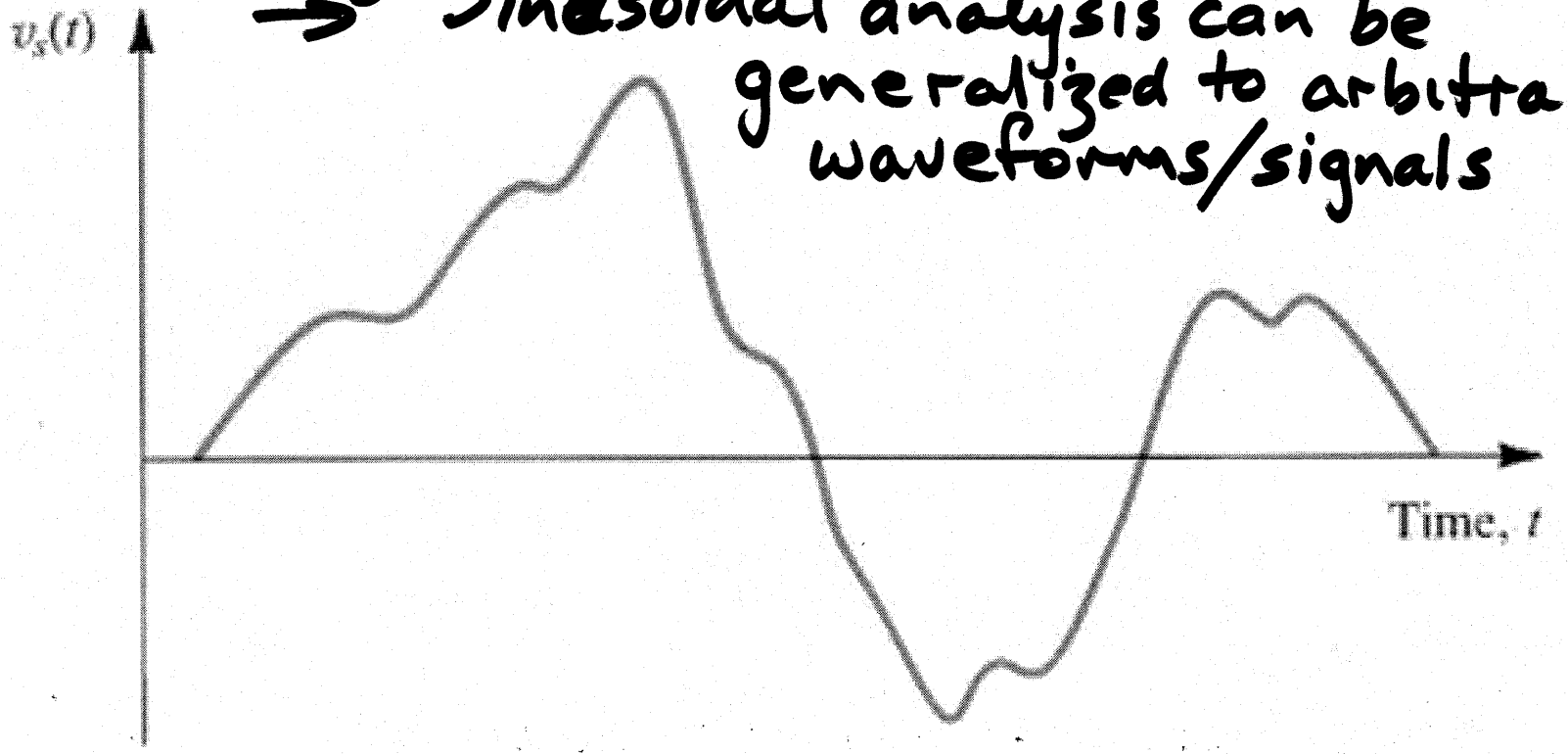
See Exercises 1.1, 1.2. (The answers should be immediately obvious to you!!)

Figure 1.1 Two alternative representations of a signal source: **(a)** the Thévenin form, and **(b)** the Norton form.

In general, YOU do the text EXAMPLES
I will do selected EXERCISES

Arbitrary waveforms & Fourier components

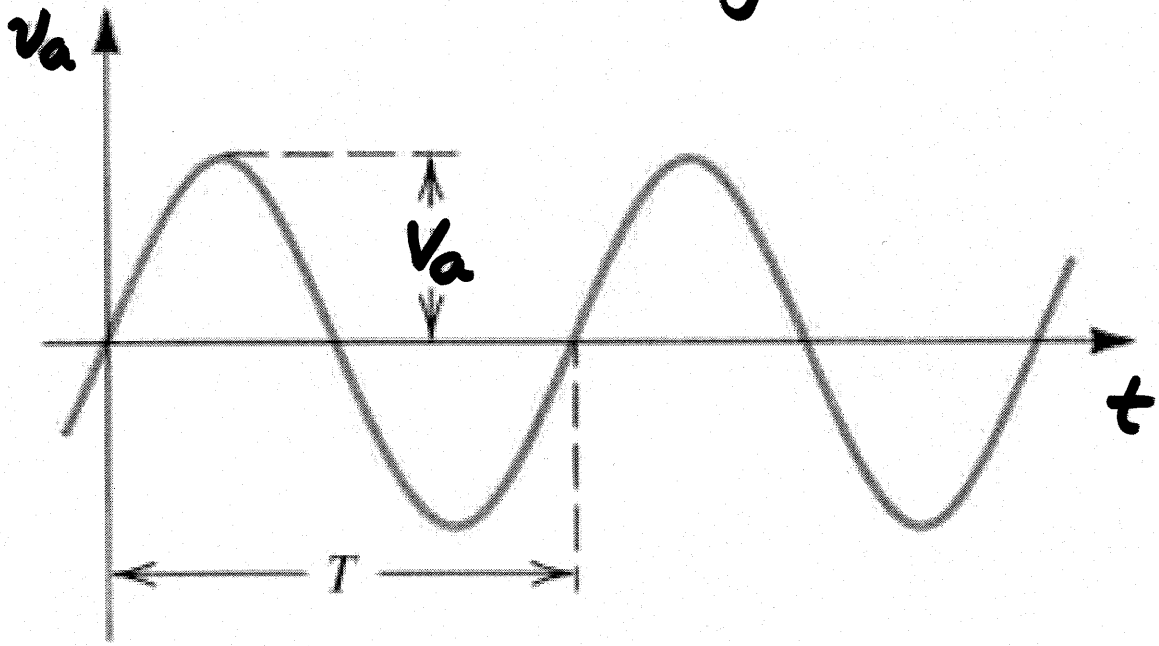
→ Sinusoidal analysis can be generalized to arbitrary waveforms/signals



Revise Fourier analysis, etc (ECE 223?) but we will not need in EEE 321

Figure 1.2 An arbitrary voltage signal $v_s(t)$.

See later for more symbol conventions



$$v_a(t) = V_a \sin \omega t$$

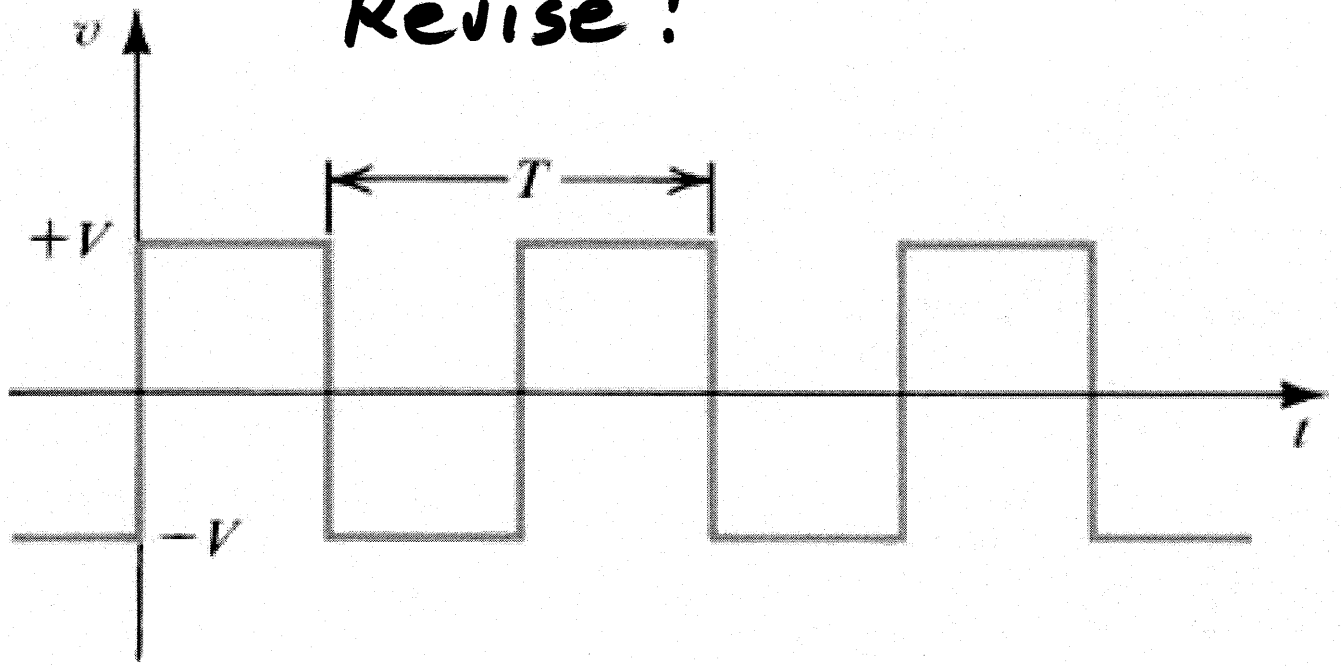
$$\omega = 2\pi f = 2\pi/T$$

Figure 1.3 Sine-wave voltage signal of amplitude V_a and frequency $f = 1/T$ Hz. The angular frequency $v = 2pf$ rad/s.

$$\omega = 2\pi f \Rightarrow v = 2pf$$

Note: Symbols can change with software

We will need some basic digital concepts for logic gate circuits, etc.
Revise!



But we won't need: harmonic components
binary numbers
etc

Figure 1.4 A symmetrical square-wave signal of amplitude V.

Need D/A conversion
Circuits in both ECE 321 & ECE 301

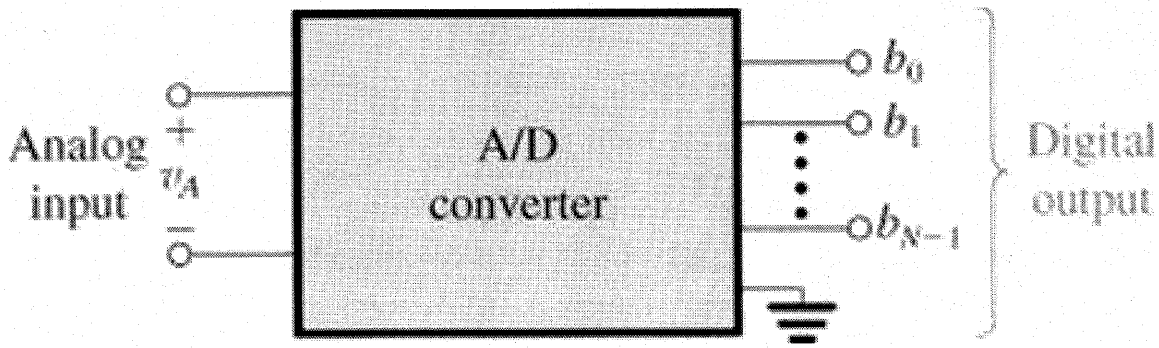
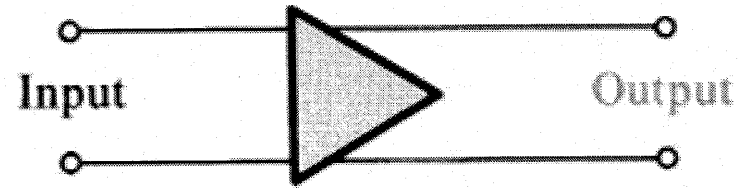


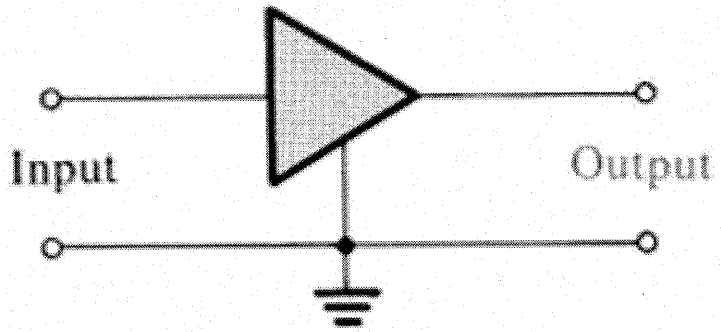
Figure 1.9 Block-diagram representation of the analog-to-digital converter (ADC).

AMPLIFIERS



Floating 2-port

(a)



(b)

Common terminal

e.g. BJT – CE (Common Emitter)

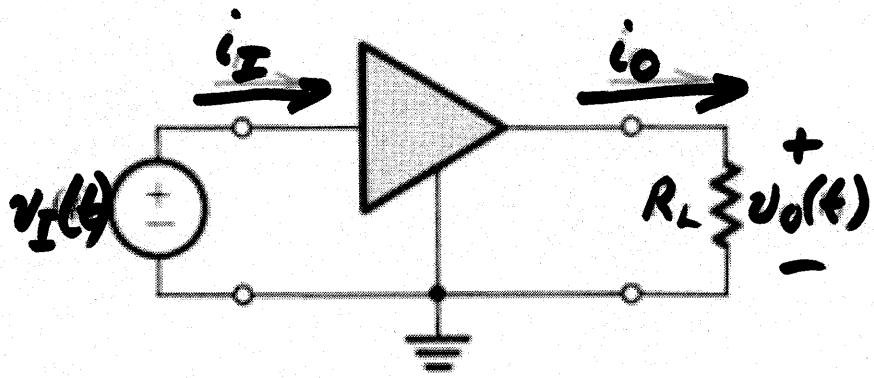
Figure 1.10 **(a)** Circuit symbol for amplifier. **(b)** An amplifier with a common terminal (ground) between the input and output ports.

MOSFET – CS (Common Source)

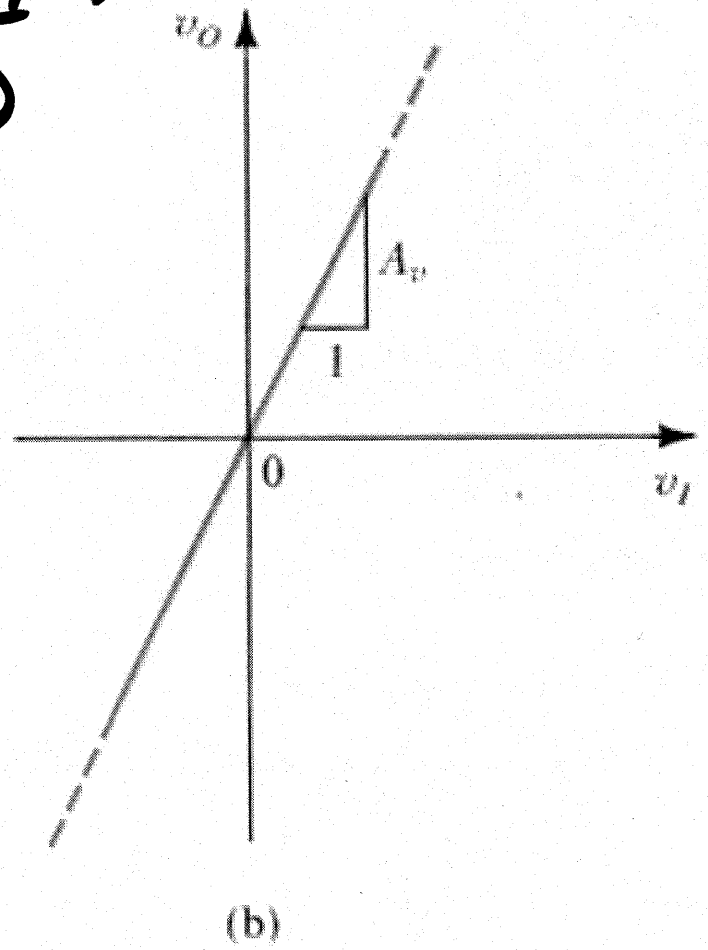
etc

Voltage gain $A_v = v_o(t)/v_I(t)$

$\Rightarrow A_v(\omega)$



(a)



(b)

Also $A_i = i_o/i_I$

$A_p = v_o i_o / v_I i_I$

$= A_v A_i$

Figure 1.11 **(a)** A voltage amplifier fed with a signal $v_I(t)$ and connected to a load resistance R_L. **(b)** Transfer characteristic of a linear voltage amplifier with voltage gain A_v.

Decibels (dB)

Revise (Bode Plots)

$$A_p|_{dB} = 10 \log_{10} P_o/P_I$$

$$= 10 \log_{10} \frac{v_o^2/R}{v_I^2/R} = 20 \log_{10} |A_v|$$

IF R SAME!!

Conventionally $A_v|_{dB} = 20 \log_{10} |v_o/v_I|$

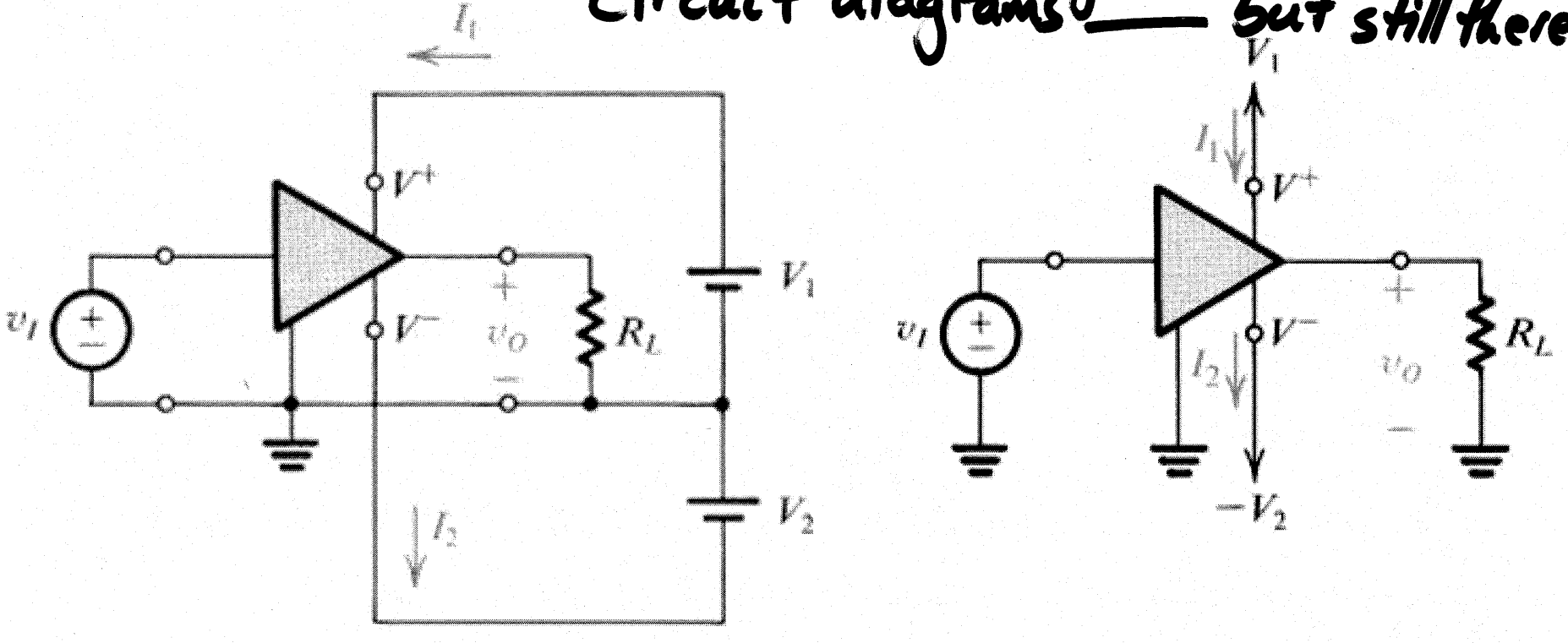
$A_i|_{dB} = 20 \log_{10} |i_o/i_I|$

But CAUTION — $A_p|_{dB} = 10 \log_{10} |A_v A_I|$

$= \frac{1}{2} \{A_v|_{dB} + A_I|_{dB}\}$

(See Ex. 1.8)

Remember: Power supplies usually omitted on circuit diagrams — but still there!



Overall efficiency $\eta = \dfrac{\text{Power out}}{\text{Power in}} = \dfrac{P_L}{P_L + P_{diss}} 100\%$

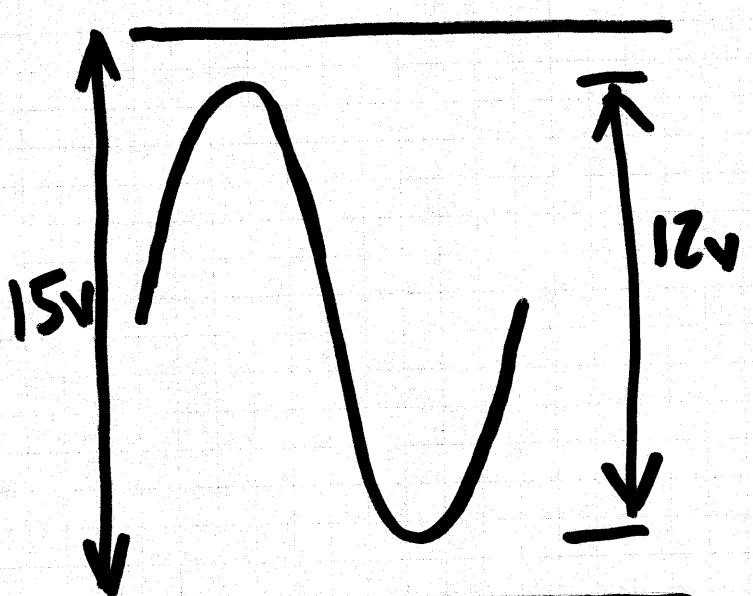
$= \dfrac{P_L}{P_{DC} + P_I} 100\%$

Figure 1.12 An amplifier that requires two dc supplies (shown as batteries) for operation.

$P_{DC} = V_1 I_1 + V_2 I_2$

P_I often ~ 0

Ex. 1·9 Single 15v supply amplifier output
12volt pk-pk sinewave into 1kΩ.
P_I from signal source negligible. Supply current = 8mA.
What is P_{diss} in amp^r and η?



$$P_{IN} \approx P_{DC} = 15v \times 8mA$$
$$= 120\,mW$$

$$P_{OUT} = \frac{1}{2}(12/2)^2/10^3$$
$$= \frac{144}{8}\,mW$$

$$\therefore \eta = \frac{144}{8 \times 120}\,100\% = 15\%$$

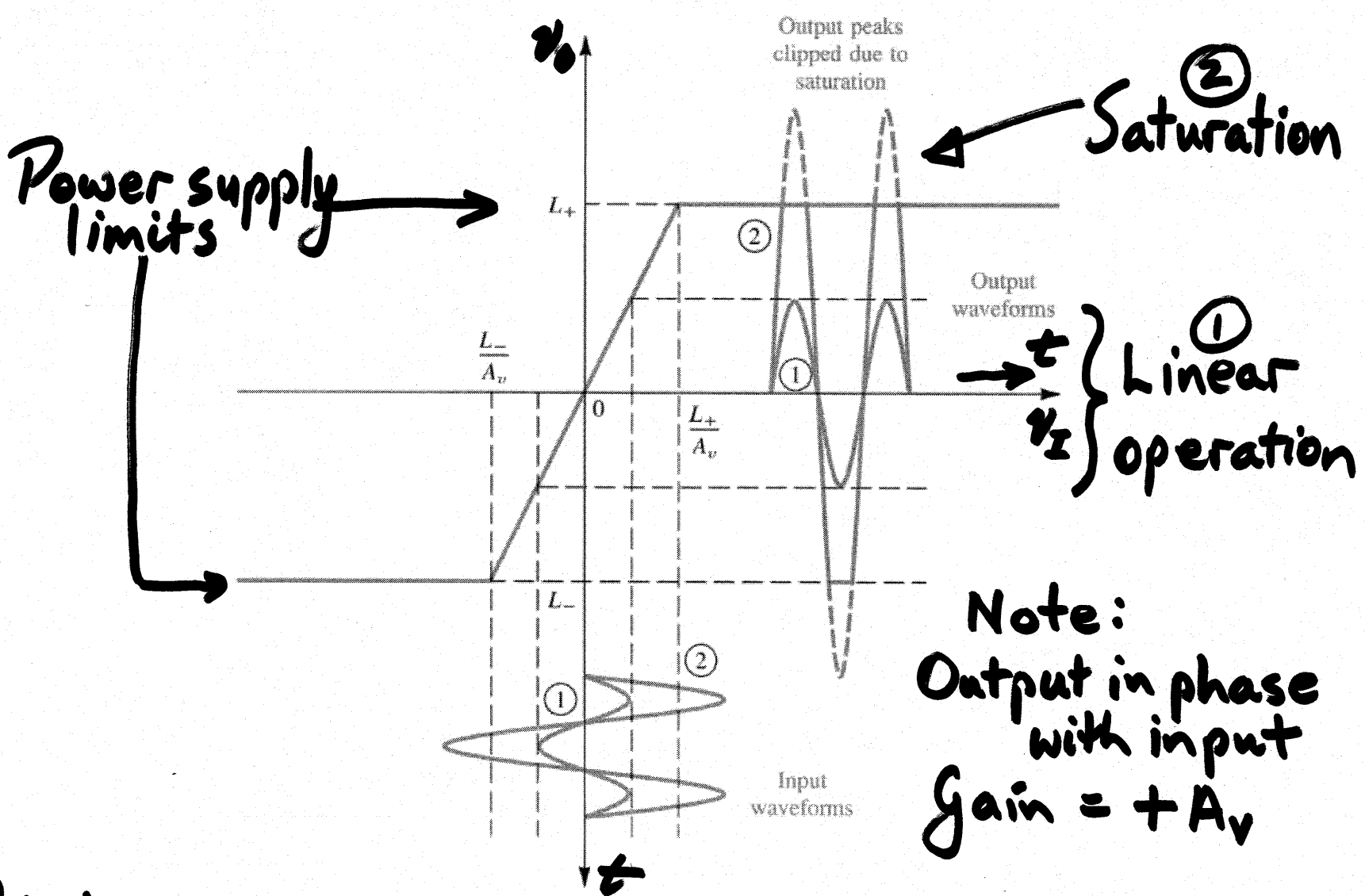
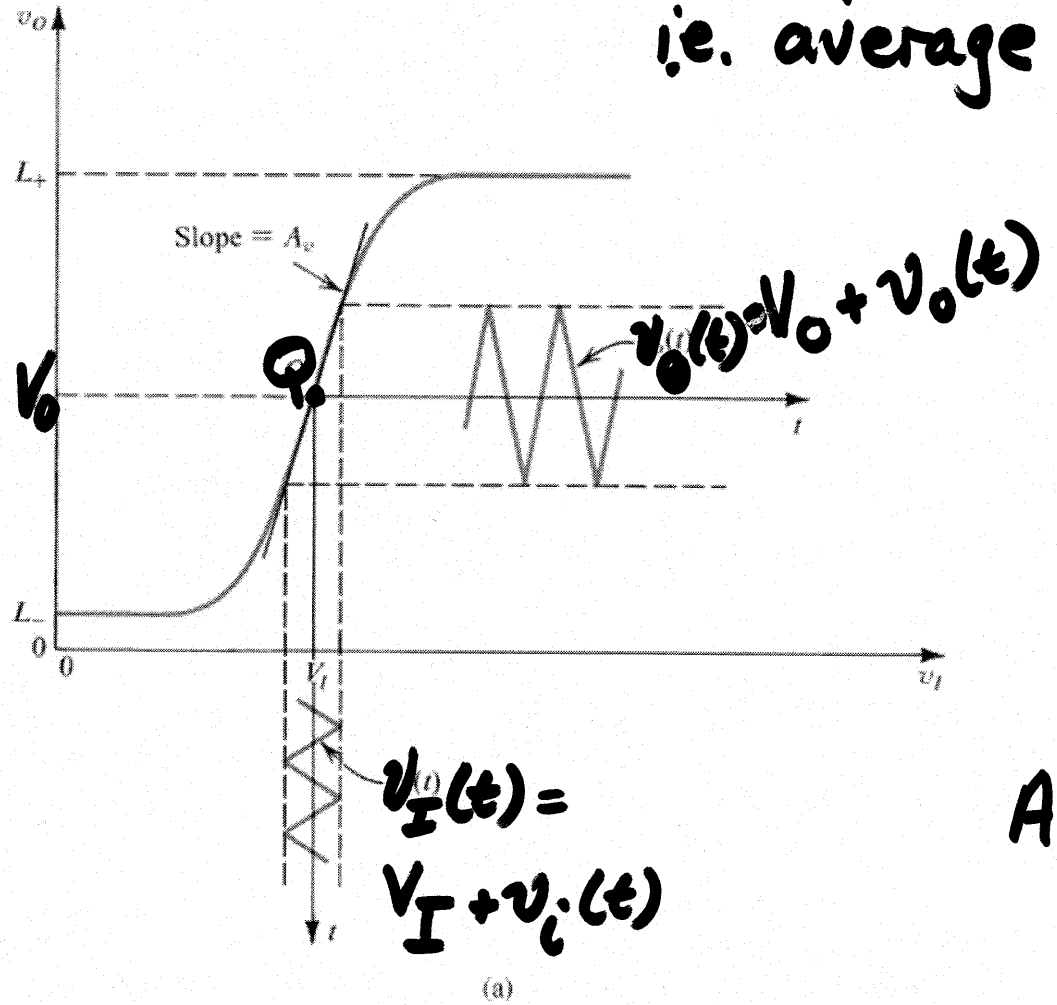


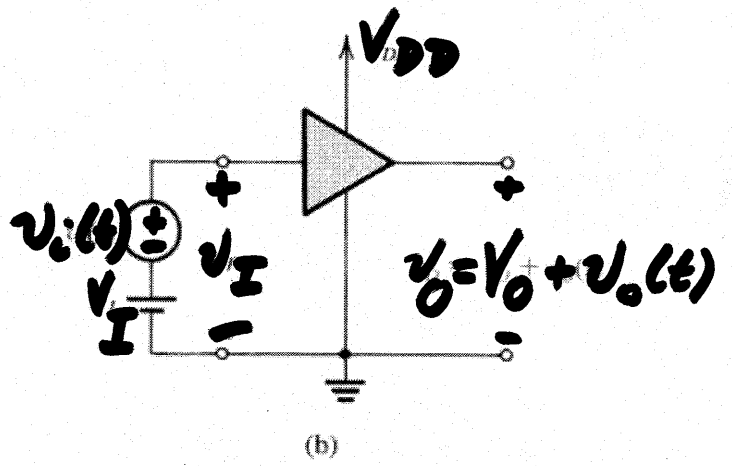
Figure 1.13 An amplifier transfer characteristic that is linear except for output saturation.

This is a common graphical visualization of the transfer characteristic with $v_I(t)$ and $v_o(t)$

Q-point = Quiescent point = Bias point = DC level
i.e. average



(a)



(b)

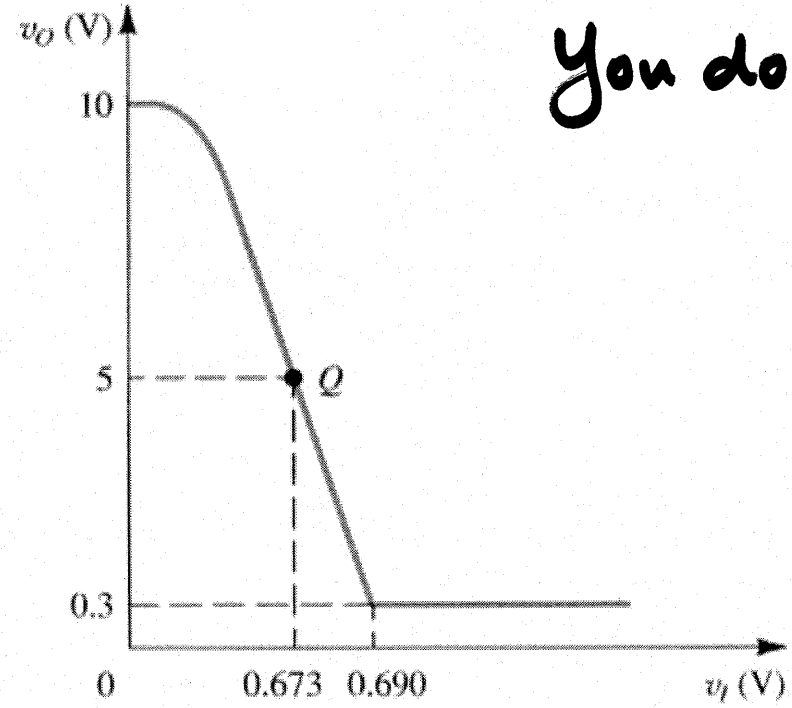
$A_v = v_o / v_i$ implies linear

$$\Rightarrow \left.\frac{dv_o}{dv_I}\right|_Q$$

Figure 1.14 **(a)** An amplifier transfer characteristic that shows considerable nonlinearity. **(b)** To obtain linear operation the amplifier is biased as shown, and the signal amplitude is kept small. Observe that this amplifier is operated from a single power supply, V_{DD}.

Example 1.2 Inverting amp:

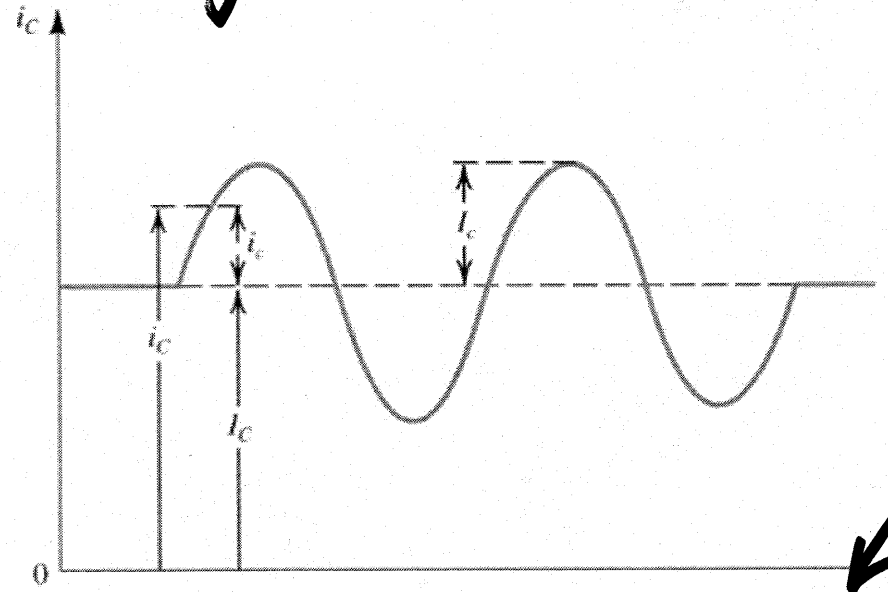
You do (or look at)



(Ex. 1.10 extends Example 1.2
Need to "plug" into equation
Figure here not accurate enough.)

Figure 1.15 A sketch of the transfer characteristic of the amplifier of Example 1.2. Note that this amplifier is inverting (i.e., with a gain that is negative).

Power supply V_{DD} & I_{DD}, etc



Average/DC

Time-varying

Instantaneous signal $i_A(t) = I_A + i_a(t)$

$= I_A + I_a \sin \omega t$

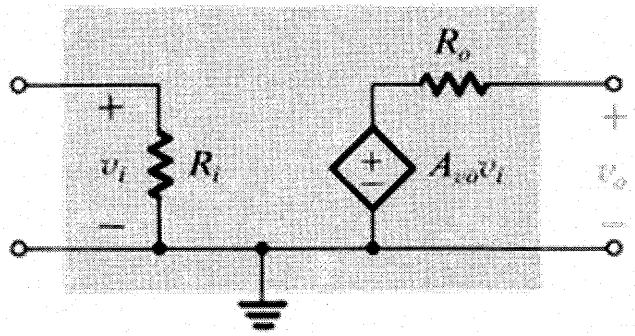
for sinusoids

Amplitude

Figure 1.16 Symbol convention employed throughout the book.

Symbol Convention

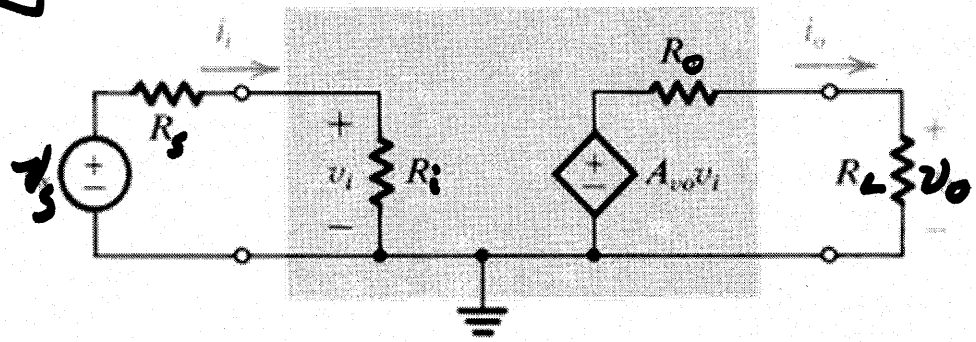
VOLTAGE AMPLIFIERS



(a)

Amp⁻ equivalent circuit:

R_i, R_o, A_{vo}



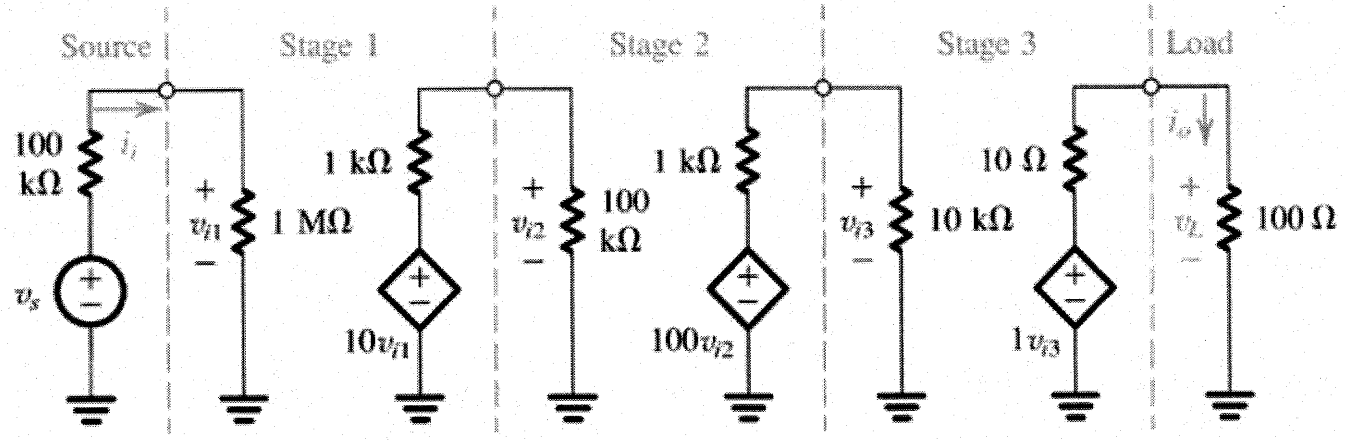
(b)

Source (Thevenin)

Load

$$v_o = \frac{R_L}{R_o + R_L} \cdot A_{vo} \frac{R_i}{R_s + R_i} v_s$$

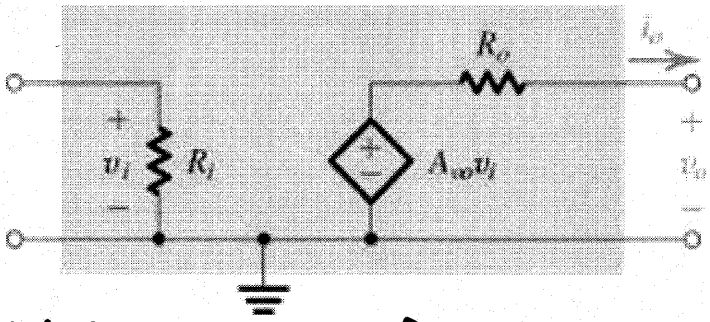
Figure 1.17 **(a)** Circuit model for the voltage amplifier. **(b)** The voltage amplifier with input signal source and load.



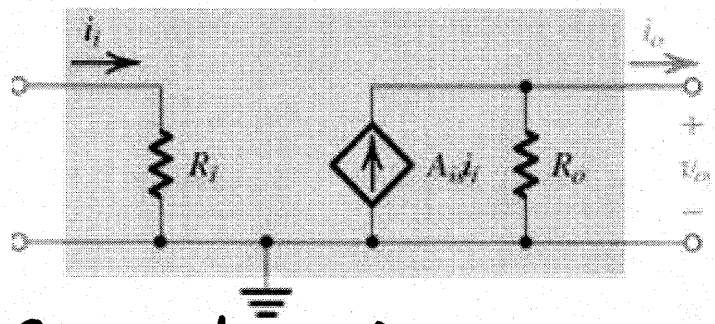
$$v_L = \frac{100}{100+10} \times 1 \times \frac{10K}{10K+1K} \times 100 \times \frac{100K}{100K+1K} \times 10 \times \frac{1M}{1M+100K} \cdot v_s$$

Figure 1.18 Three-stage amplifier for Example 1.3.

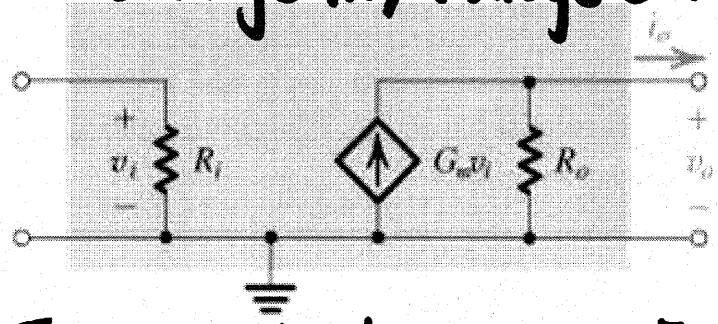
AMPLIFIER TOPOLOGIES



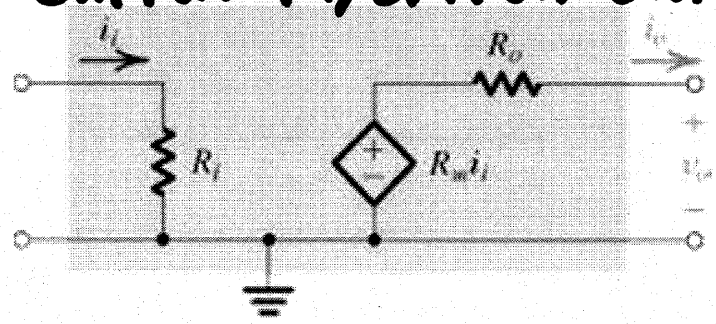
Voltage amp:
Voltage in/Voltage out



Current amp:
Current in/current out



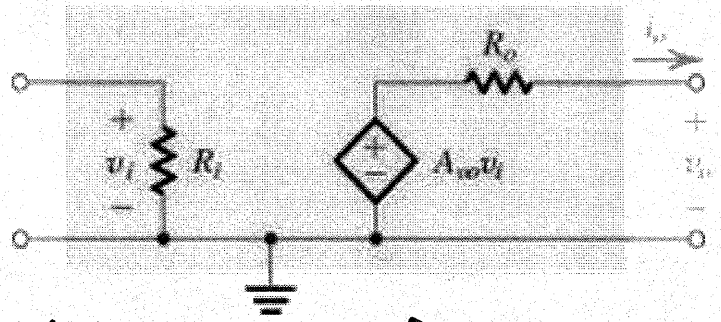
Transconductance amp:
Voltage in/current out



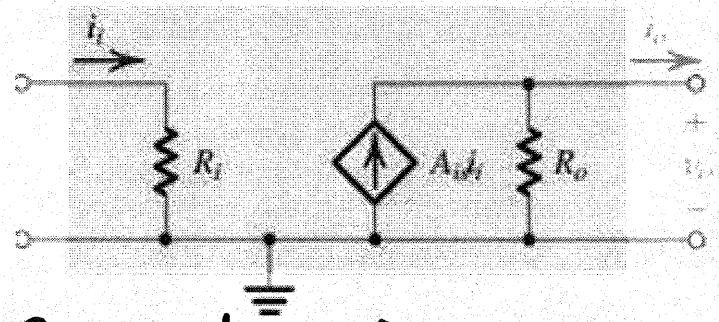
Transresistance amp:
Current in/voltage out

Table 1.1 The Four Amplifier Types

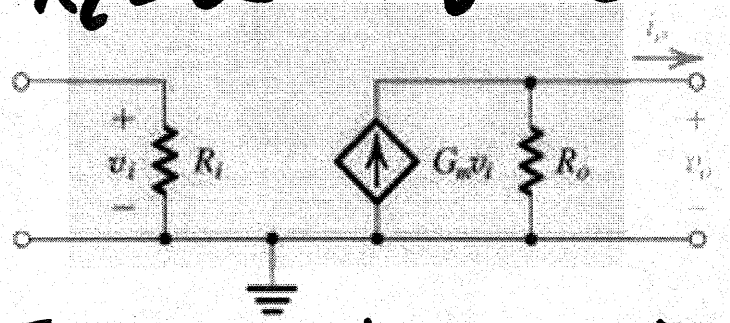
IDEAL AMPLIFIER TOPOLOGIES



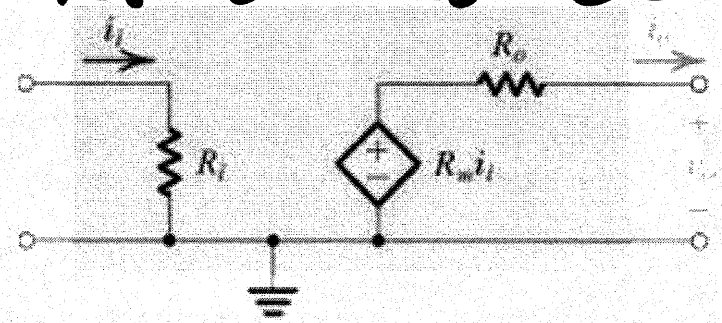
Voltage amp:
$R_i = \infty$ $R_o = 0$



Current amp:
$R_i = 0$ $R_o = \infty$



Transconductance amp:
$R_i = \infty$ $R_o = \infty$



Transresistance amp:
$R_i = 0$ $R_o = 0$

Table 1.1 The Four Amplifier Types

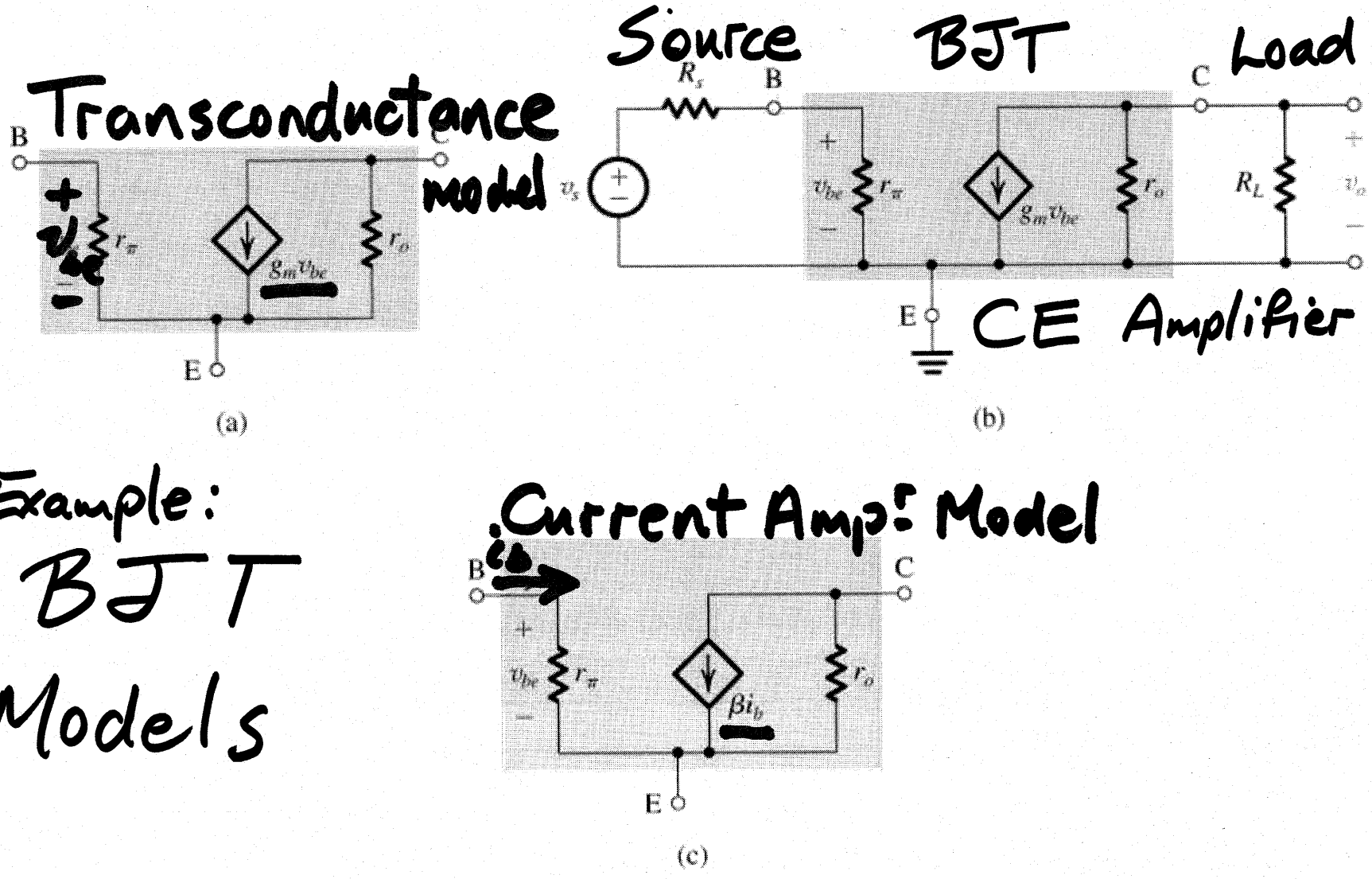
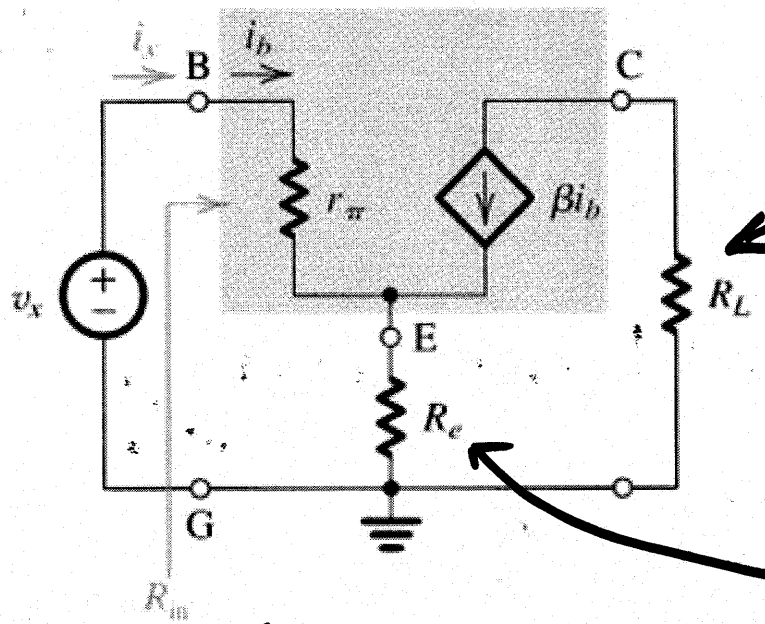


Figure 1.19 **(a)** Small-signal circuit model for a bipolar junction transistor (BJT). **(b)** The BJT connected as an amplifier with the emitter as a common terminal between input and output (called a common-emitter amplifier). **(c)** An alternative small-signal circuit model for the BJT.

Ex. 1.20 R_{in} = ? looking into Base terminal



Collector load

Emitter resistor

Figure E1.20

Apply "test voltage" v_x, so $R_{in} = v_x / i_x$

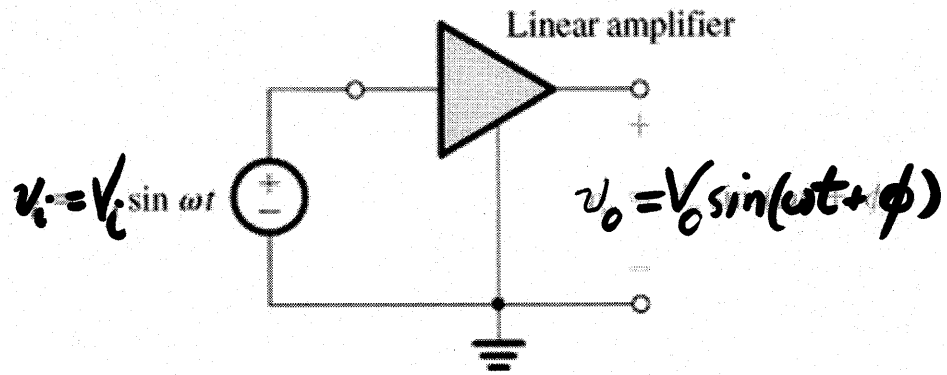
$i_b = i_x$

& $v_x = i_b r_\pi + R_e (i_b + \beta i_b)$

$= i_x [r_\pi + (1+\beta) R_e]$

$\therefore R_{in} = r_\pi + (1+\beta) R_e$

FREQUENCY RESPONSE



Specify $|T(\omega)| = V_o/V_i$

$\angle T(\omega) = \phi$

c.f. Bode plots

Figure 1.20 Measuring the frequency response of a linear amplifier. At the test frequency *v*, the amplifier gain is characterized by its magnitude (V_o/V_i) and phase *f*.

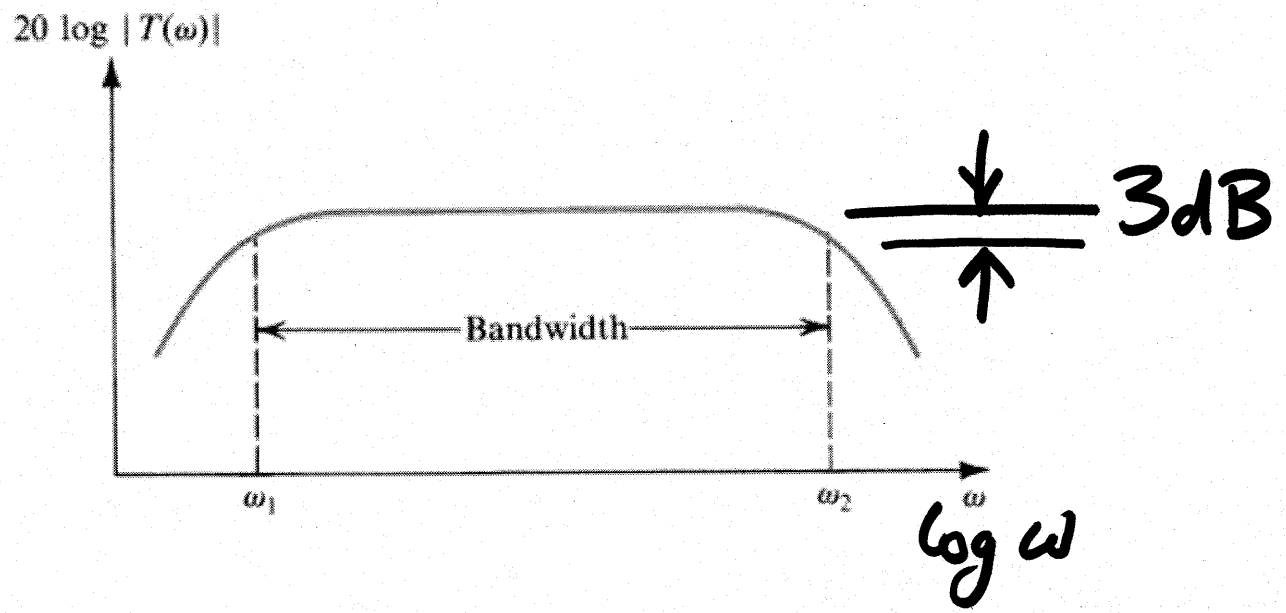
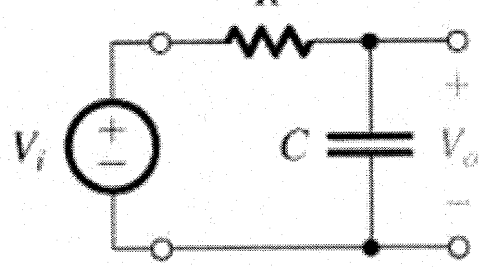


Figure 1.21 Typical magnitude response of an amplifier. $|T(V)|$ is the magnitude of the amplifier transfer function—that is, the ratio of the output $V_o(V)$ to the input $V_i(V)$.

STC Networks Appendix D

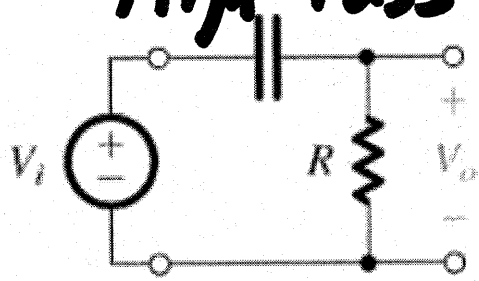
(single time constant)

Low Pass



(a)

High Pass



(b)

$$\frac{V_o}{V_i} = \frac{1}{1 + sRC} \qquad \frac{sRC}{1 + sRC} \qquad s = j\omega$$

More general for amp.'s

$$\frac{K}{1 + (s/\omega_0)} \xrightarrow{\omega \to 0} K \qquad \frac{Ks}{s + \omega_0} \xrightarrow{\omega \to \infty} K$$

Figure 1.22 Two examples of STC networks: **(a)** a low-pass network and **(b)** a high-pass network.

$$|T| = |K| / \sqrt{1 + (\omega/\omega_0)^2} \qquad |K| / \sqrt{1 + (\omega_0/\omega)^2}$$

$$\angle T = -\tan^{-1}(\omega/\omega_0) \qquad +\tan^{-1}(\omega_0/\omega)$$

$$\omega_0 = 1/RC = \frac{1}{\tau}$$

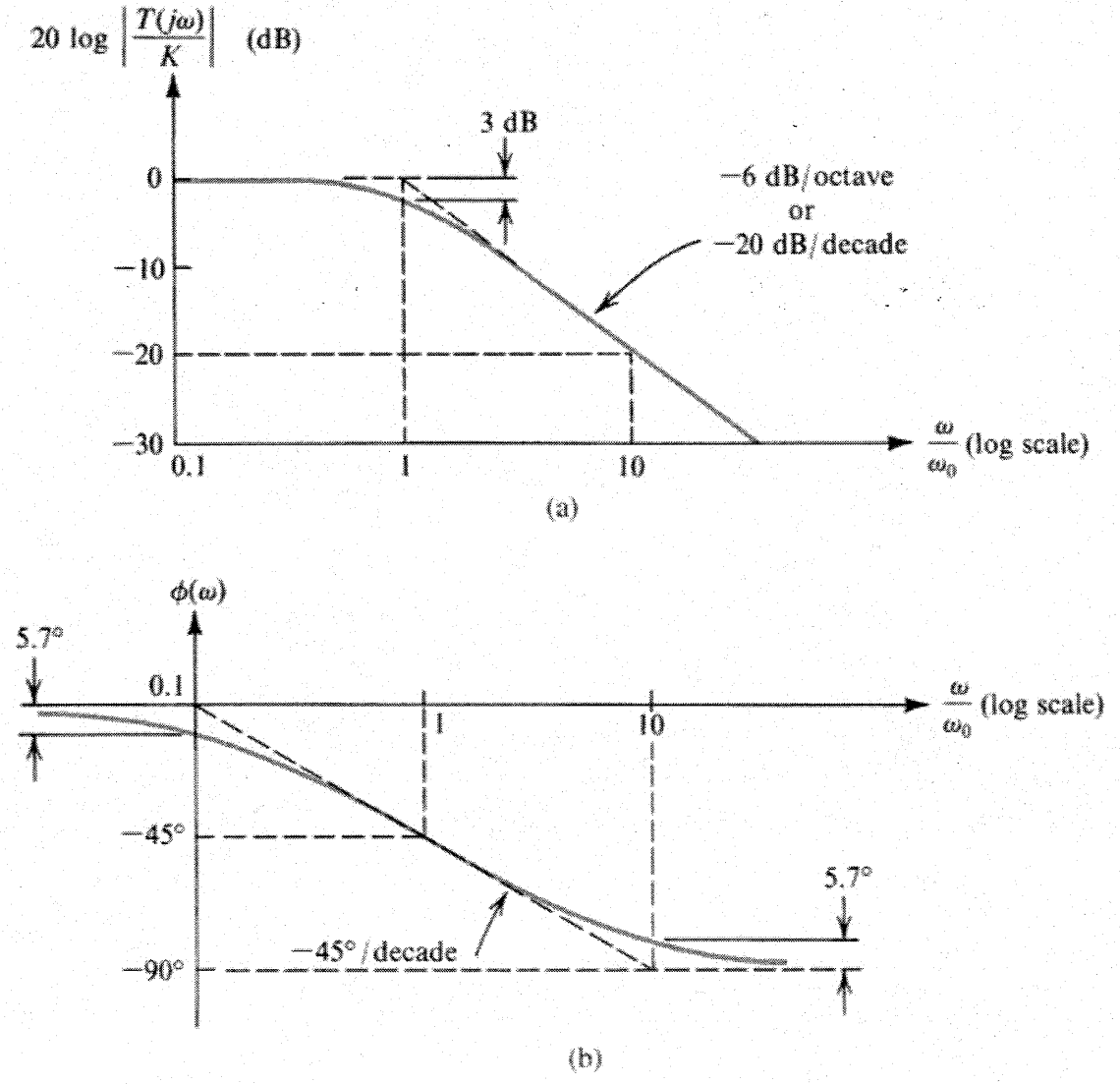


Figure 1.23 **(a)** Magnitude and **(b)** phase response of STC networks of the low-pass type.

Low Pass Bode Plots

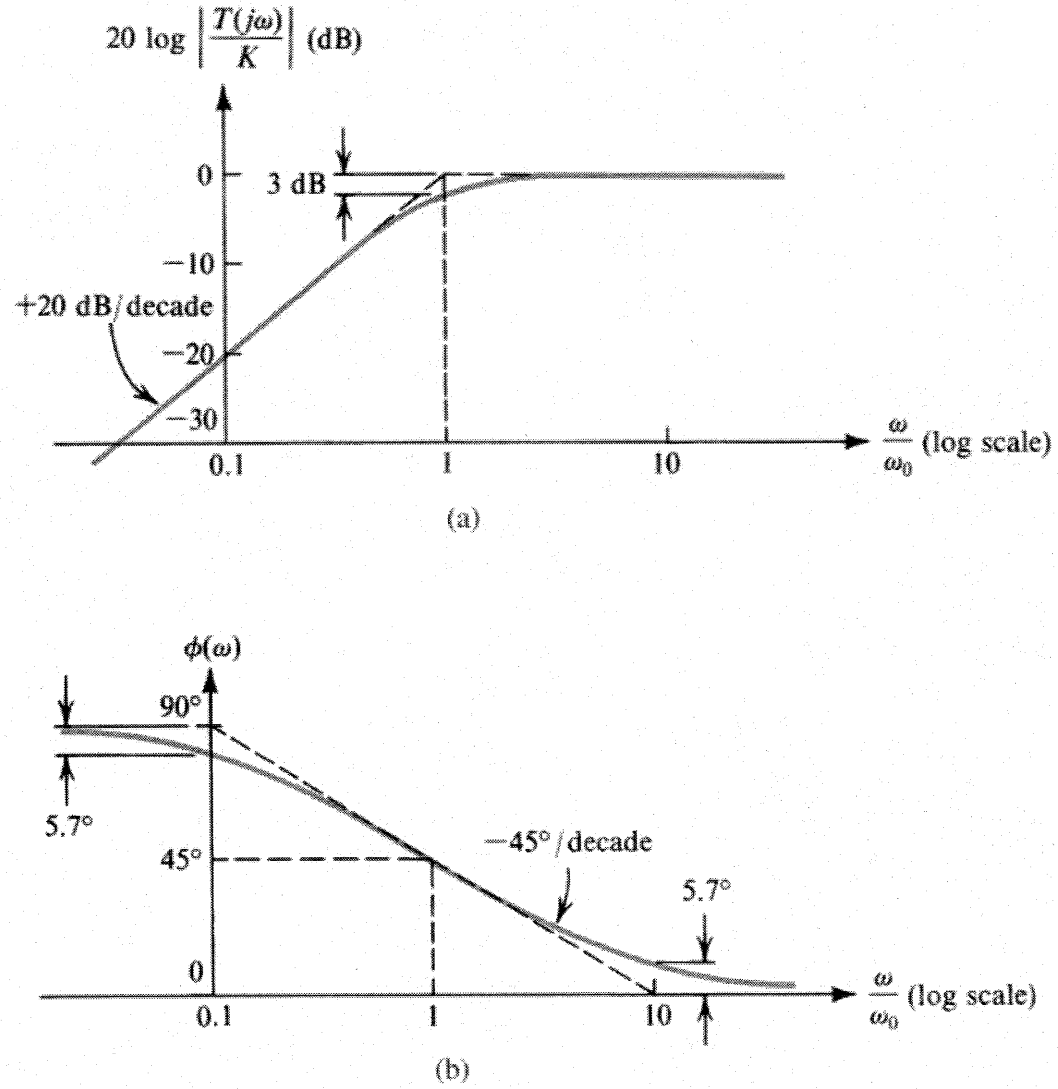
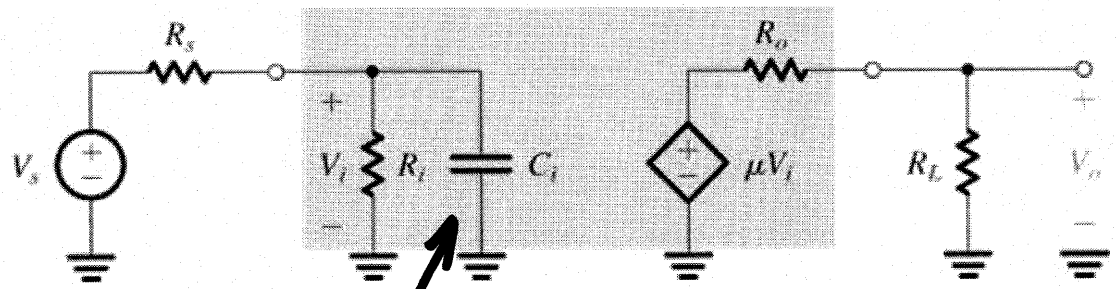


Figure 1.24 **(a)** Magnitude and **(b)** phase response of STC networks of the high-pass type.

High Pass Bode Plots

Example 1.5



At high frequency

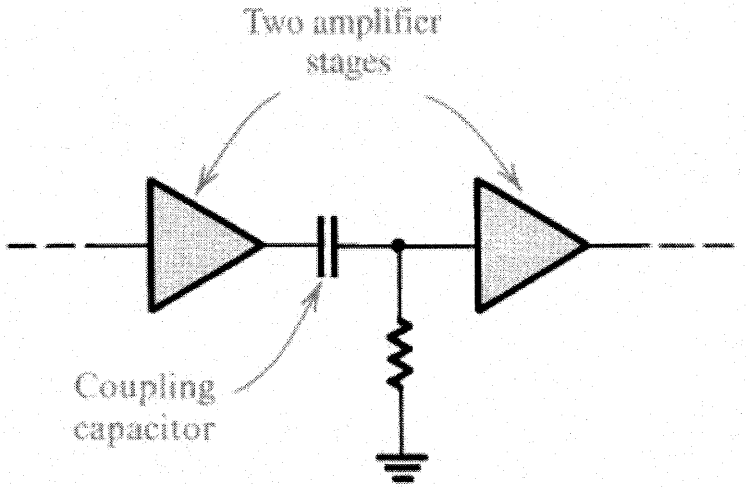
$\frac{1}{j\omega C} \rightarrow 0$, so $V_i \rightarrow 0$

so $V_o \rightarrow 0$

High frequency "roll-off"

Figure 1.25 Circuit for Example 1.5.

Capacitive Coupling



As $\omega \to 0$, $X_C = \frac{1}{\omega C} \to \infty$

∴ Coupling capacitor stops working at low frequencies.

Figure 1.27 Use of a capacitor to couple amplifier stages.

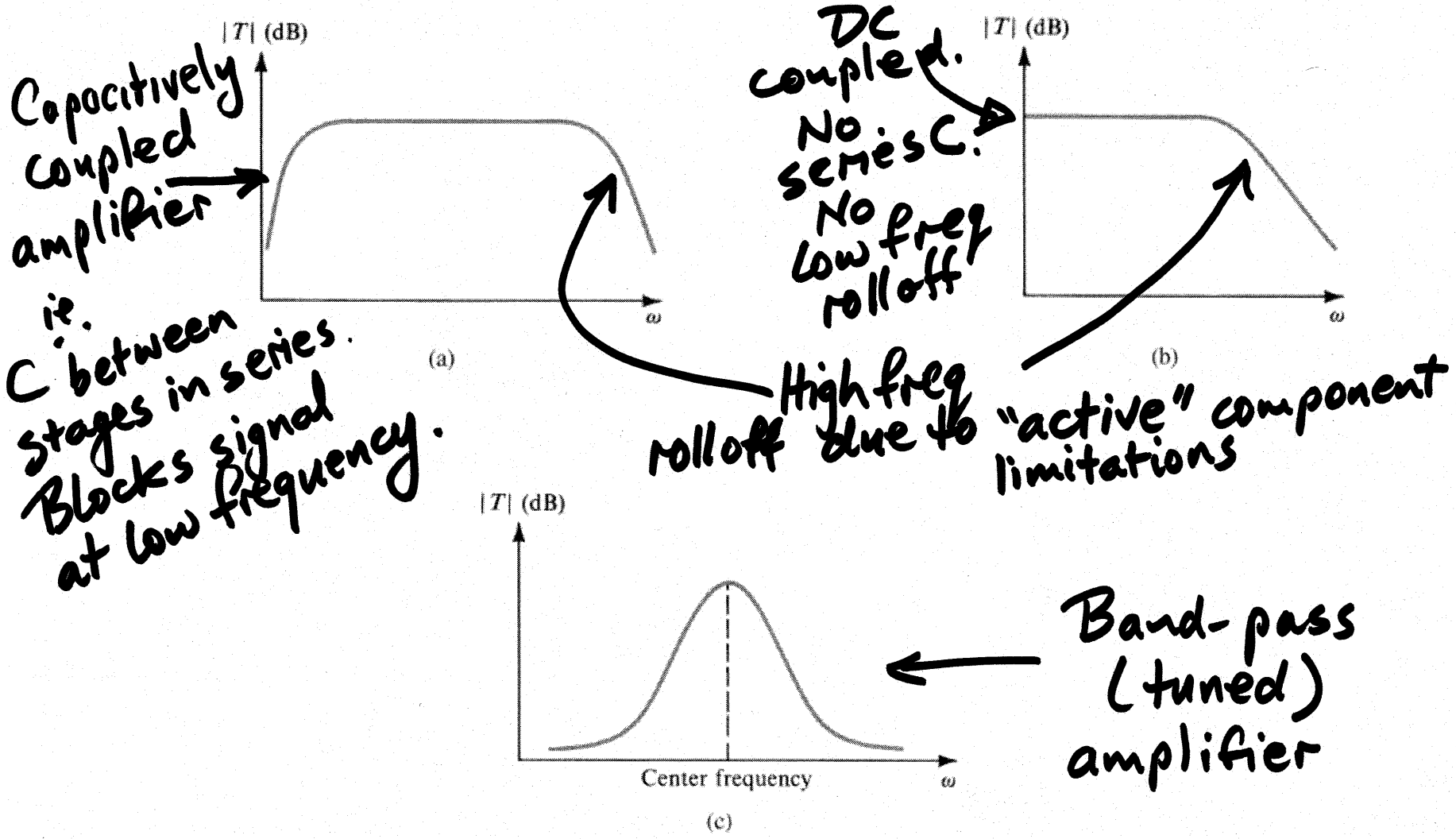


Figure 1.26 Frequency response for **(a)** a capacitively coupled amplifier, **(b)** a direct-coupled amplifier, and **(c)** a tuned or bandpass amplifier.

Ex. D1.23

Find C for $f_{3dB} < 100Hz$

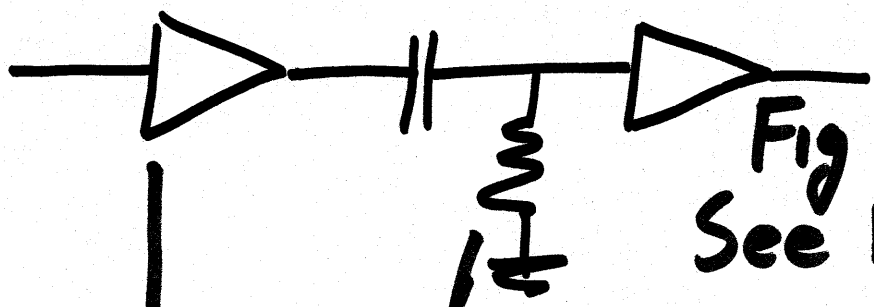


Fig 1.27
See back

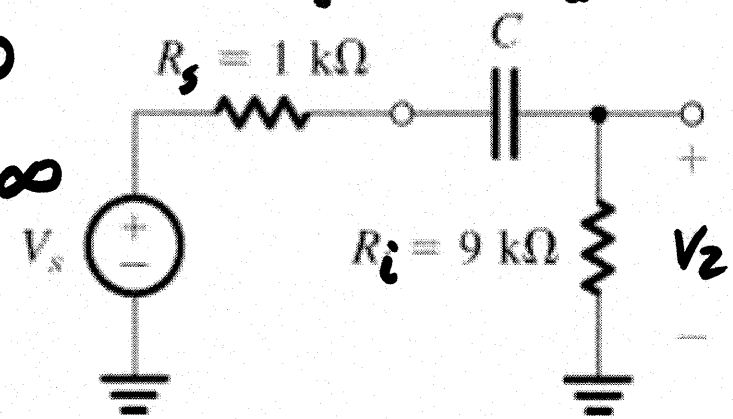


Figure E1.23

$R_i = 9K\Omega$ includes R_{in2}

$\frac{V_2}{V_s} \to 0$ as $\omega \to 0$

$\to \frac{9}{10}$ as $\omega \to \infty$

∴ High pass ckt.

$$\frac{V_2}{V_s} = \frac{9K}{9K + \frac{1}{sC} + 1K}$$

$$= \frac{9}{10} \cdot \frac{1}{1 + \frac{1}{sRC}}$$

where R = 10K

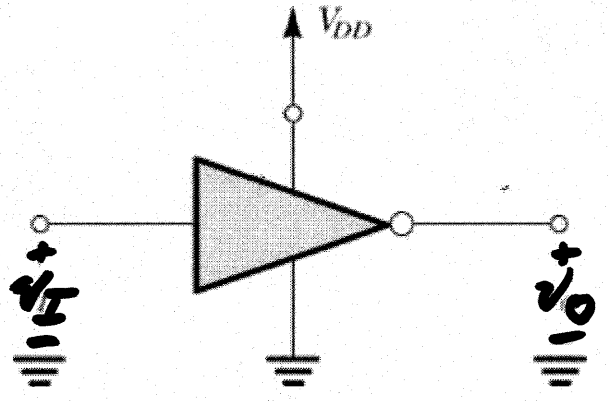
$f_{3dB} < 100Hz \longrightarrow \omega_{3dB} < 628$ rad/s

$\therefore RC \geq 1/628, \quad C \geq 10^{-4}/628$

$\approx 0.16\mu F$

Perhaps $0.18\mu F$ or $0.22\mu F$ also OK answers.

DIGITAL LOGIC INVERTER



v_I = "0" $\quad\quad$ v_O = "1"

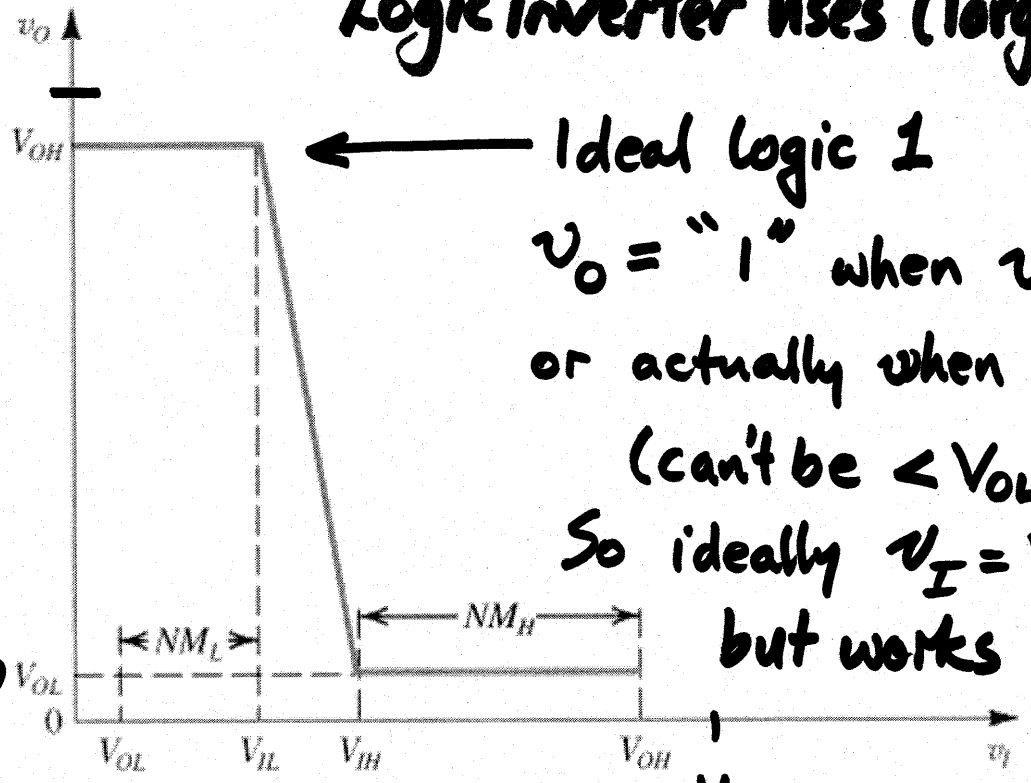
v_I = "1" $\quad\quad$ v_O = "0"

} Logic levels

Figure 1.28 A logic inverter operating from a dc supply V_{DD}.

VOLTAGE TRANSFER CHARACTERISTIC (VTC)

Note: Amplifier uses (small signal) linear range.
Logic inverter uses (large signal) saturation limits.



Ideal logic 1

v_O = "1" when v_I = "0"

or actually when $v_I = V_{OL}$ to V_{IL}

(can't be < V_{OL})

So ideally $v_I = V_{OL}$ for logic "0"

but works (i.e. $v_O = V_{OH}$ = logic "1") up to V_{IL}

Call this range "Noise margin"

$NM_L = V_{IL} - V_{OL}$

Note:

$V_{OH} \lesssim V_{DD}$

(technology dependent)

Ideal logic 0

Figure 1.29 Voltage transfer characteristic of an inverter. The VTC is approximated by three straightline segments. Note the four parameters of the VTC (V_{OH}, V_{OL}, V_{IL}, and V_{IH}) and their use in determining the noise margins (NM_H and NM_L).

Similarly $NM_H = V_{OH} - V_{IH}$ is range when input functions as "1" i.e. output "0"

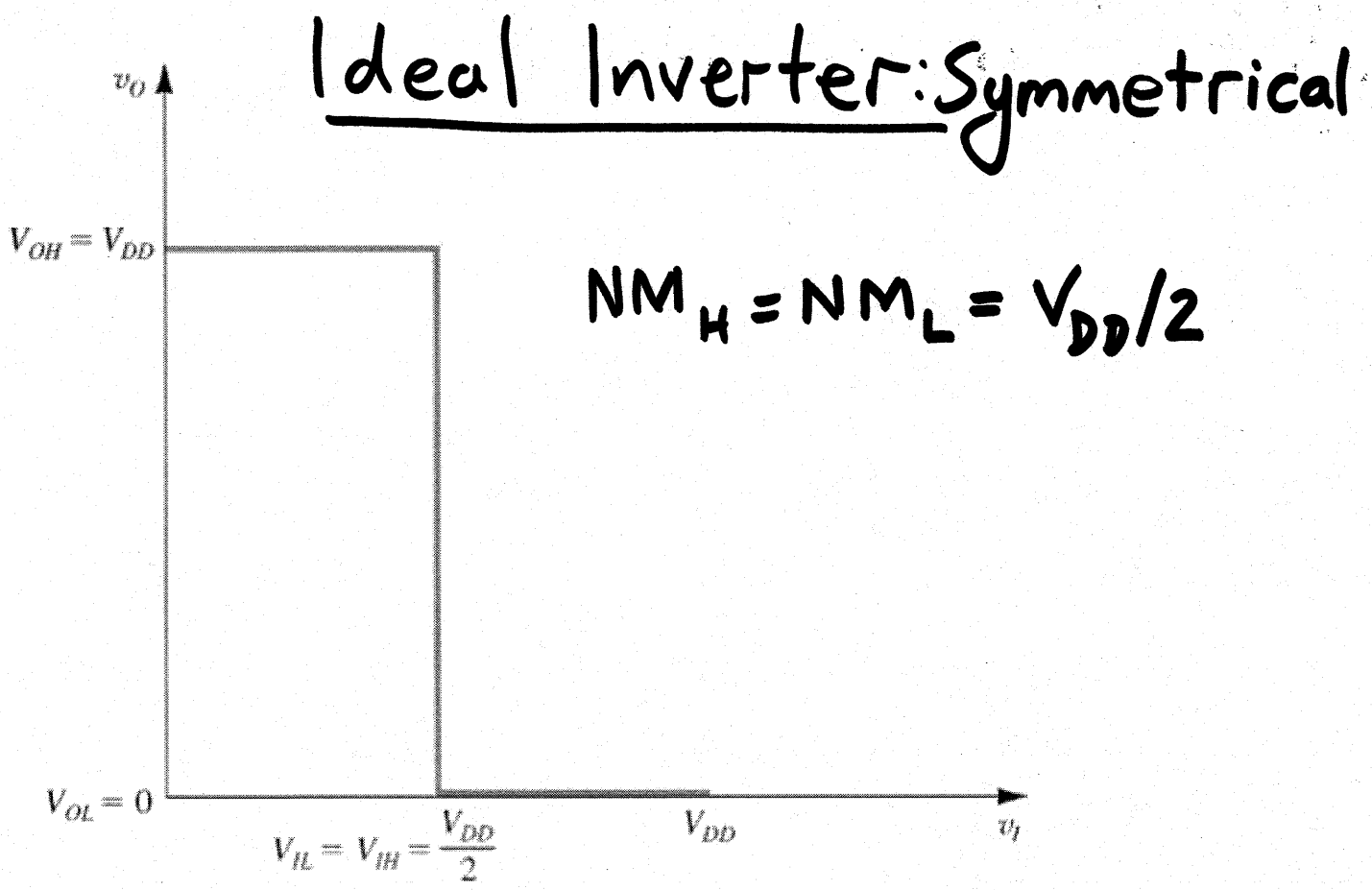


Figure 1.30 The VTC of an ideal inverter.

Inverter as Voltage Controlled Switch (VCS)

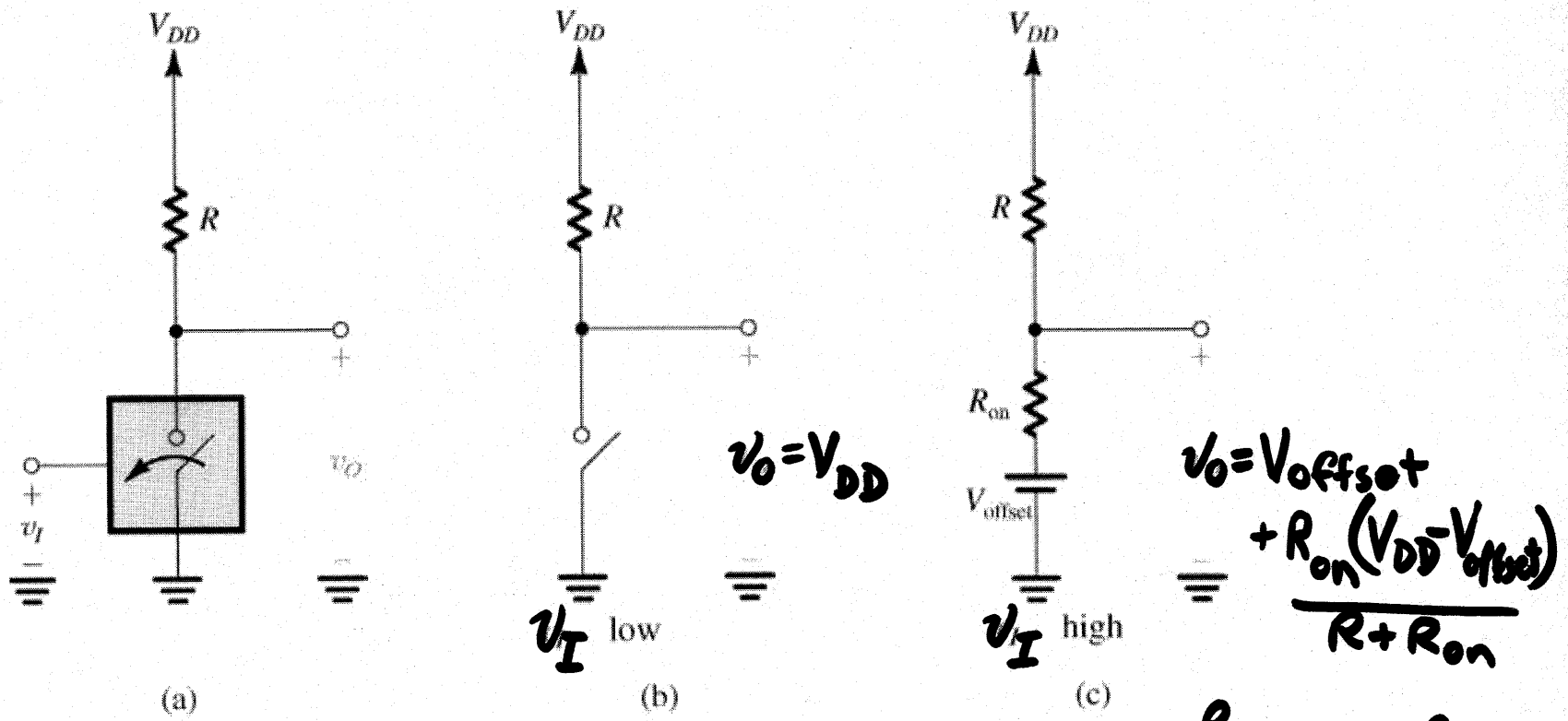


Figure 1.31 **(a)** The simplest implementation of a logic inverter using a voltage-controlled switch; **(b)** equivalent circuit when v_I is low; and **(c)** equivalent circuit when v_I is high. Note that the switch is assumed to close when v_I is high.

$R_{on} \to 0$ → V_{offset}

$V_{offset} \sim 0$ → $\frac{R_{on}}{R_{on}+R} V_{DD}$

Ex 1.24 $V_{DD} = 5v$, $R = 1K$, $R_{on} = 100\Omega$

$V_{offset} = 0.1v$, $V_{IL} = 0.8v$, $V_{IH} = 1.2v$

$V_{OH} = V_{DD} = 5v$

$$V_{OL} = \frac{R}{R+R_{on}} V_{offset} + \frac{R_{on}}{R+R_{on}} V_{DD}$$

$$= \frac{1000}{1100}(0.1) + \frac{100}{1100}(5)$$

$$= 6/11 \text{ volts} = 0.545v$$

$$NM_H = V_{OH} - V_{IH} = 5 - 1.2 = 3.8v$$

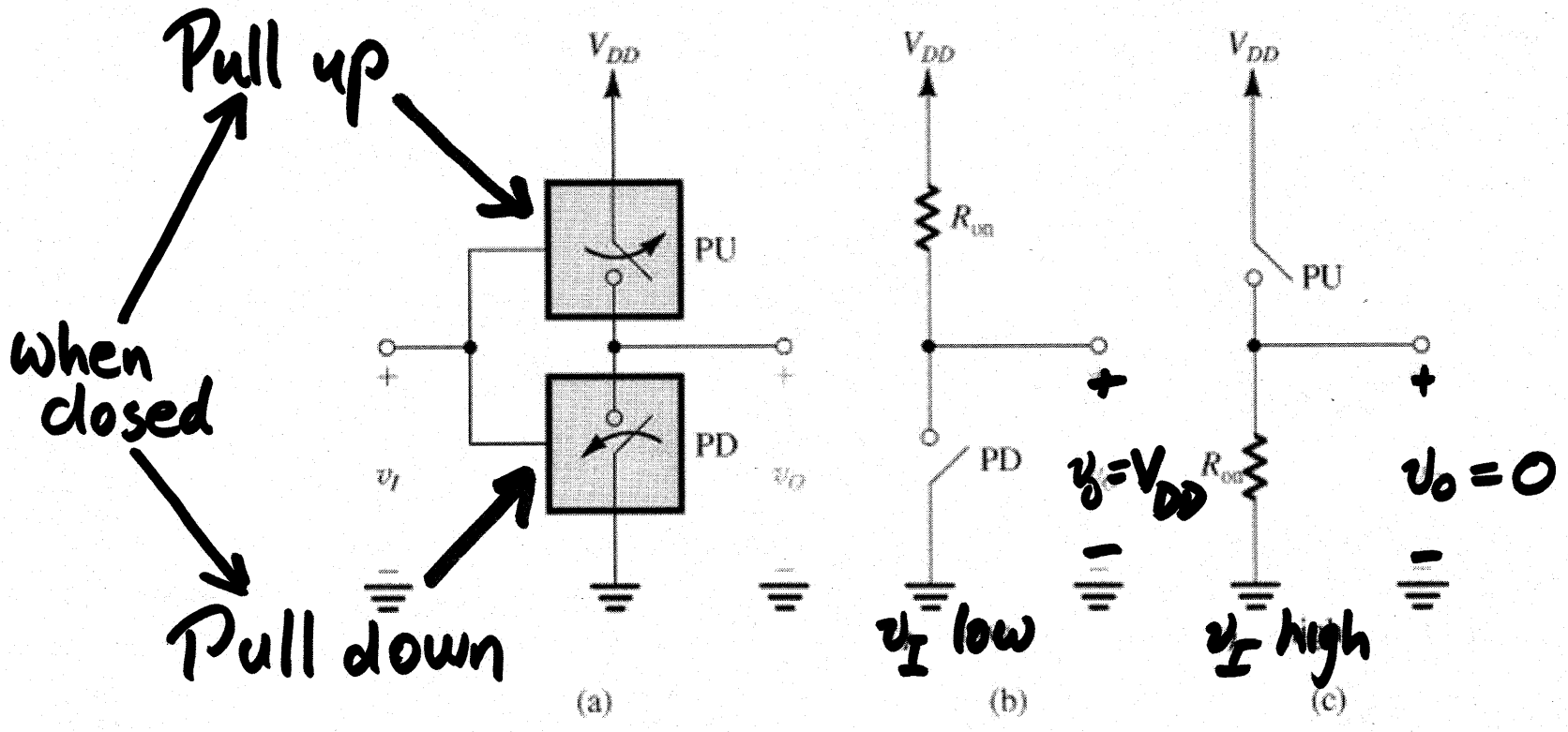
$$NM_L = V_{IL} - V_{OL} = 0.8 - 0.55 = 0.25v$$

Av. static power dissipation (Assume 50% duty cycle) $= \frac{1}{2} \times 5 \text{ volts} \left[0A + \frac{V_{DD} - V_{offset}}{R+R_{on}} \right]$

$$= 2.5(5-0.1)/(100+1000)$$

$$= \frac{2.5 \times 4.9}{1.1} mW = 11.1 mW$$

COMPLEMENTARY SWITCHES



$P_D)_{static} = 0$

Figure 1.32 A more elaborate implementation of the logic inverter utilizing two complementary switches. This is the basis of the CMOS inverter studied in Section 4.10.

e.g. CMOS

In practice, current flows each transition through linear region, so $P_D)_{dyn} \propto freq = fCV_{DD}^2$,

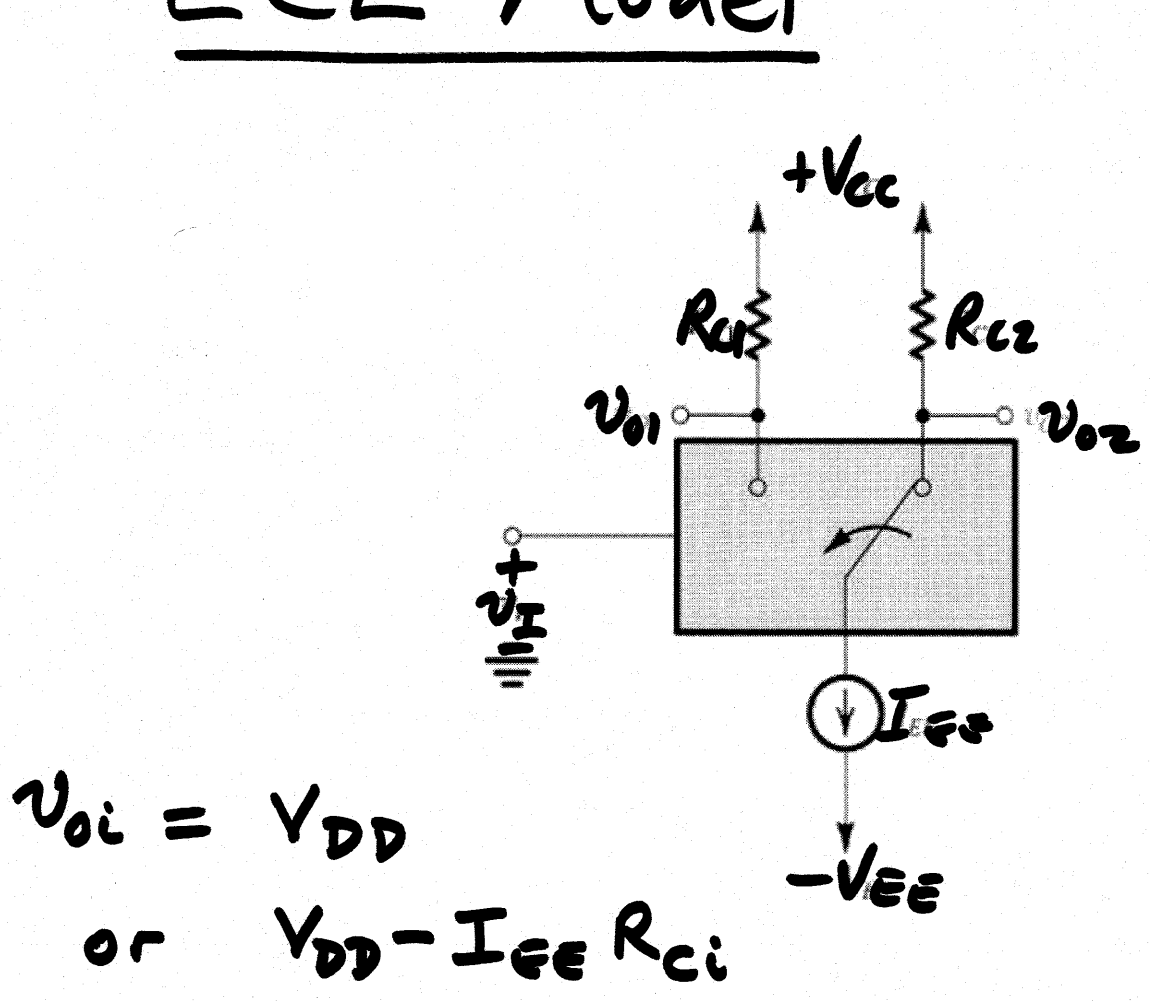
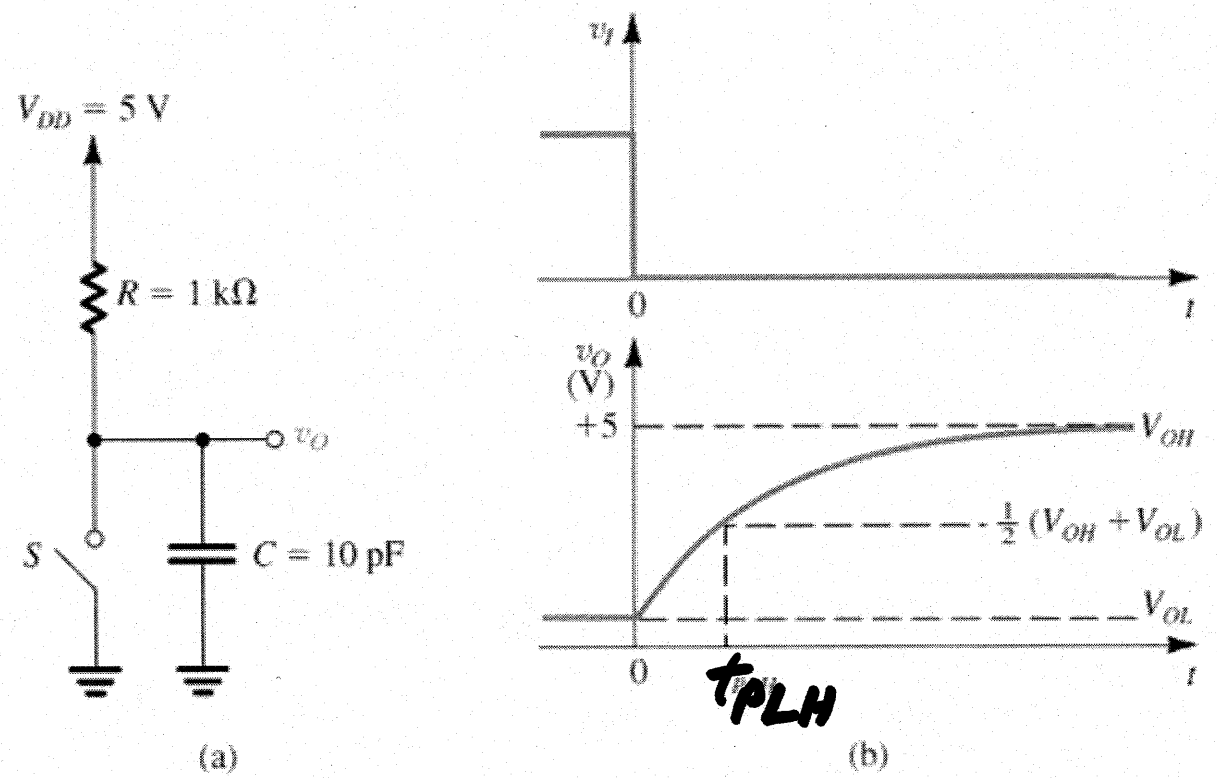


Figure 1.33 Another inverter implementation utilizing a double-throw switch to steer the constant current I_{EE} to R_{C1} (when v_I is high) or R_{C2} (when v_I is low). This is the basis of the emitter-coupled logic (ECL) studied in Chapters 7 and 11.



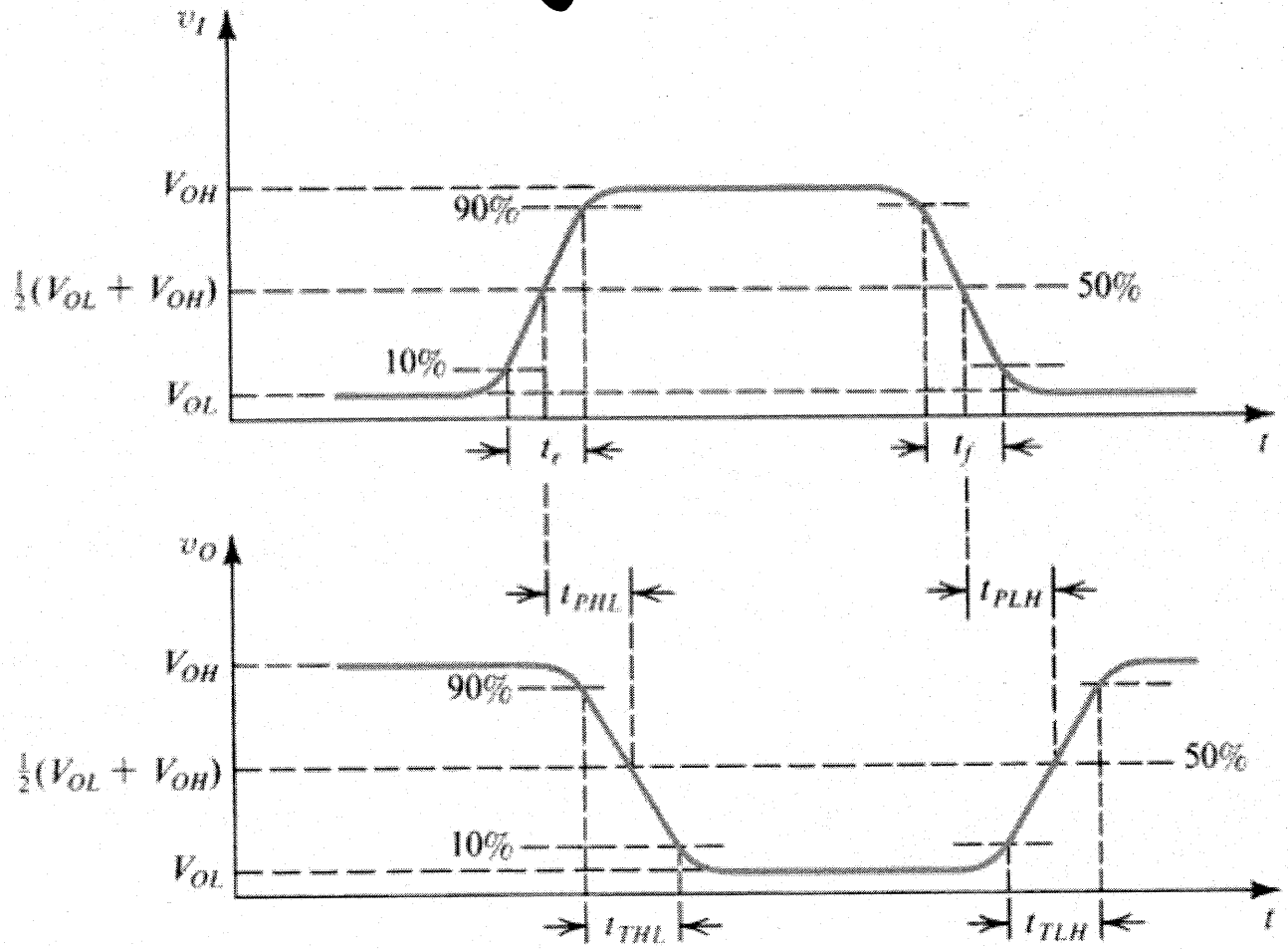
C load of next stage

Low → high propagation delay t_{PLH}

Figure 1.34 Example 1.6: **(a)** The inverter circuit after the switch opens (i.e., for $t \geq 0+$). **(b)** Waveforms of v_I and v_O. Observe that the switch is assumed to operate instantaneously. v_O rises exponentially, starting at V_{OL} and heading toward V_{OH}.

Or use $\tau \longrightarrow v_O(t) = V_{OL} + (V_{OH} - V_{OL})(1 - \exp -\frac{t}{RC})$

Risetimes/switching times → waveform shape



10%-90% risetime (& falltime)

Figure 1.35 Definitions of propagation delays and transition times of the logic inverter.

SUMMARY

- Course introduction & organization
  - texts
  - website, on-line, WebCT
  - assignment schedule, etc
- Introduction to amplifier concepts
  - Voltage gain, bias point

Voltage amplifiers:
- Models
- Topologies
- BJT CE model
- Frequency response

Digital logic inverter:
- Transfer characteristic
- Noise margins
- Power, risetimes
- CMOS & ECL models