Package Reliability
TKK 2009 Lecture 3 Part B2

James E. Morris
Dept of Electrical & Computer Engineering
Portland State University

2(a) Electromigration

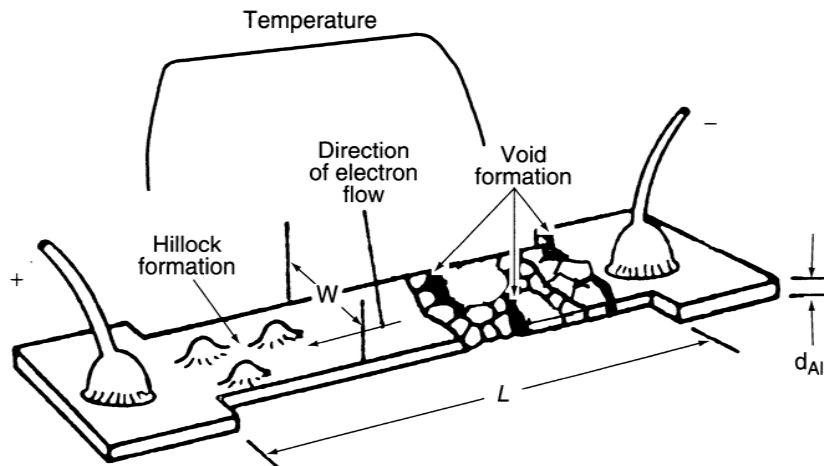


Fig. 5-15 Schematic model of damage in an interconnect subject to electromigration. Hillocks and voids develop in response to temperature gradients superimposed on the directed electron current flow.

2

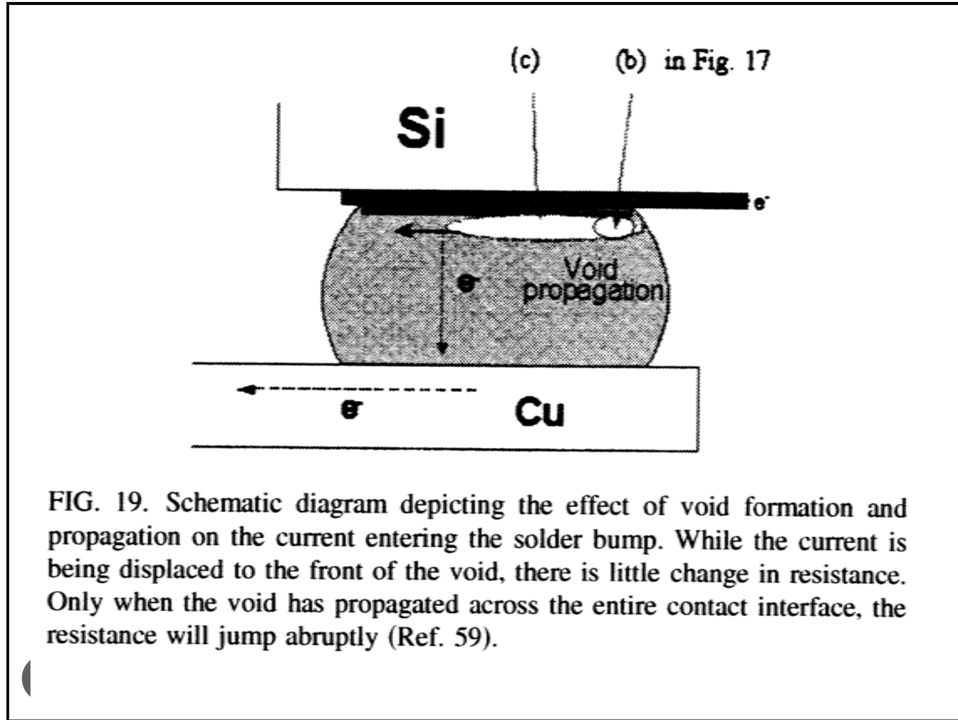


FIG. 19. Schematic diagram depicting the effect of void formation and propagation on the current entering the solder bump. While the current is being displaced to the front of the void, there is little change in resistance. Only when the void has propagated across the entire contact interface, the resistance will jump abruptly (Ref. 59).

Critical Product in Short Strip

$$J = -C\frac{D}{kT}\frac{d\sigma\Omega}{dx} + C\frac{D}{kT}Z^{*}eE$$

Jσ
Jem
Δ x
Cathode
Al
Anode
e
TiN

If J =0, there is no net electromigration flux.

$$\Rightarrow \frac{\Delta\sigma\Omega}{\Delta x} = Z^{*}e\rho j$$

E= Electric Field (E = ρj)

➡ **Critical product** $(j\Delta x)_{critical} = \frac{\Delta\sigma\Omega}{Z^{*}e\rho}$

If $j\Delta x < (j\Delta x)_c$ ⇒ No electromigration damage

Electronic Thin Film Lab — *Materials Science & Engineering, UCLA*

Small Critical Product in Solders

$$(j\Delta x)_c = \frac{\Delta \sigma\Omega}{Z^* e\rho} \Rightarrow (j\Delta x)_c = \frac{Y\Delta \varepsilon\Omega}{Z^* e\rho}$$

$\Delta\sigma = Y\Delta\varepsilon$, $\Delta\varepsilon$=0.2% at elastic limit

	Y(Gpa)	Z^*	ρ(μΩ-cm)
Solder	~30	~30	~22
Al	~69	2~4	~2
Cu	~110		

$$(j\Delta x)_{c_solder} = \frac{Y\Delta \varepsilon\Omega}{Z^* e\rho} \approx 5\times10^{-3}(j\Delta x)_{c_Cu/Al}$$

(annotations: 0.5 on Y; 10 on Z^*; 10 on ρ)

- At constant Δx, the current density needed to fail solder is **2~3 orders smaller** than that needed to fail Al or Cu
- If Al or Cu fails at 10^5 to10^6 A/cm^2, solder will fail at 10^3 or 10^4 A/cm^2

Mean Time To Failure

$$MTTF = Aj^{-n}exp\left(\frac{Q}{kt}\right)$$

n = 1.8, Q = 0.8 eV
(By Flip Chip Technologies)

(hrs)

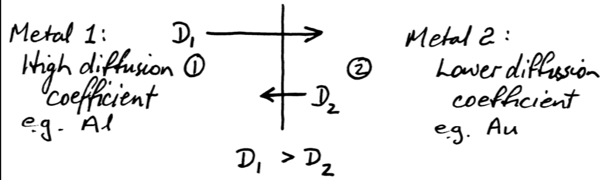
	1.5 A (1.9x10^4 A/cm^2)		1.8 A (2.25 x10^4 A/cm^2)		2.2 A (2.75 x10^{4}A/cm^2)	
	Expected	**Actual**	**Expected**	**Actual**	**Expected**	**Actual**
100 °C			**380**	**97**	**265**	**63**
125 °C	**108**	**573***	**79.6**	**43**	**55.5**	**3**
140 °C	**46**	**121**	**34**	**32**	**24**	**1**

* not failed, These MTTF are averaged value of three samples

These results show that a small increase in j and T has dramatically reduced MTTF; a unique behavior of flip chip solder joint. by W.J. Choi, UCLA

2(b) Kirkendall Voids

Interface — dissimilar metals



$D_1 > D_2$

Net effect:

① Al | Au ②

Voids develop on Metal 1 side

* High resistance interface
* Mechanically weakened
* Diffusion constants increase rapidly with temperature.
  ∴ Must keep temperatures low (temperature × time)

Also: Au/Cu → ductile intermetallics & voids → decreased bond strength

7

TABLE I. Melting point and diffusivities of Cu, Al, and eutectic SnPb.

	Melting point (K)	Temperature ratio 373 K/T m	Diffusivities at 100 °C (cm^2/s)	Diffusivities at 350 °C (cm^2/s)
Cu	1356	0.275	Lattice $D_l = 7\times10^{-28}$	$D_l = 5\times10^{-17}$
			Grain boundary $D_{gb} = 3\times10^{-15}$	$D_{gb} = 1.2\times10^{-9}$
			Surface $D_s = 10^{-12}$	$D_s = 10^{-8}$
Al	933	0.4	Lattice $D_l = 1.5\times10^{-19}$	$D_l = 10^{-11}$
			Grain boundary $D_{gb} = 6\times10^{-11}$	$D_{gb} = 5\times10^{-7}$
Eutectic SnPb	456	0.82	Lattice $D_l = 2\times10^{-9} - 2\times10^{-10}$	Molten state $D_l > 10^{-5}$

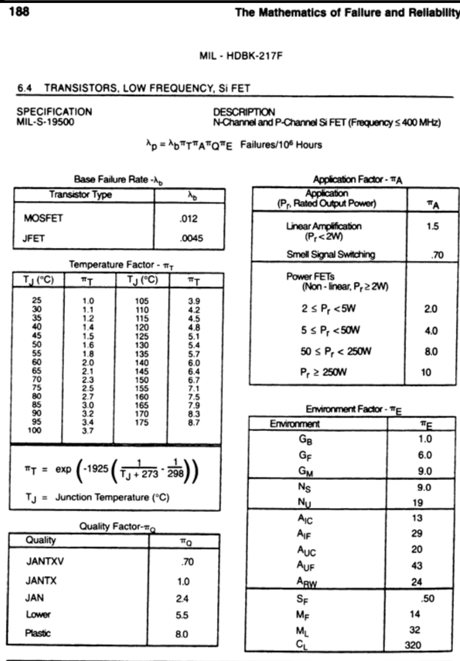
8

4/21/2009

4. MIL-HDBK-217

Standards for microelectronics reliability evaluation under various device categories

Example:- M. Ohring



188 The Mathematics of Failure and Reliability

MIL - HDBK-217F

6.4 TRANSISTORS, LOW FREQUENCY, Si FET

SPECIFICATION
MIL-S-19500

DESCRIPTION
N-Channel and P-Channel Si FET (Frequency ≤ 400 MHz)

$\lambda_p = \lambda_b \pi_T \pi_A \pi_Q \pi_E$ Failures/10^6 Hours

Base Failure Rate - λ_b

Transistor Type	λ_b
MOSFET	.012
JFET	.0045

Temperature Factor - π_T

T_J (°C)	π_T	T_J (°C)	π_T
25	1.0	105	3.9
30	1.1	110	4.2
35	1.2	115	4.5
40	1.4	120	4.8
45	1.5	125	5.1
50	1.6	130	5.4
55	1.8	135	5.7
60	2.0	140	6.0
65	2.1	145	6.4
70	2.3	150	6.7
75	2.5	155	7.1
80	2.7	160	7.5
85	3.0	165	7.9
90	3.2	170	8.3
95	3.4	175	8.7
100	3.7		

$$\pi_T = \exp\left(-1925\left(\frac{1}{T_J + 273} - \frac{1}{298}\right)\right)$$

T_J = Junction Temperature (°C)

Quality Factor - π_Q

Quality	π_Q
JANTXV	.70
JANTX	1.0
JAN	2.4
Lower	5.5
Plastic	8.0

Application Factor - π_A

Application (P_r, Rated Output Power)	π_A
Linear Amplification (P_r < 2W)	1.5
Smell Signal Switching	.70
Power FETs (Non - linear, $P_r \geq 2W$)	
$2 \leq P_r < 5W$	2.0
$5 \leq P_r < 50W$	4.0
$50 \leq P_r < 250W$	8.0
$P_r \geq 250W$	10

Environment Factor - π_E

Environment	π_E
G_B	1.0
G_F	6.0
G_M	9.0
N_S	9.0
N_U	19
A_{IC}	13
A_{IF}	29
A_{UC}	20
A_{UF}	43
A_{RW}	24
S_F	.50
M_F	14
M_L	32
C_L	320

6-8

Fig. 4-6 Failure rate for low-frequency field-effect transistors. Page 6-8 reproduced from MIL-HDBK-217F.

9

Physics of Failure vs MIL-HDBK-217

Above: λ_p = .012 x 1.1 x 8.0 x .50 x .70

= 0.037 failures per 10^6 hours

i.e. 37 FITs (failures per 10^9 hours)

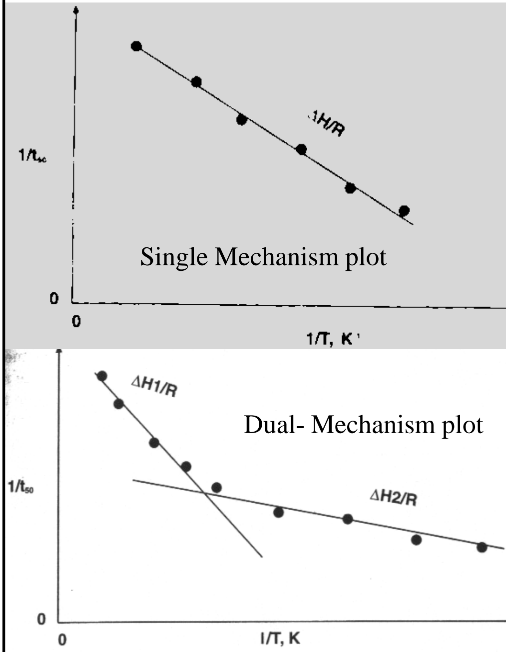
MIL-HDBK-217 often orders out in predictions

Physics of Failure:

Computer modeling based on experimental data

10 4/21/2009

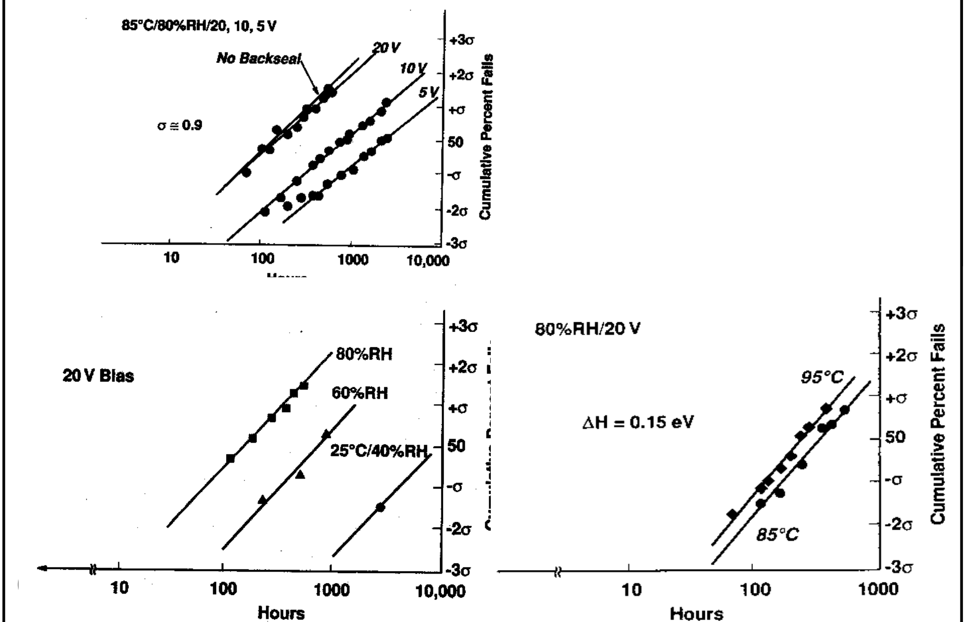
5(a) Corrosion



- Electrochemical corrosion
- Vapor pressure enhanced
- Surface porosity
- Voltage effects
- Chloride concentration
- Diffusion controlled
- Effects of hermeticity
  - Corrosion/Migration/Fatigue
- Relative humidity

4/21/2009

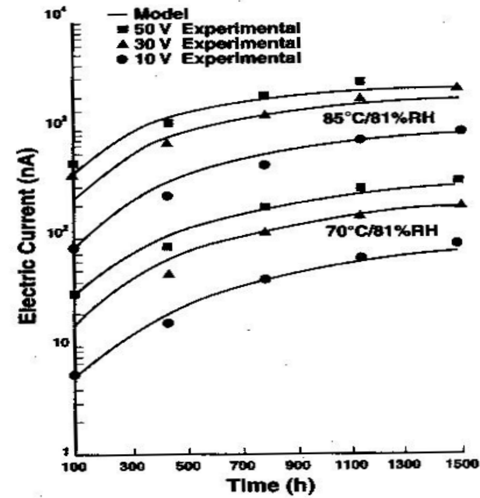
5(b) Wet Migration e.g. Ag migration



Migration through polymeric films

- *When the thin-film conductors are coated with a polymer*: one has to deal with current leakages that increases as the function of time as interface degradation occurs between the polymer and the substrate, the chip, or the metal circuitry.

Epoxy: Electric leakage current vs time at 81%RH



13

Dry Migration

- *Dry migration through glass* occurs at higher temperature and voltage conditions compared with wet migration.
- e.g. Ag ion migration under driving force of an electric field have been observed to diffuse through borosilicate glass and form dendritic growths with activation energies on the order of 1.0 to 1.3 eV.

14

4/21/2009

6(a) Popcorn Failure

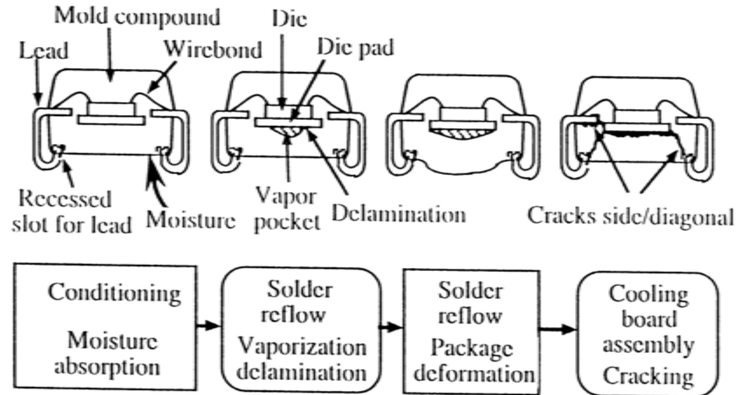
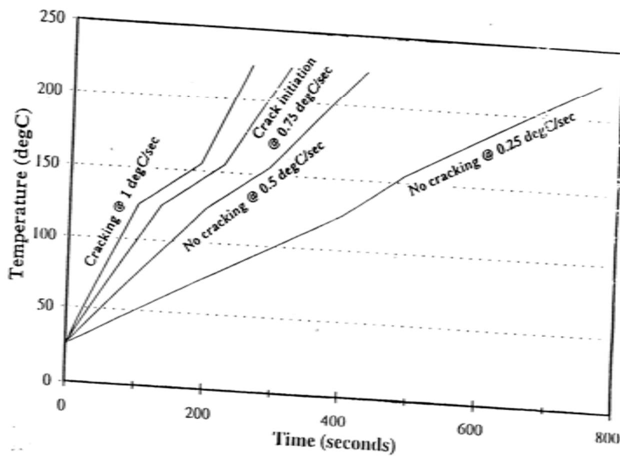


Figure 4.12 *Conditions leading to package popcorning during assembly [Nguyen 1993]*

Optimum reflow temperature ramp rates

Here, a ramp rate between 0.50 and 0.75°C/sec was found to be optimum for devices preconditioned at Level-1.



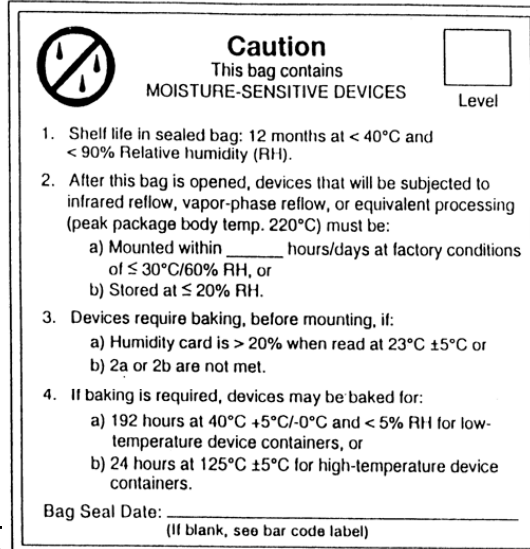
Packing Materials

Caution label

Affixed to the outside surface of the moisture barrier bag.

The label provides:

- Factory seal date
- Shelf life in bag
- Shelf life out of bag (classification level)
- Baking instructions



Caution
This bag contains
MOISTURE-SENSITIVE DEVICES

Level

1. Shelf life in sealed bag: 12 months at < 40°C and < 90% Relative humidity (RH).
2. After this bag is opened, devices that will be subjected to infrared reflow, vapor-phase reflow, or equivalent processing (peak package body temp. 220°C) must be:
   a) Mounted within ______ hours/days at factory conditions of ≤ 30°C/60% RH, or
   b) Stored at ≤ 20% RH.
3. Devices require baking, before mounting, if:
   a) Humidity card is > 20% when read at 23°C ±5°C or
   b) 2a or 2b are not met.
4. If baking is required, devices may be baked for:
   a) 192 hours at 40°C +5°C/-0°C and < 5% RH for low-temperature device containers, or
   b) 24 hours at 125°C ±5°C for high-temperature device containers.

Bag Seal Date: ______________________
(If blank, see bar code label)

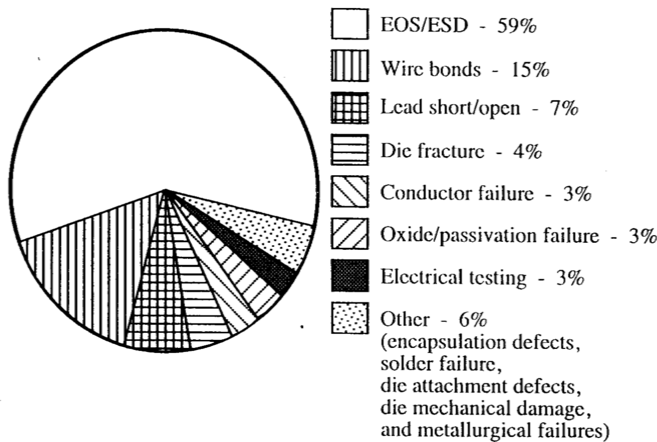
IPC-786-005

6(b) Dry Packing

17 4/21/2009

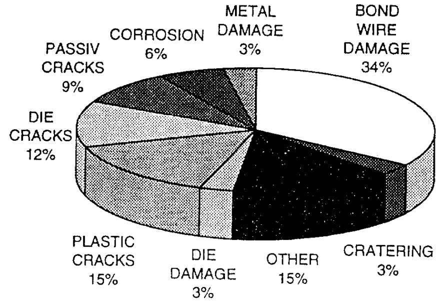
7. Distribution of Failures: Commercial integrated circuits (PEMs)

FAILURE MECHANISMS, SITES, AND MODES

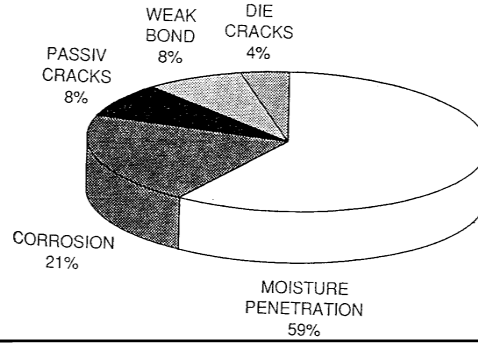


18 ..1/2009

Temperature Cycle Failures



HAST Failures:1988-1994



19