Electronics Packaging
TKK 2009 Lecture 1

James E. Morris
Dept of Electrical & Computer Engineering
Portland State University

Tuesday Lecture
April 7: Introduction
April 21: Package Reliability
April 28: Electrically Conductive Adhesives II

Friday Lecture
April 17: Electrical Package Design
April 24: Electrically Conductive Adhesives I

Download course notes from: http://www.ece.pdx.edu/~jmorris/TKK/UG

e-mail: jmorris@cecs.pdx.edu

7 April 2009 Electronics Packaging TKK 2009
Lecture 1  Introduction

• The package roadblock to system performance

• What is packaging?

• Packaging technologies
Figure 1. IC Feature Gate Size
Why is Packaging Important?

- Elementary example:

```
<table>
<thead>
<tr>
<th></th>
<th>1980</th>
<th>1990</th>
</tr>
</thead>
<tbody>
<tr>
<td>Feature size</td>
<td>4 μm</td>
<td>1 μm</td>
</tr>
<tr>
<td>Chip area</td>
<td>0.3 cm²</td>
<td>1.5 cm²</td>
</tr>
<tr>
<td>Gates/chip</td>
<td>5,000</td>
<td>100,000</td>
</tr>
<tr>
<td>μP clock freq</td>
<td>6 MHz</td>
<td>40 MHz</td>
</tr>
<tr>
<td>Power</td>
<td>2W</td>
<td>10 W</td>
</tr>
<tr>
<td>I/O count</td>
<td>64</td>
<td>1500</td>
</tr>
</tbody>
</table>
```

**Chip density, power, speed**

```
<table>
<thead>
<tr>
<th></th>
<th>1980</th>
<th>1990</th>
</tr>
</thead>
<tbody>
<tr>
<td>Ckt size</td>
<td>L²</td>
<td>4μ→1μ</td>
</tr>
<tr>
<td>Chip size</td>
<td>0.3cm²</td>
<td>5xArea→ 1.5cm²</td>
</tr>
<tr>
<td>Ckts/chip</td>
<td>N</td>
<td>5x16N=80N (20N)</td>
</tr>
<tr>
<td>Pwr diss</td>
<td>2w</td>
<td>I→4÷80x2w/4=40w (10w)</td>
</tr>
<tr>
<td>Clk freq</td>
<td>6MHz</td>
<td>C/16, I/4</td>
</tr>
</tbody>
</table>
```
### ITRS product categories

<table>
<thead>
<tr>
<th>Product category</th>
<th>Product description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Low cost</td>
<td>&lt;$ 300: consumer products, microcontrollers, disk drivers</td>
</tr>
<tr>
<td>Hand-held</td>
<td>&lt;$ 1000: battery powered products e.g. mobile and cellular products</td>
</tr>
<tr>
<td>Cost/performance</td>
<td>&lt;$3000: notebooks, desktop personal computers</td>
</tr>
<tr>
<td>High performance</td>
<td>&gt;$3000: high-end workstations, servers, avionics, supercomputer</td>
</tr>
<tr>
<td>Harsh environment</td>
<td>Under-the-hood and other hostile environment products</td>
</tr>
<tr>
<td>Memory</td>
<td>DRAM’s, SRAM’s</td>
</tr>
</tbody>
</table>

---

### ITRS Packaging requirements

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Feature Size (μm)</td>
<td>0.5</td>
<td>0.35</td>
<td>0.25</td>
<td>0.18</td>
<td>0.12</td>
<td>0.07</td>
</tr>
<tr>
<td>Gates/chip</td>
<td>300K</td>
<td>800K</td>
<td>2M</td>
<td>5M</td>
<td>10M</td>
<td>100M</td>
</tr>
<tr>
<td>Transistors (cm⁻²)</td>
<td>0.01B</td>
<td>0.04B</td>
<td>0.1B</td>
<td>0.22B</td>
<td>0.6B</td>
<td>2.1B</td>
</tr>
<tr>
<td>Chip Size (mm²)</td>
<td>250</td>
<td>400</td>
<td>600</td>
<td>800</td>
<td>1000</td>
<td>1250</td>
</tr>
<tr>
<td>Logic/Uniprocessor</td>
<td>132</td>
<td>200</td>
<td>320</td>
<td>500</td>
<td>700</td>
<td>1000</td>
</tr>
<tr>
<td>DRAM</td>
<td>10</td>
<td>15</td>
<td>30</td>
<td>40</td>
<td>40–120</td>
<td>40–200</td>
</tr>
<tr>
<td>Maximum Power (W/Die)</td>
<td>3</td>
<td>4</td>
<td>4</td>
<td>4</td>
<td>4</td>
<td>4</td>
</tr>
<tr>
<td>High Performance</td>
<td>5</td>
<td>3.3</td>
<td>2.2</td>
<td>2.7</td>
<td>1.5</td>
<td>1.5</td>
</tr>
<tr>
<td>Portable</td>
<td>3.3</td>
<td>2.2</td>
<td>2.2</td>
<td>1.5</td>
<td>1.5</td>
<td>1.5</td>
</tr>
<tr>
<td>No. I/Os</td>
<td>500</td>
<td>750</td>
<td>1500</td>
<td>2000</td>
<td>3500</td>
<td>5000</td>
</tr>
</tbody>
</table>
Semi-log Moore's plots of the Road-map data

Rent's Rule

FIGURE 9.11 Rent's curves for various digital systems. Data points are classified according to product identification.
Rent’s rule plot of roadmap data

\[ I/O's = \alpha (gates/chip)^\beta \]

<table>
<thead>
<tr>
<th>Component</th>
<th>( \beta )</th>
<th>( K_p )</th>
</tr>
</thead>
<tbody>
<tr>
<td>SRAM</td>
<td>0.12</td>
<td>6</td>
</tr>
<tr>
<td>( \mu P )</td>
<td>0.45</td>
<td>0.82</td>
</tr>
<tr>
<td>Gate array</td>
<td>0.50</td>
<td>1.9</td>
</tr>
<tr>
<td>Computr:chip</td>
<td>0.63</td>
<td>1.4</td>
</tr>
<tr>
<td>Computr:syst</td>
<td>0.25</td>
<td>82</td>
</tr>
</tbody>
</table>
Rent’s Rule

Example I/O

<table>
<thead>
<tr>
<th>Package</th>
<th>1980</th>
<th>1990</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>64-pin DIL</td>
<td>1500-pin QFP</td>
</tr>
<tr>
<td></td>
<td>0.1in pitch</td>
<td>0.01in pitch</td>
</tr>
<tr>
<td></td>
<td>3.3x1.0in²</td>
<td>3.75x3.75in²</td>
</tr>
<tr>
<td>Pkg I/O</td>
<td>64 pins</td>
<td>Rent’s rule→</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1500 pins</td>
</tr>
<tr>
<td>Chip:</td>
<td>0.6x0.5cm²</td>
<td>1.25x1.2cm²</td>
</tr>
<tr>
<td>I/O pitch</td>
<td>344 μm</td>
<td>33 μm</td>
</tr>
</tbody>
</table>
Clock Frequency vs Time

**Figure 7.5** Microprocessor and single chip packaging evolution.

Bare and packaged chip speeds

**Figure 1.3.** Bare-chip and conventional packaging speed trends.
Power dissipation follows clock frequency

Trend to CSP
Electronics Packaging is Multi-disciplinary!

- **Electrical**
  - Architectures
  - Power distribution
  - EMI/EMC, crosstalk, ΔI & switching noise
- **Mechanical**
  - Vibrations
  - Stress
- **Thermal**
  - Conduction cooling
  - Convection cooling
- **Materials**
  - Metallurgy
  - Ceramics
  - Polymers
  - Surface science
  - Interfaces/diffusion
- **Manufacturing**
  - Instrumentation
  - Process control
  - Manufacturability/Test
Packaging Levels

Lead Pitch/Density: peripheral leads, area array, 3D

FIGURE 7.25 Summary of single chip package evolution.
PWB Density

FIGURE 16.32  PWB roadmap.
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PWB line width, pitch, & pin-count

FIGURE 16.33  The relationship between line width, pin pitch, and number of pins.
Electronics Packaging

Electronics packaging covers all technologies involved in device manufacture and design from the chip to the board. In modern devices, it is usually the package which limits system performance, and its cost can greatly exceed the cost of the silicon chip it supports. Packaging engineers are much in demand, therefore, due also to the fact that the field’s inherently multi-disciplinary nature creates a shortage of qualified people. Modern practice calls for chip/package co-design, making an understanding of packaging principles a must for all IC designers.

Lecture Objectives

- Introduce first-level interconnect technologies:
  - wire-bond & flip-chip
- Introduce standard SMT & PTH packages
  - (surface mount technology & pin through hole)
- Introduce MCM, COB, DCA, CSP, WLP, etc
  - (multi-chip modules, chip on board, direct chip attach, chip-scale package, wafer-level packaging)
- Introduce basic packaging acronyms
Packaging Technologies

- Single-chip packages (SCPs)
- Multi-chip modules (MCMs)
- Encapsulation
- Wire Bond
- [TAB (tape automated bonding)]
- Flip-Chip
- New developments

Single-Chip Packages:

- 1st level interconnects: wire-bond, TAB, FC
- 2nd level interconnects: PTH & SMT
- MCMs (multi-chip modules)
- DCA (direct chip attach)
- CSP (chip scale packages)
First-level interconnect

- Wirebond
- TAB
- Flip-chip
  (Tape-automated bonding)

Figure 1-2 Common types of first level connections. Chip to common circuit base. (Courtesy E. Larson)

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<table>
<thead>
<tr>
<th>Through-hole mount</th>
<th>Shape</th>
<th>Material</th>
<th>Lead pitch</th>
<th># of pins</th>
</tr>
</thead>
<tbody>
<tr>
<td>DIP Single-in-line package</td>
<td>Ceramic Plastic</td>
<td>2.54 mm (1000mil)</td>
<td>8 - 64</td>
<td></td>
</tr>
<tr>
<td>SIP Single-in-line package</td>
<td>Plastic</td>
<td>2.54 mm (1000mil)</td>
<td>3 - 25</td>
<td></td>
</tr>
<tr>
<td>ZIP Single-in-line package</td>
<td>Plastic</td>
<td>2.54 mm (1000mil)</td>
<td>16 - 28</td>
<td></td>
</tr>
<tr>
<td>S-DIP Single-in-line package</td>
<td>Plastic</td>
<td>3.96 mm (160mil)</td>
<td>20 - 66</td>
<td></td>
</tr>
<tr>
<td>SK-DIP Single-in-line package</td>
<td>Ceramic Plastic</td>
<td>2.54 mm (1000mil)</td>
<td>24 - 32</td>
<td></td>
</tr>
<tr>
<td>PGA Pin grid array</td>
<td>Ceramic Plastic</td>
<td>3.96 mm (160mil)</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Surface mount</th>
<th>Shape</th>
<th>Material</th>
<th>Lead pitch</th>
<th># of pins</th>
</tr>
</thead>
<tbody>
<tr>
<td>SOP Small outline package</td>
<td>Plastic</td>
<td>1.27 mm (50mil)</td>
<td>8 - 40</td>
<td></td>
</tr>
<tr>
<td>QFP Quad flat pack</td>
<td>Plastic</td>
<td>1.0 mm</td>
<td>88 - 200</td>
<td></td>
</tr>
<tr>
<td>PFP Flat package of plastic</td>
<td>Ceramic</td>
<td>1.27 mm (50mil)</td>
<td>20 - 40</td>
<td></td>
</tr>
<tr>
<td>LCC Leadless chip carrier</td>
<td>Ceramic</td>
<td>1.27 mm (50mil)</td>
<td>20 - 40</td>
<td></td>
</tr>
<tr>
<td>PLCC Plastic leaded chip carrier</td>
<td>Ceramic</td>
<td>1.27 mm (50mil)</td>
<td>18 - 124</td>
<td></td>
</tr>
<tr>
<td>VQFN Very small outline package</td>
<td>Ceramic</td>
<td>0.5mm</td>
<td>32 - 200</td>
<td></td>
</tr>
</tbody>
</table>

- PTH
- PGA
- SMT: J-lead, Gull-wing, Leadless
- COB/DCA
- flip-chip
- TAB

**FIGURE 3.10** Various types of integrated circuit packages and mounting techniques: (a) Dual-in-line package (DIP), (b) pin grid array (PGA), (c) J-lead chip carrier, (d) gull-wing chip carrier, (e) leadless chip carrier, (f) flip-chip mounting with collapsible solder balls, and (g) tape-automated bonding (TAB) applied directly on the PC board.
Figure 1: Schematic of a SLICC package.

Fig.1  Perspective view of the molded chip scale package
Second-level package attach

**FIGURE 1-6.** A multilayer circuit board showing the attachment of through-hole and surface mount packages. Surface mounting allows attachment of components to both sides of the board and a higher wiring density in the board since it permits blind vias that do not occupy the grid point throughout the entire board depth.

Substrate Vias

PCB (printed circuit board) or PWB (printed wiring board)

Multi-layer laminate

Drilled, electroplated Cu

Copper paste (ALIVH), silver loaded (ECA) epoxies, etc
- Flip-chip (C4) BGA (C5) MCM-C
**Figure 13.61** Cost comparison between various multichip packages [13.7].

**Figure 2.11** Microprocessor performance trends.
Encapsulation: “Glob-top”


COB/DCA encapsulation

Figure 6-40. TAB Encapsulation. A single-orifice nozzle dispenses encapsulant on the bonded chip.

Syringe dispense
Encapsulation: Cavity-fill

Encapsulation: Transfer molding

FIGURE 16.12 A typical transfer molding process.
Encapsulation: Underfill

Figure 1: DCA General Process Flow

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Figure 15.16: Underfill dispensing parameters and optimization

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Wire-bonding

- Dual-in-line (DIL) plastic package (DIP)

**Figure 1-12.** Cutaway view of a postmolded plastic package in the configuration of a dual-line package (DIP).

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**Figure 5.1** Geometric parameters of a typical wirebonded structure
Figure 2-7b  State of the art wire bonding (1.25 mil Al wire, 465 I/O, 4.8 mil pitch).
Figures 11-12. Ultrasonic wedge bonding: (a) ultrasonic wedge bonding tool with typical dimensions; (b) ultrasonic wedge bonding process.
Figure 8-16. Idealized Wirebond Configuration. A transverse load is applied to the wirebond. The top figure illustrates the vertical projection of the wire and the melt front approaching at a mean velocity $u_x$.

Wire sweep

Figure 8-18. Horizontal Displacement of a Wirebond at Different Flow Regimes. Deflection ($h_y$) illustrated for increasing higher flow Reynolds numbers to show the ultimate collapse of the wire. For a package with a pad spacing of 0.254 mm, wire sweep occurs at $Re = 0.0156$. This critical value is governed by the wire properties, the flow characteristics, and the package configuration.
**Wafer bumping**

1. Ox (CVD), 1 to 1.5 μm
2. Aluminum, 1 μm
3. SiO (thermally grown)
4. Wafer as received is cleaned and sputter-etched
5. Au, 100 nm
6. Contact/barrier layer(s), 100 nm each
7. Sputter deposit contact/barrier layers and protect with layer of sputtered Au
8. Laminate photoresist
9. Laminate with photo resist (25 μm thick) and develop

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**Figure 7.9 Wafer bumping process flow**

- Solder bumps
- As printed →
- Re-flowed →
WLP & Redistribution

**Figure 7.16** Cross section of plastic flip chip BGA package (all dimensions are in micrometers)

**Figure 10.11** Typical redistribution technology. (Courtesy of IZM Berlin)
FIGURE 3.16 Insulated metal substrate

Figure 1.11 NEC's 3-D stack-up chip scale package (CSP) for memory devices.
Lecture Summary

- Standard packages
- Encapsulation
- First level interconnect (chip to package):
  - Wire-bond, TAB, flip-chip (C4)
- Second-level interconnect (package to board):
  - PTH, SMT, PGA, BGA (C4/C5), etc
- MCMs, CSPs, WLP, etc