# Electronics Packaging
## TKK 2009 Lecture 1

**James E. Morris**
**Dept of Electrical & Computer Engineering**
**Portland State University**

Portland State UNIVERSITY

Nanoelectronics & Packaging Lab

## Electronics Packaging

| Tuesday Lecture | Friday Lecture |
|---|---|
| April 7: Introduction | |
| | April 17: Electrical Package Design |
| April 21: Package Reliability | April 24: Electrically Conductive Adhesives I |
| April 28: Electrically Conductive Adhesives II | |

**Download course notes from: http://www.ece.pdx.edu/~jmorris/TKK/UG**

**e-mail: jmorris@cecs.pdx.edu**

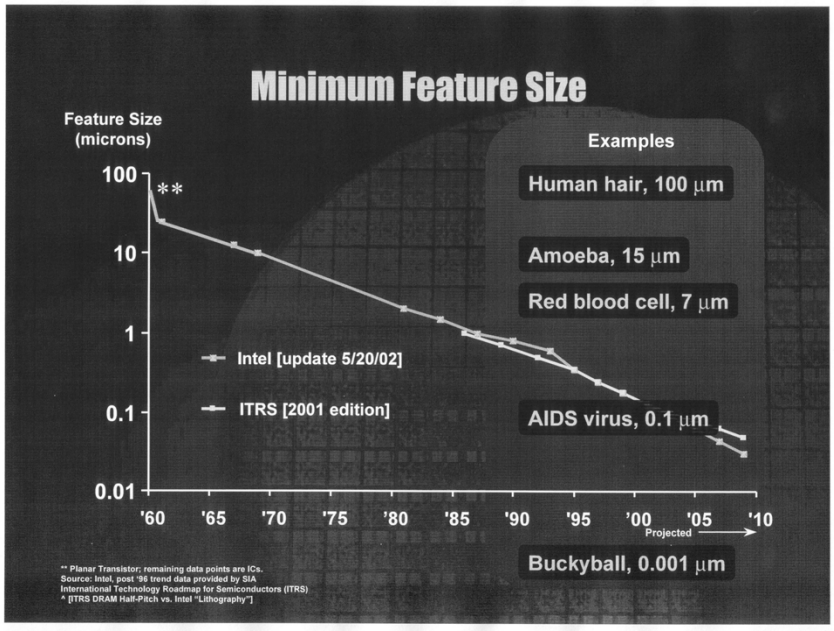
## References


- R. Ulrich & W.D.Brown (editors) "Advanced Electronic Packaging, 2nd edition" Wiley/IEEE Press (2005)
- Tummala (editor) "Fundamentals of Microsystems Packaging" McGraw-Hill (2001)
- Pecht et al "Integrated Circuit, Hybrid, & MCM Packaging Design Guidelines" Wiley (1994)
- J.E. Morris (editor) "Electronics Packaging Forum: Vols 1 & 2" VNR (1990)
- J.E. Morris (editor) "Electronics Packaging Forum: MCM Issues" IEEE Press (1994)
- Johan Liu (editor) "Conductive Adhesives for Electronics Packaging" Electrochemical (1999)




## Lecture 1 **Introduction**

- The package roadblock to system performance
- What is packaging?
- Packaging technologies

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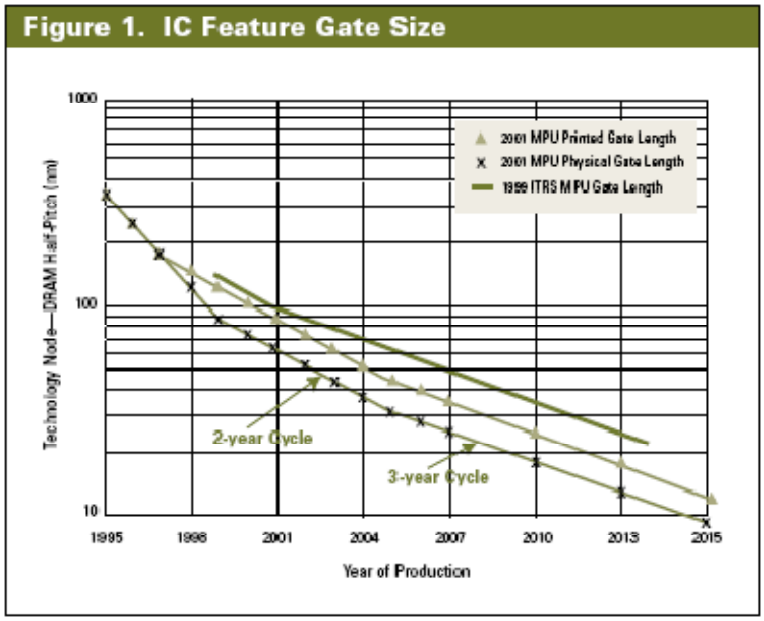
Borsuk & Coffey, Defense Horizons

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## Why is Packaging Important?

- **Elementary example:**

| Semiconductor Chip Parameters | 1980 | 1990 |
|---|---|---|
| **Feature size** | **4 μm** | **1 μm** |
| **Chip area** | **0.3 $cm^2$** | **1.5 $cm^2$** |
| **Gates/chip** | **5,000** | **100,000** |
| **μP clock freq** | **6 MHz** | **40 MHz** |
| **Power** | **2 W** | **10 W** |
| **I/O count** | **64** | **1500** |



## Chip density, power, speed

| | 1980 | | 1990 | |
|---|---|---|---|---|
| Ckt size | $L^2$ | $4\mu \rightarrow 1\mu$ | $L^2/16$ | |
| Chip size | $0.3cm^2$ | 5xArea→ | $1.5cm^2$ | |
| Ckts/chip | N | → | 5x16N=80N | (20N) |
| Pwr $diss^n$ | 2w | I÷4→ | 80x2w/4=40w | (10w) |
| Clk freq | 6MHz | C/16, I/4 | 24MHz | (40MHz) |

# ITRS product categories

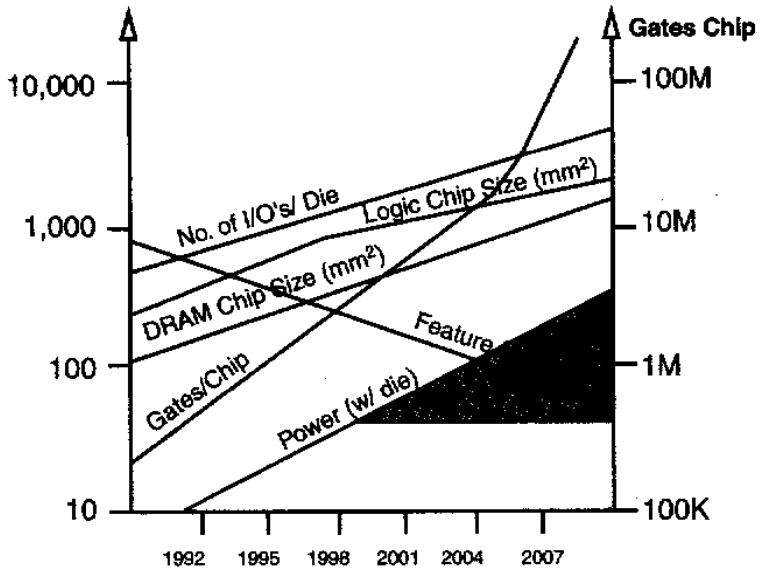
| Product category | Product description |
|---|---|
| Low cost | <$ 300: consumer products, microcontrollers, disk drivers |
| Hand-held | <$ 1000: battery powered products e.g. mobile and cellular products |
| Cost/performance | <$3000: notebooks, desktop personal computers |
| High performance | >$3000:high-end work stations, servers, avionics, supercomputer |
| Harsh environment | Under-the-hood and other hostile environment products |
| Memory | DRAM's, SRAM's |



# ITRS Packaging requirements

| | 1992 | 1995 | 1998 | 2001 | 2004 | 2007 |
|---|---|---|---|---|---|---|
| Feature Size ($\mu m$) | 0.5 | 0.35 | 0.25 | 0.18 | 0.12 | 0.07 |
| Gates/chip | 300K | 800K | 2M | 5M | 10M | 100M |
| Transistors ($cm^{-2}$) | 0.01B | 0.04B | 0.1B | 0.22B | 0.6B | 2.1B |
| Chip Size ($mm^2$) | | | | | | |
| Logic/Uniprocessor | 250 | 400 | 600 | 800 | 1000 | 1250 |
| DRAM | 132 | 200 | 320 | 500 | 700 | 1000 |
| Maximum Power (W/Die) | | | | | | |
| High Performance | 10 | 15 | 30 | 40 | 40–120 | 40–200 |
| Portable | 3 | 4 | 4 | 4 | 4 | 4 |
| Power Supply Voltage (V) | | | | | | |
| Desktop | 5 | 3.3 | 2.2 | 2.2 | 1.5 | 1.5 |
| Portable | 3.3 | 2.2 | 2.2 | 1.5 | 1.5 | 1.5 |
| No. I/Os | 500 | 750 | 1500 | 2000 | 3500 | 5000 |

## Semi-log Moore's plots of the Road-map data




2009

## Rent's Rule

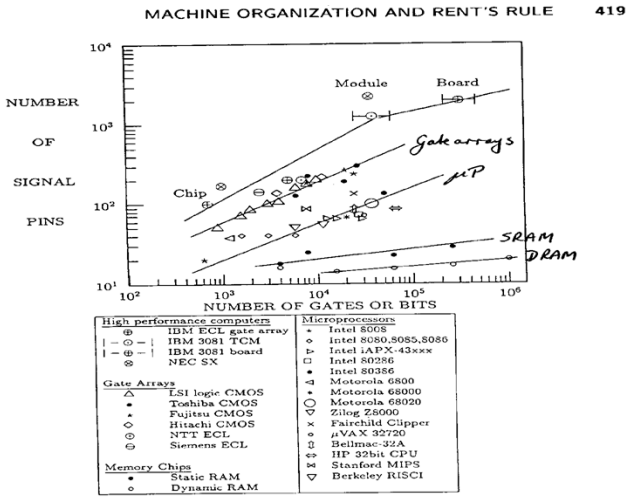
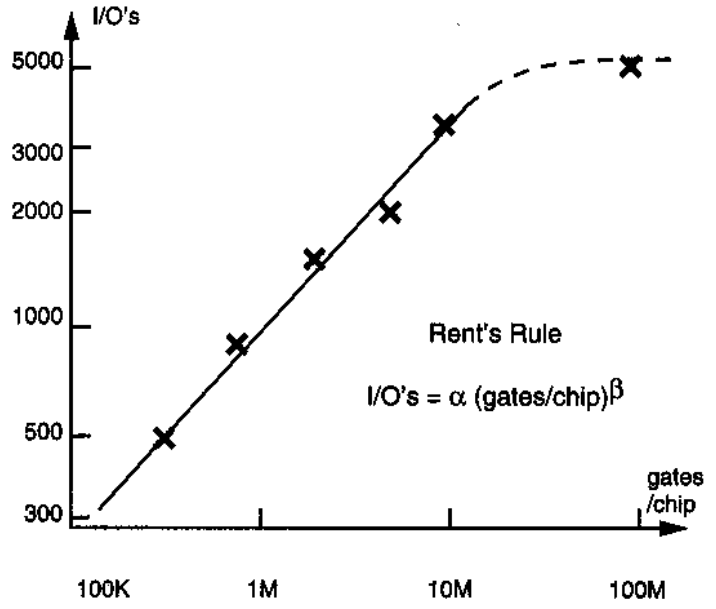



**FIGURE 9.11** Rent's curves for various digital systems. Data points are classified according to product identification.

## Rent's rule plot of roadmap data

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## Pkg pins ≈ $K_p$(bits or gates)$^{\beta}$

| | $\beta$ | $K_p$ |
|---|---|---|
| SRAM | 0.12 | 6 |
| μP | 0.45 | 0.82 |
| Gate array | 0.50 | 1.9 |
| Computr:chip | 0.63 | 1.4 |
| Computr:syst | 0.25 | 82 |

# Rent's Rule

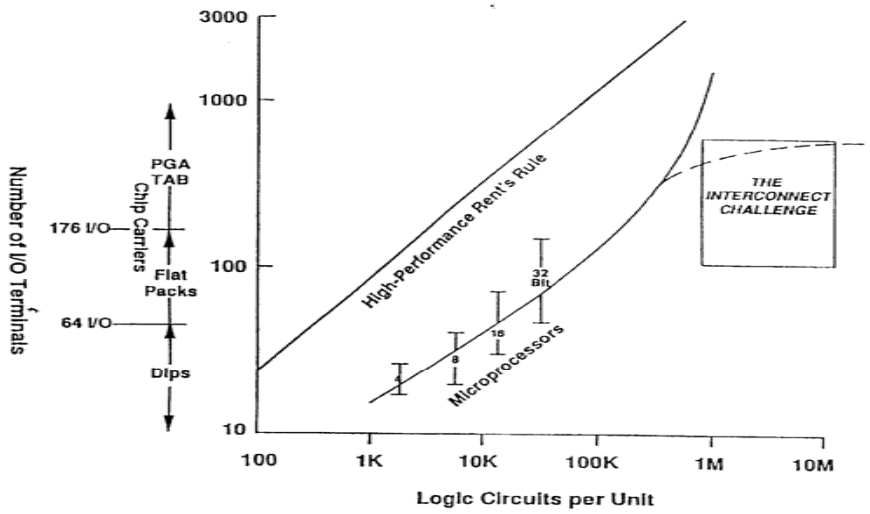



**Figure 1.4.** High-performance Rent's Rule.[4]



# Example I/O

| Package | 1980 | | 1990 |
|---|---|---|---|
| | 64-pin DIL | | 1500-pin QFP |
| | 0.1in pitch | | 0.01in pitch |
| | $3.3 \times 1.0 in^2$ | | $3.75 \times 3.75 in^2$ |
| Pkg I/O | 64 pins | Rent's rule→ | 1500 pins |
| Chip: | $0.6 \times 0.5 cm^2$ | | $1.25 \times 1.2 cm^2$ |
| I/O pitch | 344 μm | | 33 μm |

# Clock Frequency vs Time

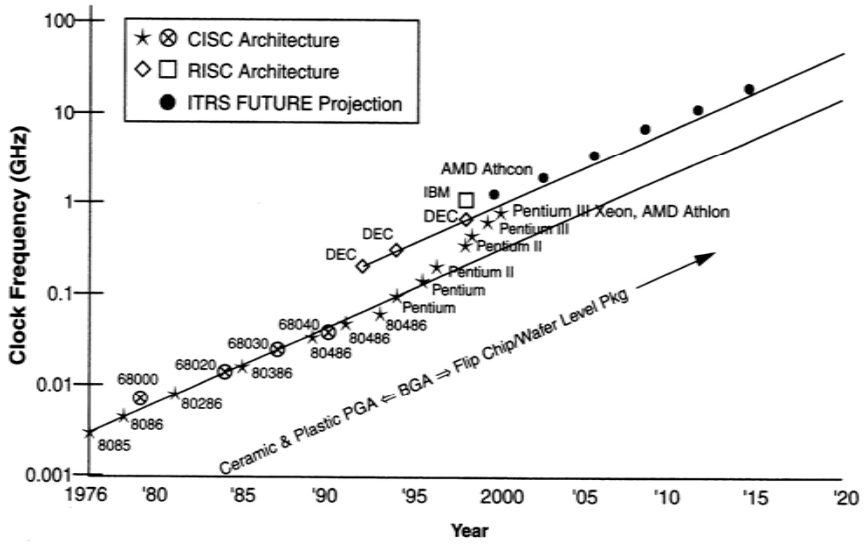



**FIGURE 7.5** Microprocessor and single chip packaging evolution.



# Bare and packaged chip speeds

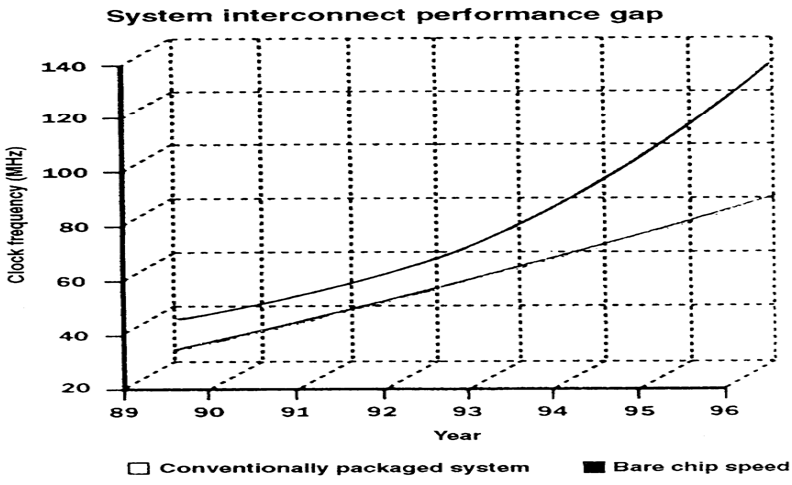



**Figure 1.3.** Bare-chip and conventional packaging speed trends.[2]

# Power dissipation follows clock frequency

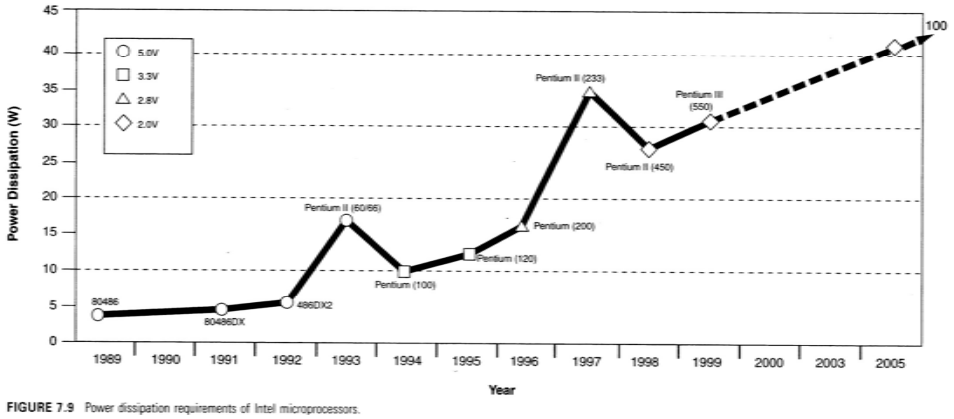



FIGURE 7.9 Power dissipation requirements of Intel microprocessors.



# Trend to CSP

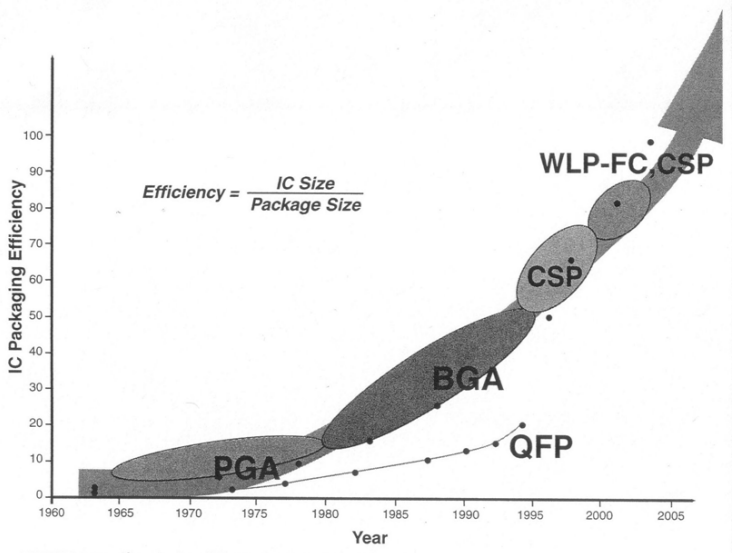



FIGURE 7.22 IC packaging efficiency of various single chip packages.

## Package functions

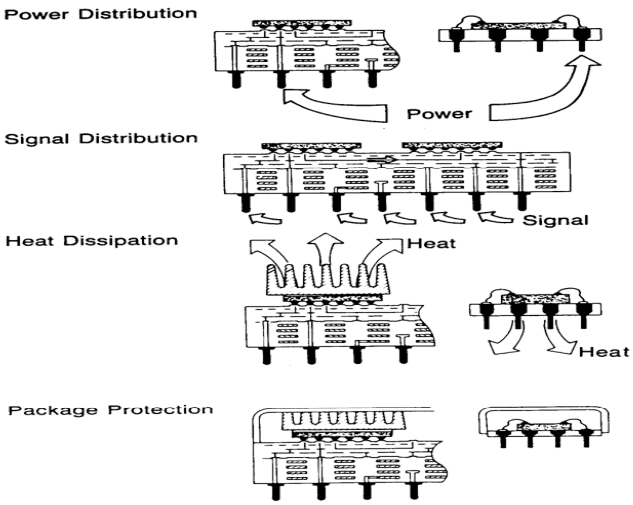


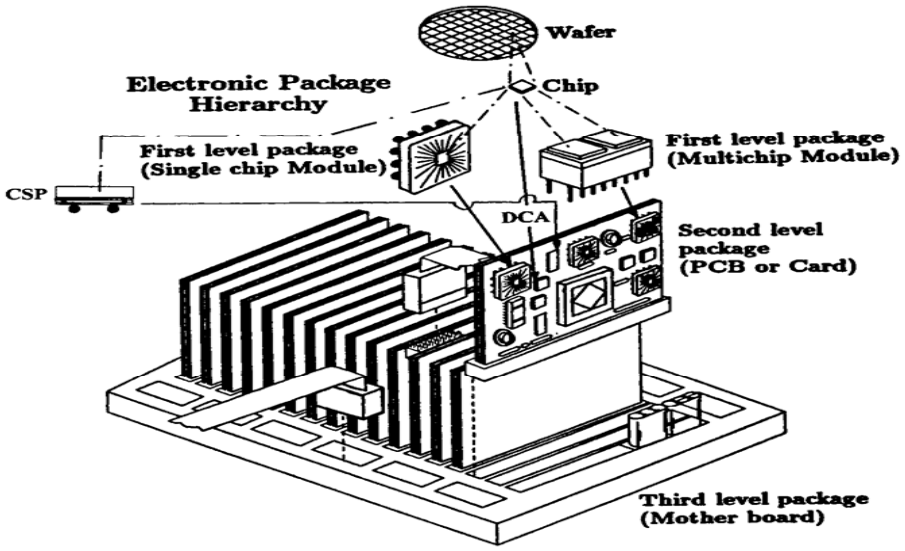

**Figure 1-1. Four Major Functions of the Package.** + Mechanical support.



## Electronics Packaging is Multi-disciplinary!

- Electrical
  - Architectures
  - Power distribution
  - EMI/EMC, crosstalk, $\Delta I$ & switching noise
- Mechanical
  - Vibrations
  - Stress
- Thermal
  - Conduction cooling
  - Convection cooling
- Materials
  - Metallurgy
  - Ceramics
  - Polymers
  - Surface science
  - Interfaces/diffusion
- Manufacturing
  - Instrumentation
  - Process control
  - Manufacturability/ Test

# Packaging Levels






# Lead Pitch/Density: peripheral leads, area array, 3D

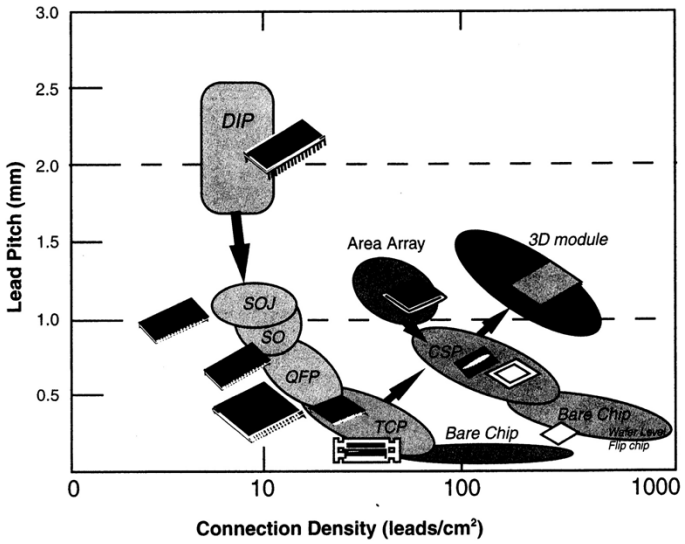



FIGURE 7.25 Summary of single chip package evolution.

# PWB Density

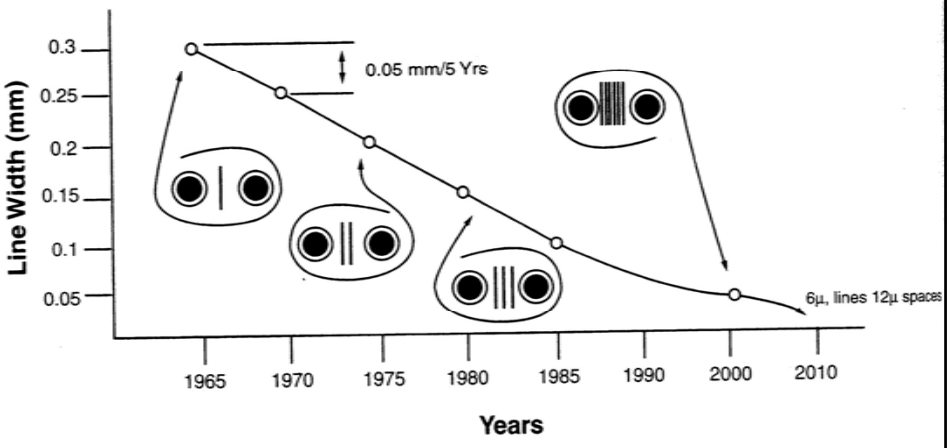



**FIGURE 16.32** PWB roadmap.



# PWB line width, pitch, & pin-count

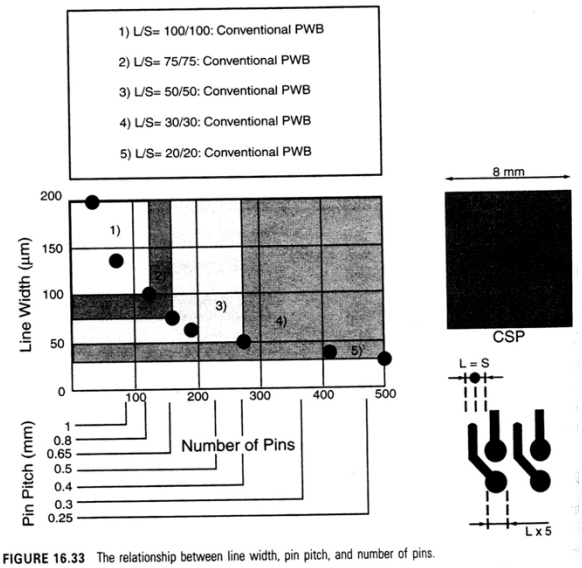



**FIGURE 16.33** The relationship between line width, pin pitch, and number of pins.

## Electronics Packaging

Electronics packaging covers all technologies involved in device manufacture and design from the chip to the board. In modern devices, it is usually the package which limits system performance, and its cost can greatly exceed the cost of the silicon chip it supports. Packaging engineers are much in demand, therefore, due also to the fact that the field's inherently multi-disciplinary nature creates a shortage of qualified people. Modern practice calls for chip/package co-design, making an understanding of packaging principles a must for all IC designers.



## Lecture Objectives

- Introduce first-level interconnect technologies:
  - wire-bond & flip-chip
- Introduce standard SMT & PTH packages
  - (surface mount technology & pin through hole)
- Introduce MCM, COB, DCA, CSP, WLP, etc
  - (multi-chip modules, chip on board, direct chip attach, chip-scale package, wafer-level packaging)
- Introduce basic packaging acronyms

## Packaging Technologies

- Single-chip packages (SCPs)
- Multi-chip modules (MCMs)
- Encapsulation
- Wire Bond
- [TAB (tape automated bonding)]
- Flip-Chip
- New developments



## Single-Chip Packages:

- 1st level interconnects: wire-bond, TAB, FC
- 2nd level interconnects: PTH & SMT
- MCMs (multi-chip modules)
- DCA (direct chip attach)
- CSP (chip scale packages)

# First-level interconnect

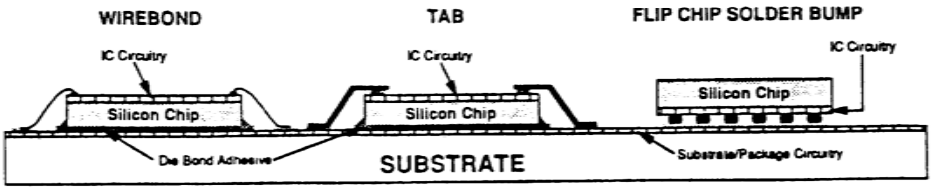



**Figure 1-2** Common types of first level connections. Chip to common circuit base. (Courtesy E. Larson).

- Wirebond TAB Flip-chip
  - (Tape-automated bonding)



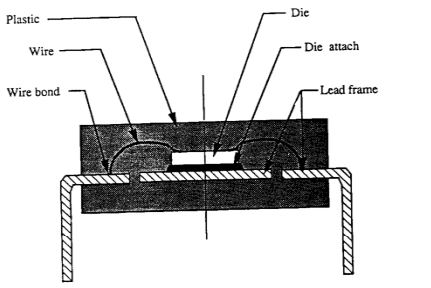



**Figure 1.1** *Cross-section of a typical plastic-encapsulated single-chip packag*

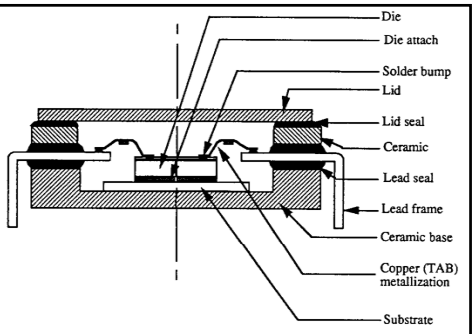



**Figure 1.2** *Cross-section of a typical ceramic single-chip package*

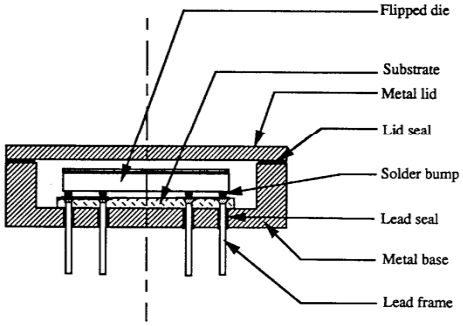



**Figure 1.3** *Cross-section of a typical metal single-chip package*

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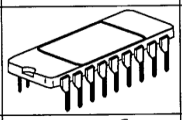
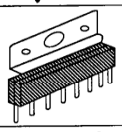
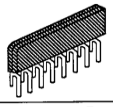
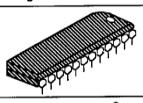
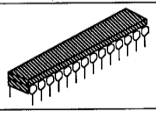
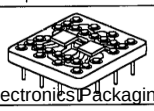
| Through hole mount | Shape | Typical features: Material | Lead pitch | # of I/O pins |
|---|---|---|---|---|
| **DIP** Dual in-line package |  | Ceramic, Plastic | • 2.54 mm (100mil) | 8 - 64 |
| **SIP** Single in-line package |  | Plastic | • 2.54 mm (100mil)<br>• 1 direction lead | 3 - 25 |
| **ZIP** Zigzag in-line package |  | Plastic | • 2.54 mm (100mil)<br>• 1 direction lead | 16 - 24 |
| **S-DIP** Shrink dual in-line package |  | Plastic | • 1.778 mm (70mil) | 20 - 64 |
| **SK-DIP** Skinny dual in-line package |  | Ceramic, Plastic | • 2.54 mm<br>• half- size pitch in the width direction | 24 - 32 |
| **PGA** Pin grid array |  | Ceramic, Plastic | • 2.54 mm (100mil) | |

**Figure 3.6** *Through-hole mount-package profiles*

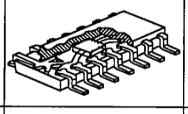
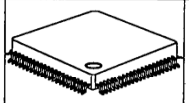
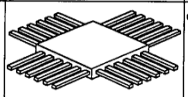
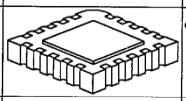
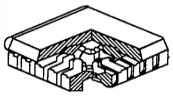
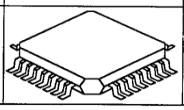
| Surface mount | Shape | Typical features: Material | Lead pitch | # of I/O pins |
|---|---|---|---|---|
| **SOP** Small outline package |  | Plastic | • 1.27mm (50mil)<br>• 2 direction lead | 8 - 40 |
| **QFP** Quad flat-pack |  | Plastic | • 1.0 mm<br>• 0.8 mm<br>• 0.65 mm<br>• 4 direction lead | 88 - 200 |
| **FPG** Flat package of glass |  | Ceramic | • 1.27 mm (50mil)<br>• 0.762mm (30mil)<br>• 2 direction lead<br>• 4 direction lead | 20 - 80 |
| **LCC** Leadless chip carrier |  | Ceramic | • 1.27mm (50mil)<br>• 1.016mm (40mil)<br>• 0.762mm (30mil) | 20 - 40 |
| **PLCC** Plastic leaded chip carrier |  | Ceramic | • 1.27mm (50mil)<br>• j-shaped bend<br>• 4 direction lead | 18 - 124 |
| **VSQF** Very small quad flatpack |  | Ceramic | • 0.5mm | 32 - 200 |

**Figure 3.7** *Surface-mount package profiles*



- PTH
- PGA
- SMT:
  - J-lead
  - Gull-wing
  - Leadless
- COB/DCA
  - flip-chip
  - TAB

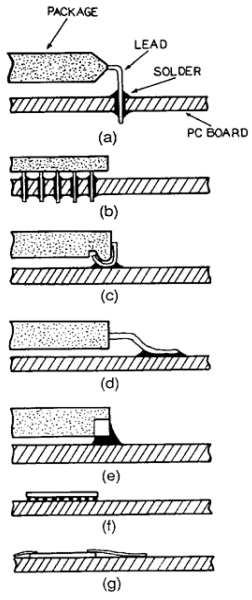



**FIGURE 3.10** Various types of integrated circuit packages and mounting techniques: (a) Dual-in-line package (DIP), (b) pin grid array (PGA), (c) J-leaded chip carrier, (d) gull-wing-leaded chip carrier, (e) leadless chip carrier, (f) flip-chip mounting with collapsible solder balls, and (g) tape-automated bonding (TAB) applied directly on the PC board

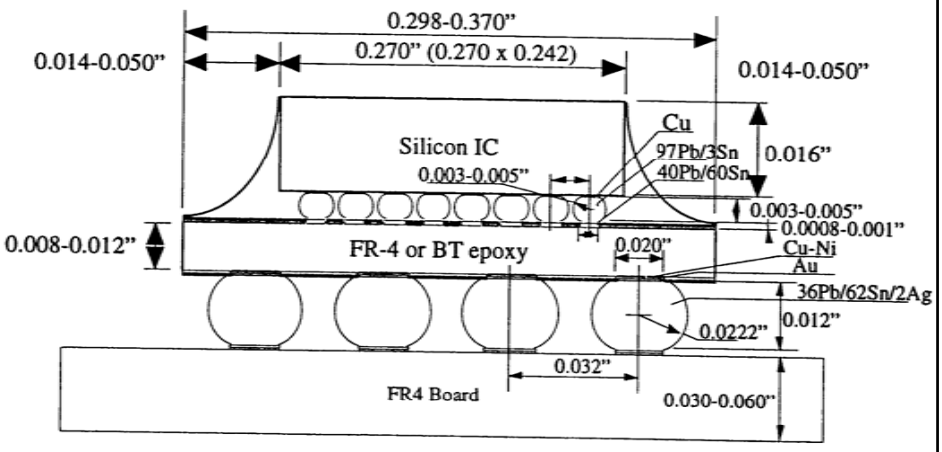



Figure 1: Schematic of a SLICC package.



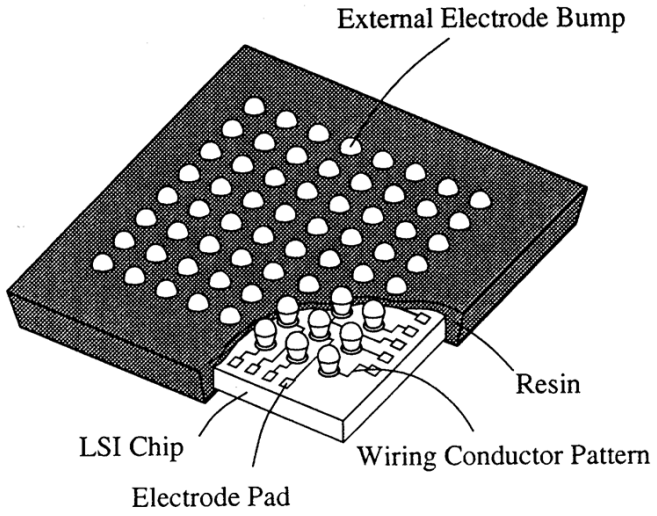



Fig.1 Perspective view of the molded chip scale package

## Second-level package attach

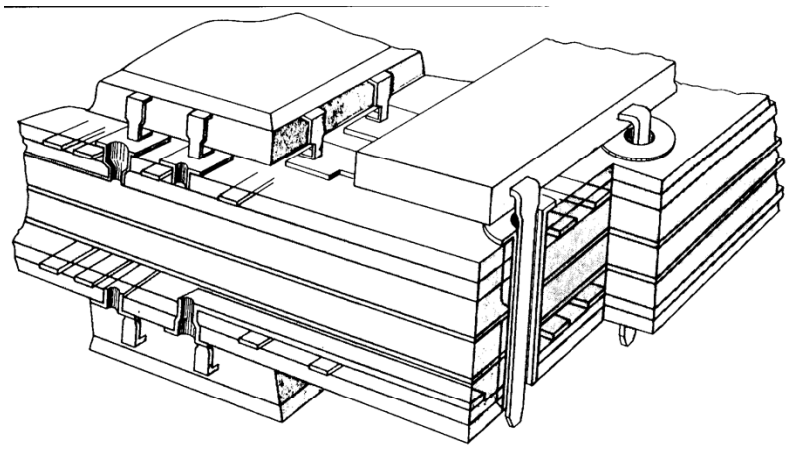
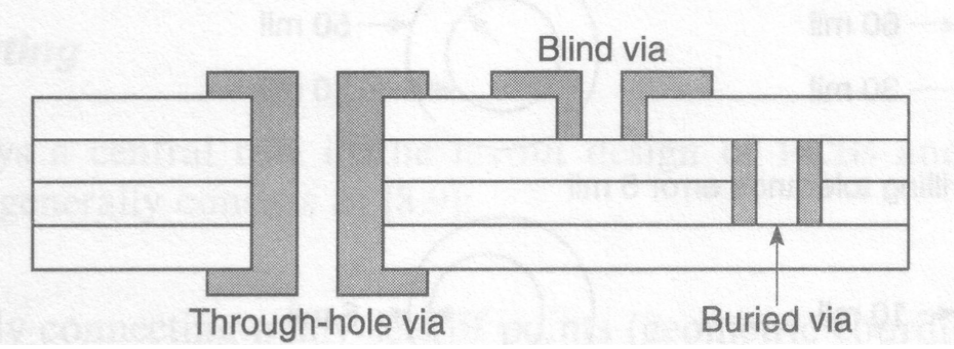


**FIGURE 1-6.** A multilayer circuit board showing the attachment of through-hole and surface mount packages. Surface mounting allows attachment of components to both sides of the board and a higher wiring density in the board since it permits blind vias that do not occupy the grid point throughout the entire board depth.

- SMT & PTH



## Substrate Vias




**PCB (printed circuit board) or PWB (printed wiring board)**

**Multi-layer laminate**

**Drilled, electroplated Cu**

**Copper paste (ALIVH), silver loaded (ECA) epoxies, etc**

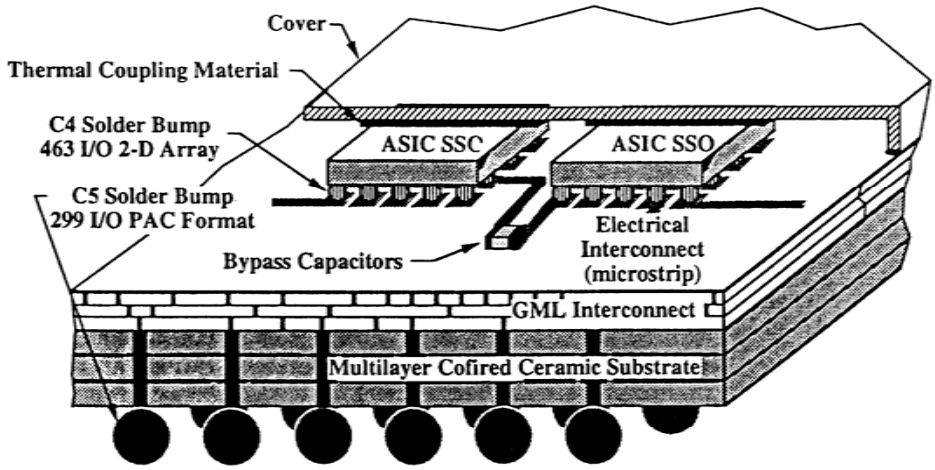



**Figure 2-14a** Schematic of workstation module.

- Flip-chip (C4) BGA (C5) MCM-C



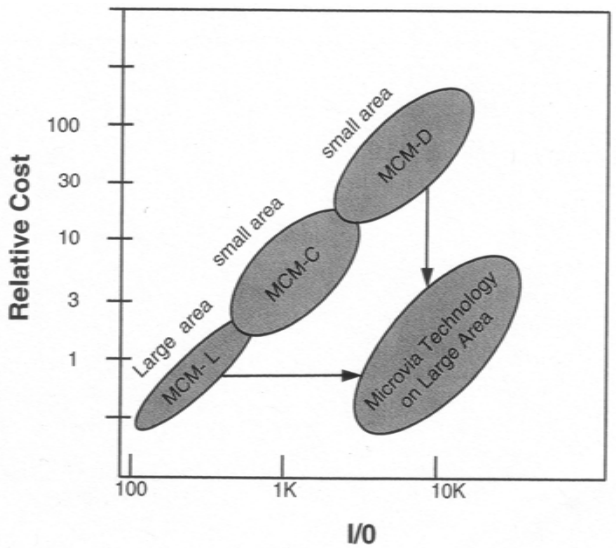



**FIGURE 8.25** MCM relative cost versus module I/O for the various MCM technologies.

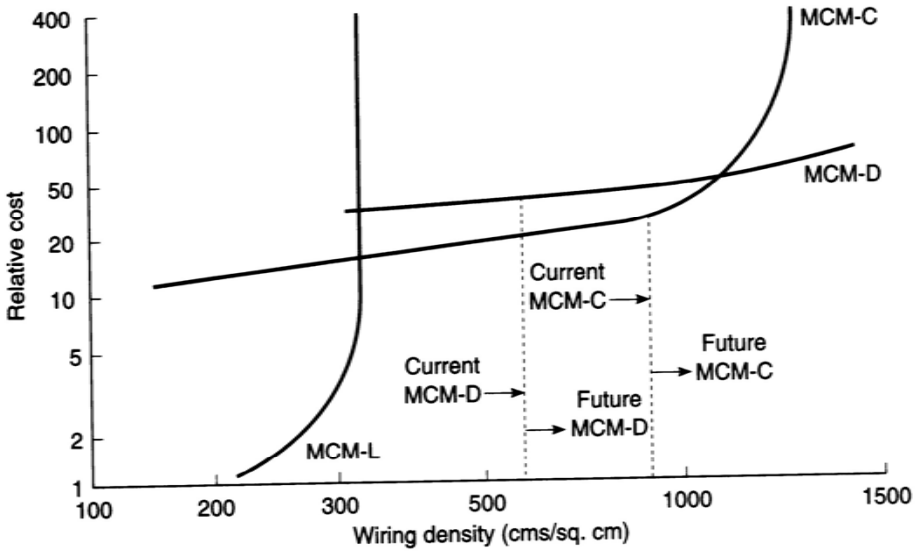



**Figure 13.61** Cost comparison between various multichip packages [13.7].



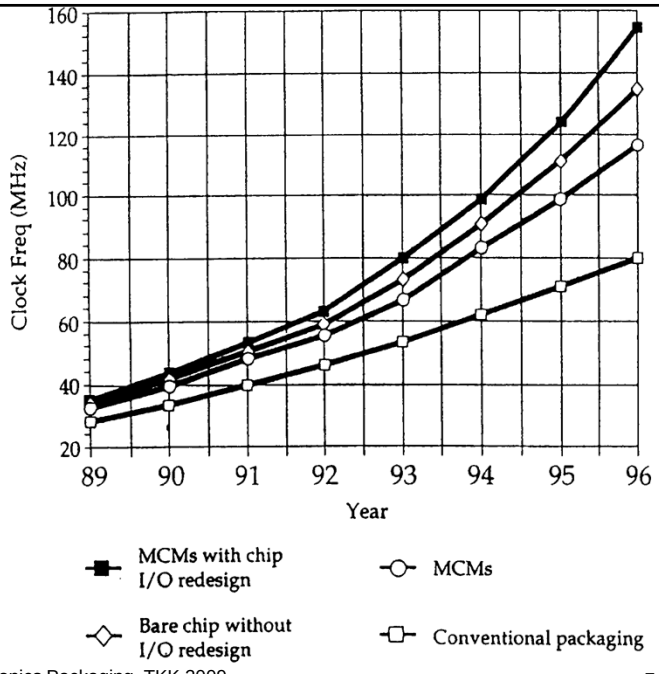



**Figure 2.1.** Microprocessor performance trends.[2]

# Encapsulation: "Glob-top"

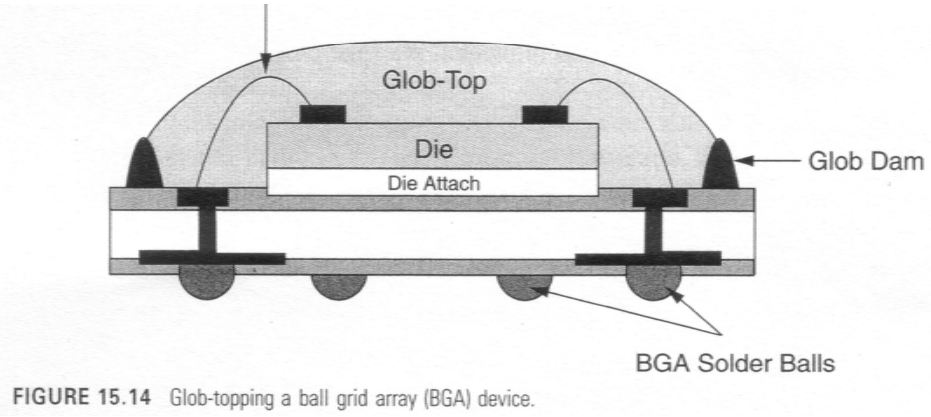
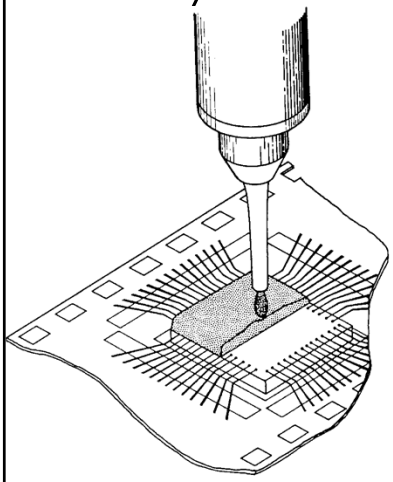



FIGURE 15.14 Glob-topping a ball grid array (BGA) device.



# COB/DCA encapsulation



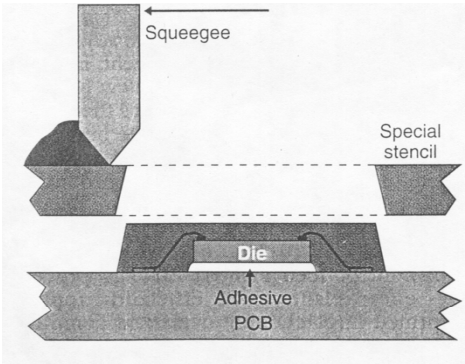
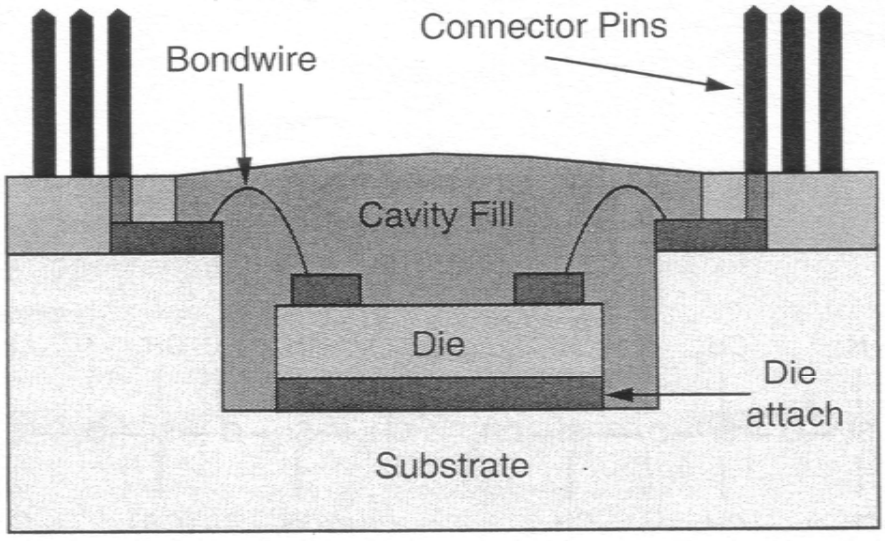



**Figure 6-40. TAB Encapsulation.** A single-orifice nozzle dispenses encapsulant on the bonded chip.

- Syringe dispense

## Encapsulation: Cavity-fill






## Encapsulation: Transfer molding

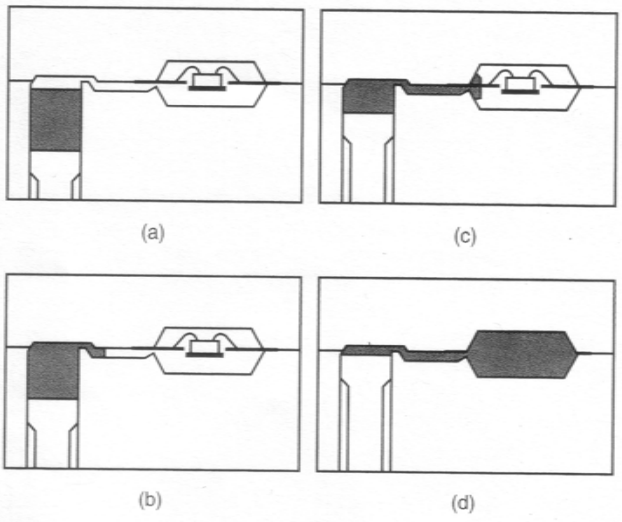
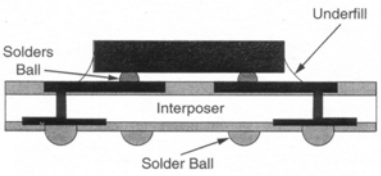



**FIGURE 15.13** A typical transfer molding process.

# Encapsulation: Underfill



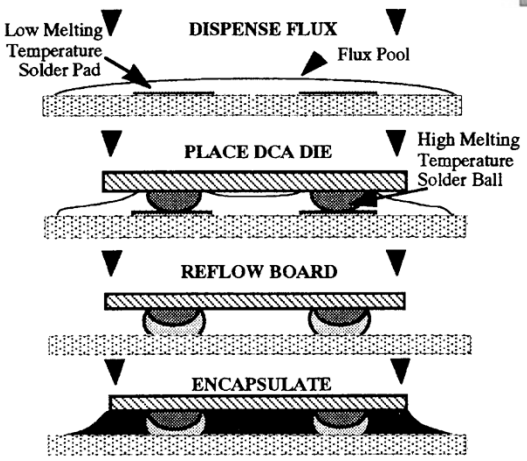




**Figure 1: DCA General Process Flow**



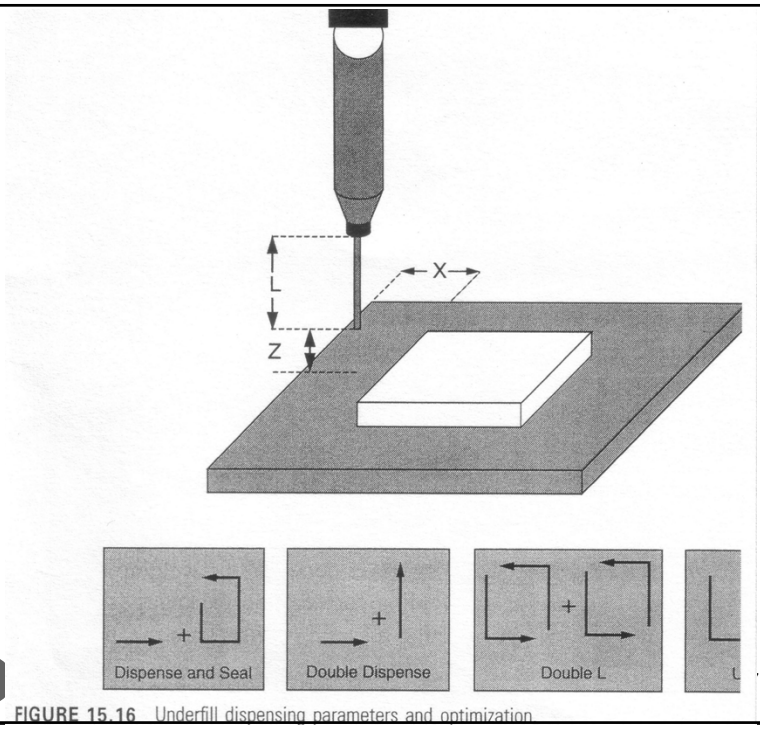



FIGURE 15.16 Underfill dispensing parameters and optimization

# Wire-bonding

- Dual-in-line (DIL) plastic package (DIP)

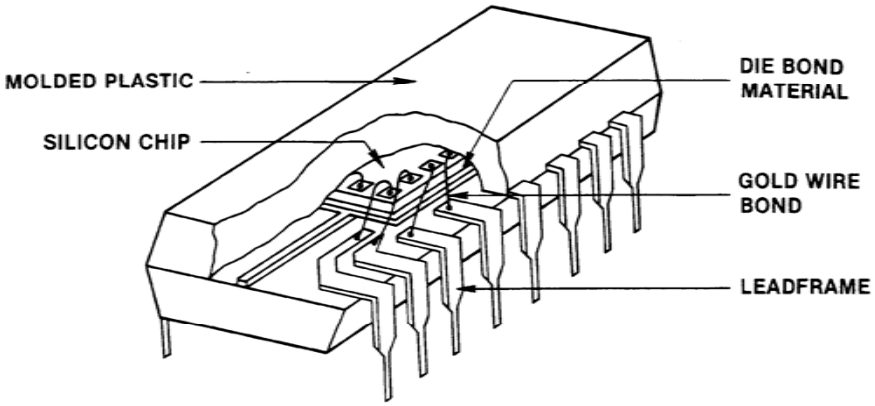



**FIGURE 1-12.** Cutaway view of a postmolded plastic package in the configuration of a dual-line package (DIP).



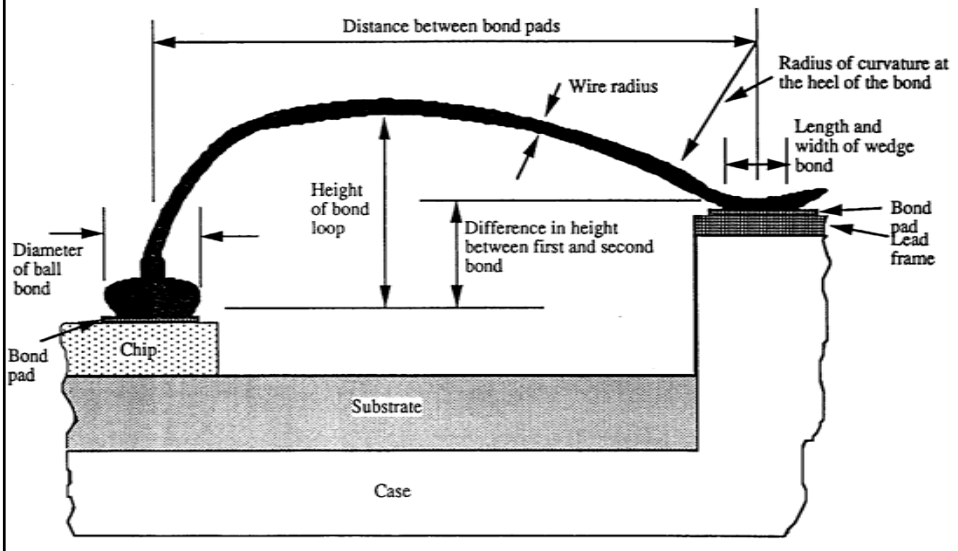



**Figure 5.1** *Geometric parameters of a typical wirebonded structure*

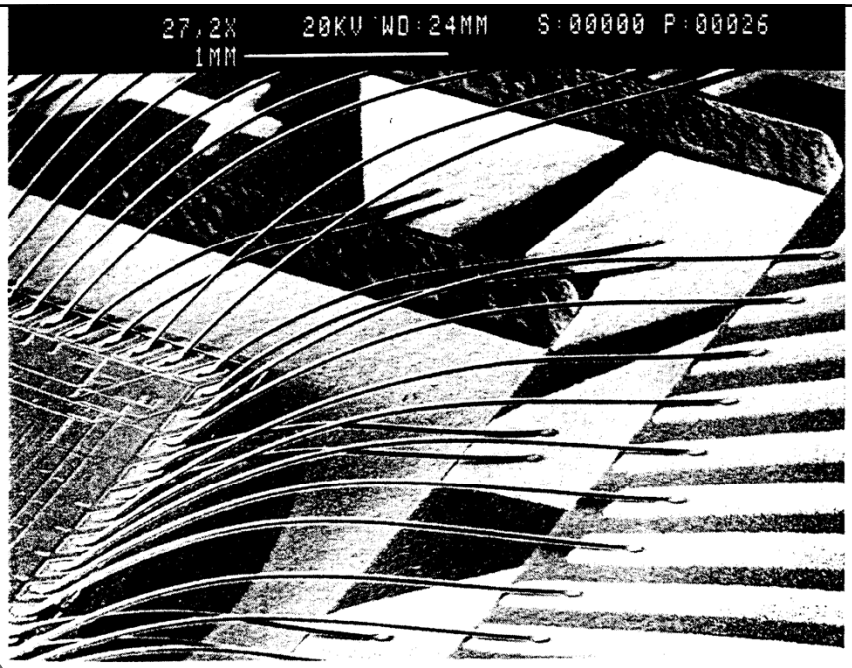
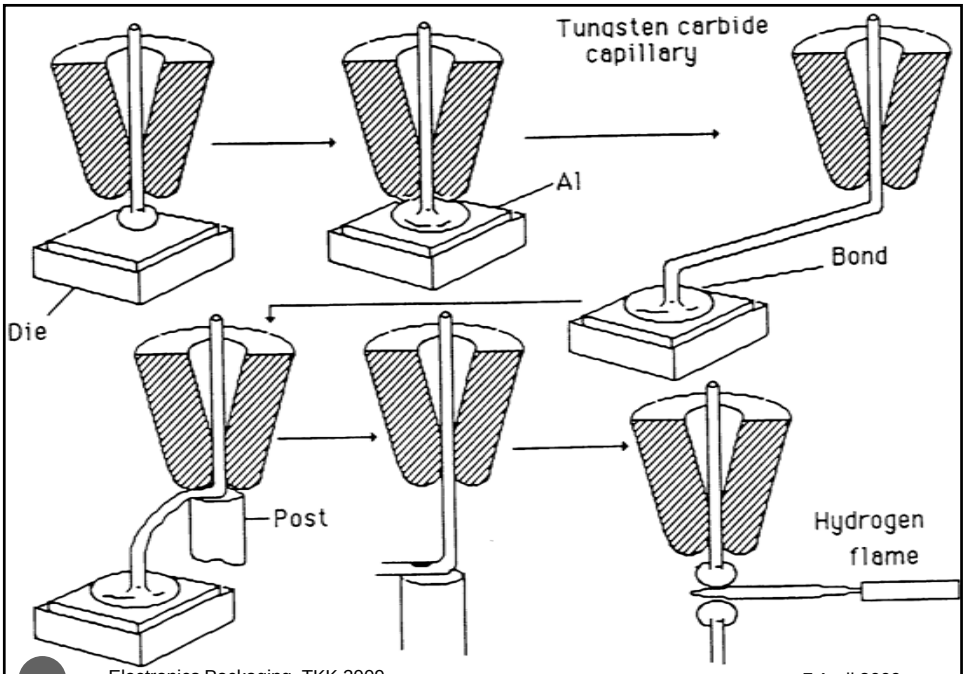
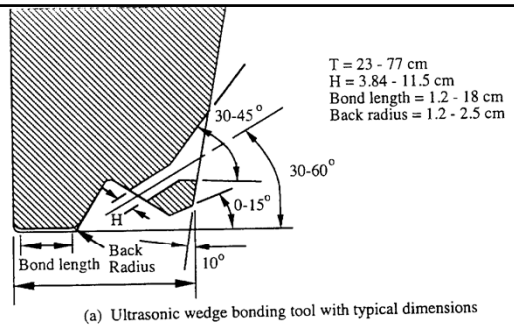


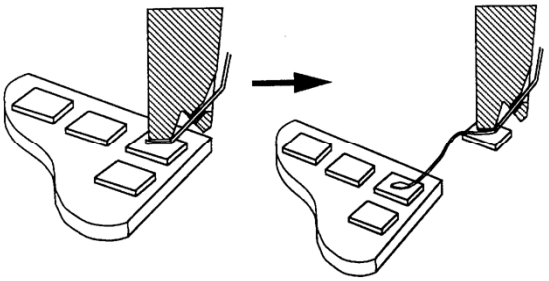



**Figure 2-7b** State of the art wire bonding (1.25 mil Al wire, 465 I/O, 4.8 mil pitch).






(a) Ultrasonic wedge bonding tool with typical dimensions

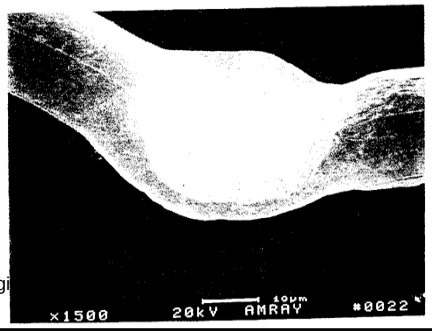


(b) Ultrasonic wedge bonding process

**Figure 3.4** *Ultrasonic wedge bonding: (a) ultrasonic wedge bonding tool with typical dimensions; (b) ultrasonic wedge bonding process*




(a)



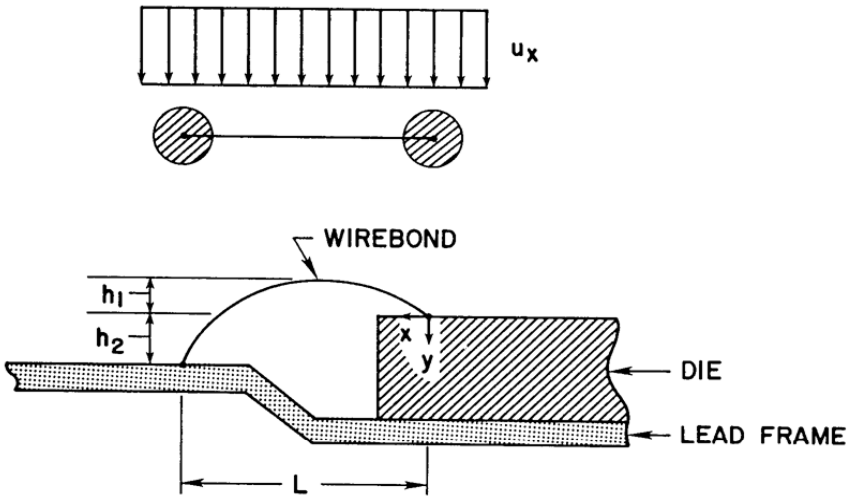



**Figure 8-16. Idealized Wirebond Configuration.** A transverse load is applied to the wirebond. The top figure illustrates the vertical projection of the wire and the melt front approaching at a mean velocity $u_x$.



## Wire sweep

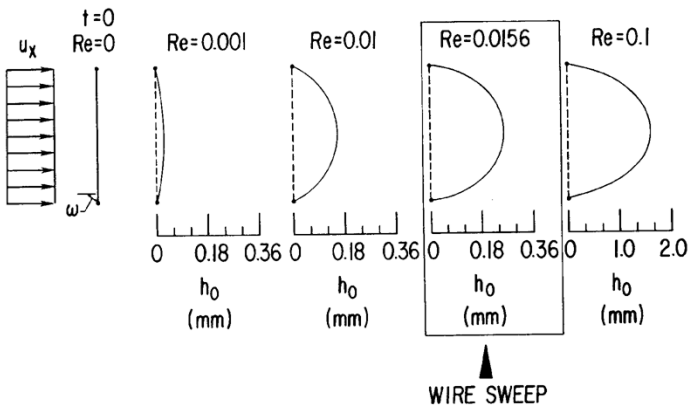



**Figure 8-18. Horizontal Displacement of a Wirebond at Different Flow Regimes.** Deflection ($H_0$) illustrated for increasing higher flow Reynolds numbers to show the ultimate collapse of the wire. For a package with a pad spacing of 0.254 mm, wire sweep occurs at $Re = 0.0156$. This critical value is governed by the wire properties, the flow characteristics, and the package configuration.

# Wafer bumping

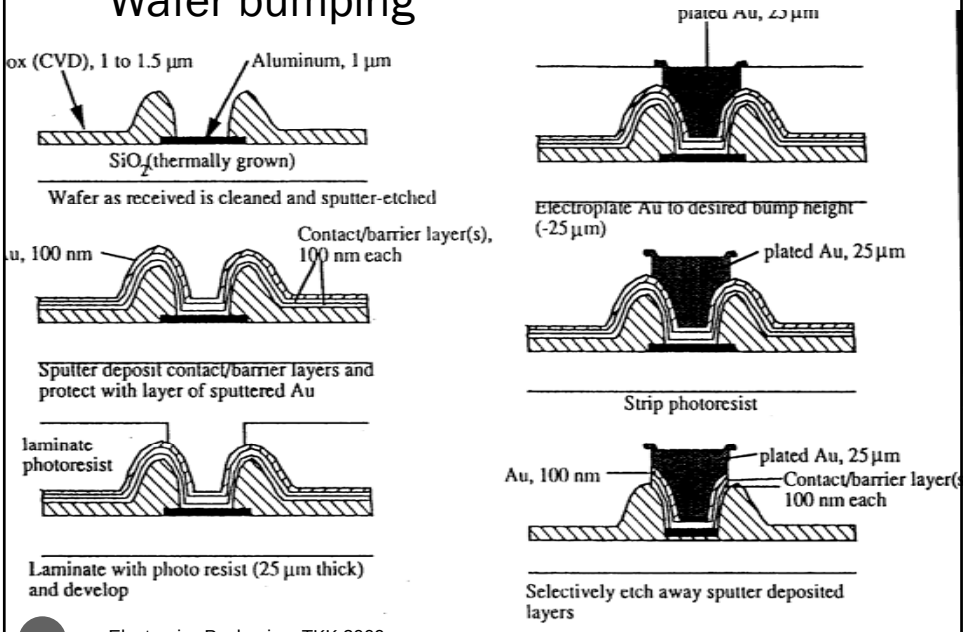
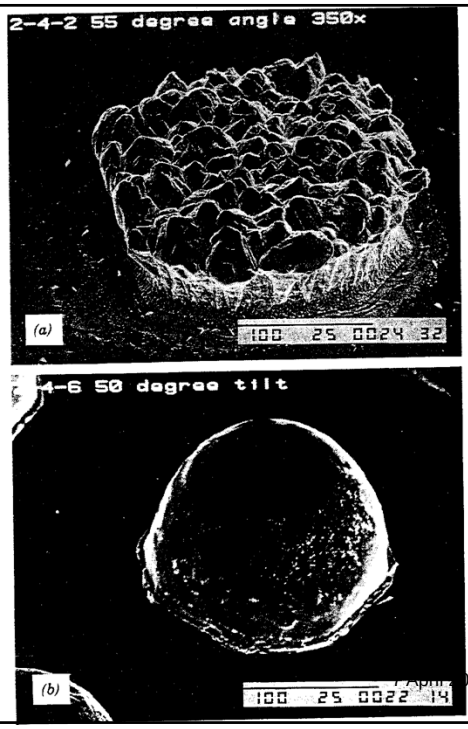





**Figure 7.9** *Wafer bumping process flow*

- Solder bumps
  - As printed →
  - Re-flowed →



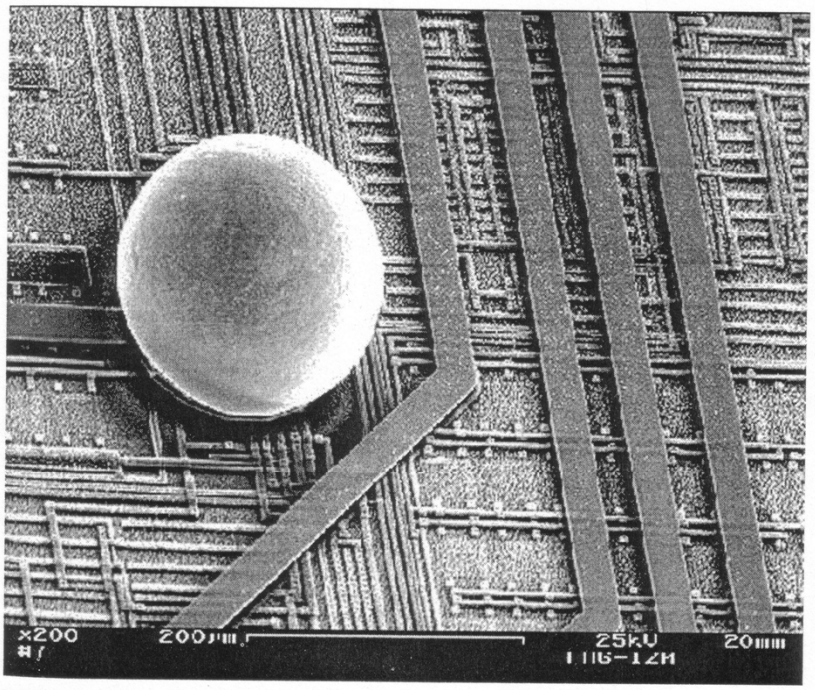



FIGURE 10.12 Comparison of typical WLP dimensions on a chip.

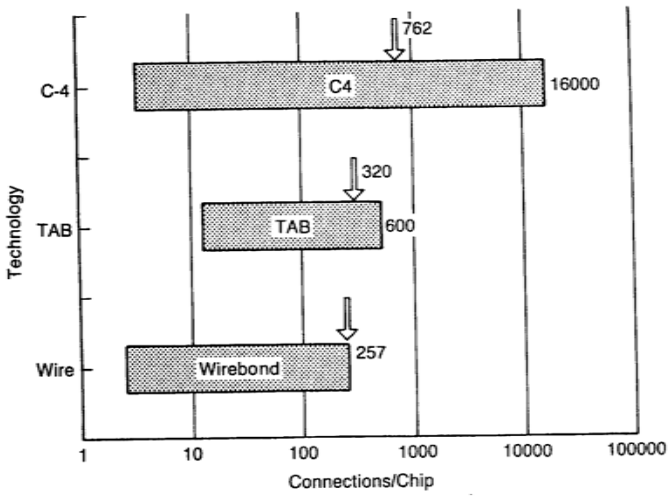



**Figure 1-16. Chip-Connection Technology.** The arrow highlights product-usage in 1987. After Koopman, Ref. [11], 1988.

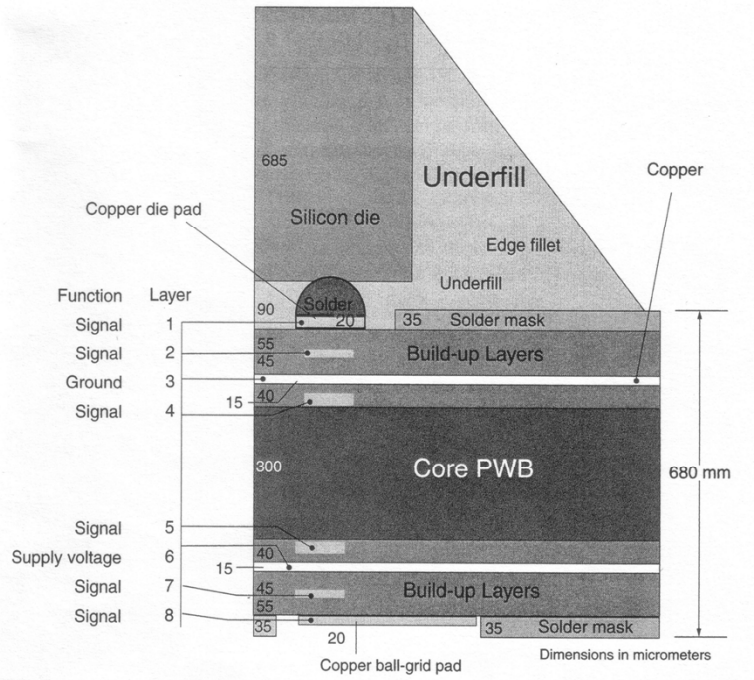



FIGURE 7.16 Cross section of plastic flip chip BGA package (all dimensions are in microns).



# WLP & Redistribution

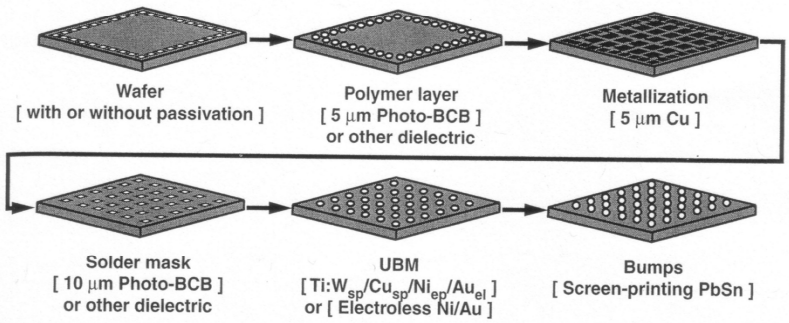



FIGURE 10.11 Typical redistribution technology. (*Courtesy of IZM Berlin*)

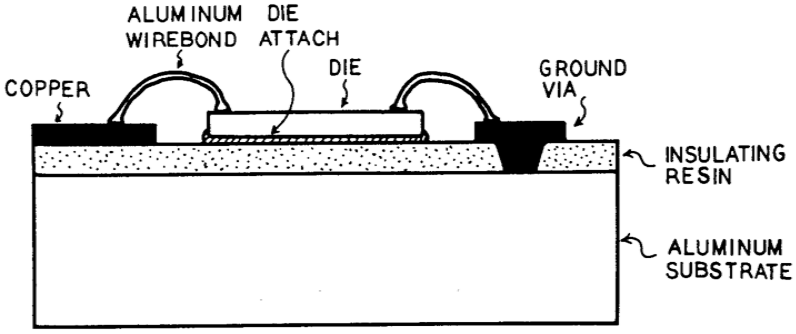



**FIGURE 3.16** Insulated metal substrate



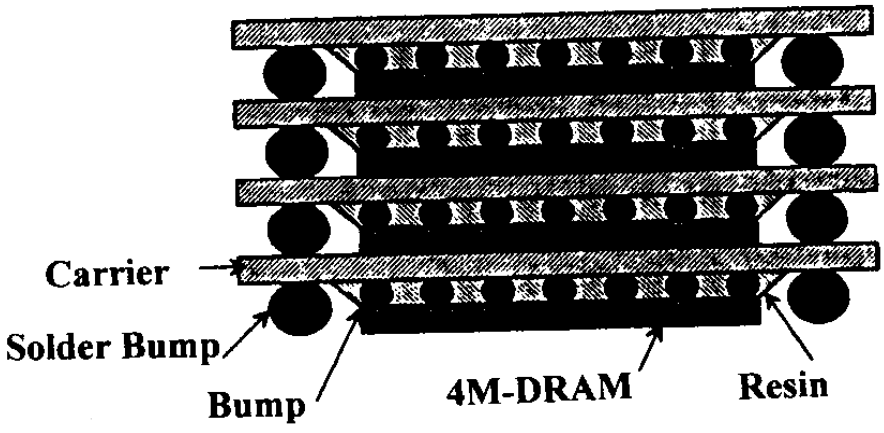



**Figure 1.11** NEC's 3-D stack-up chip scale package (CSP) for memory devices.

# Lecture Summary


- Standard packages
  - Encapsulation
- First level interconnect (chip to package):
  - Wire-bond, TAB, flip-chip (C4)
- Second-level interconnect (package to board):
  - PTH, SMT, PGA, BGA (C4/C5), etc
- MCMs, CSPs, WLP, etc

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