Nanopackaging:

Nanotechnologies & Electronics Packaging

Part B CNTs (2)

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Portland State UNIVERSITY

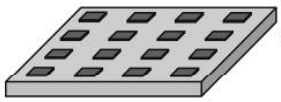
Nanoelectronics & Packaging Lab

CNT Contact Bumps

(Liu & Wang)

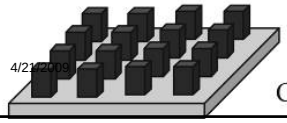
Silicon Chip

Lithography, Evaporation & Liftoff

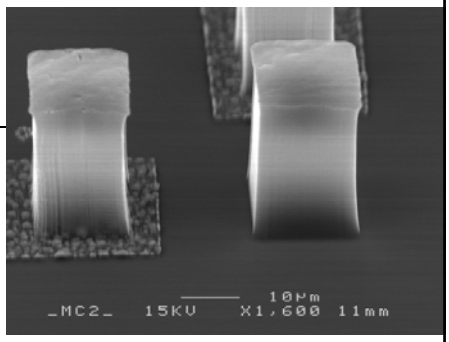


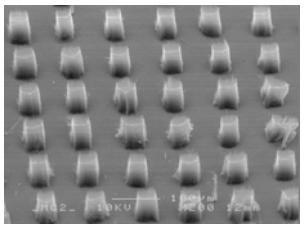
Chip with catalyst

PECVD



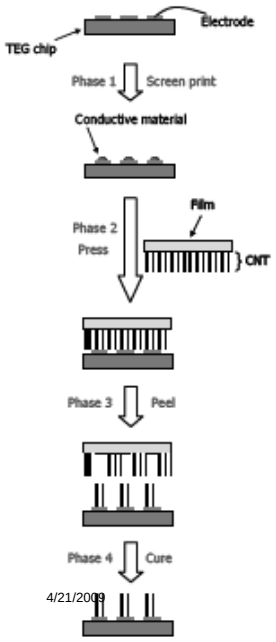
Chip with CNT bumps





CNT Bumps

(Ikuo Soga et al ECTC'08)



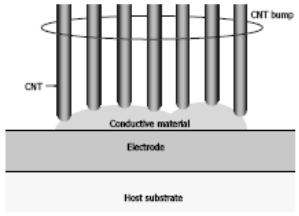
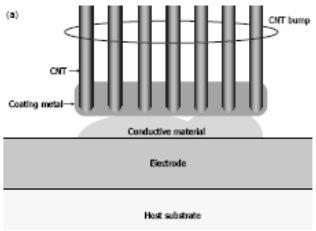


Figure 7: Contact condition of the CNT bump



High resistances with "capped" ends

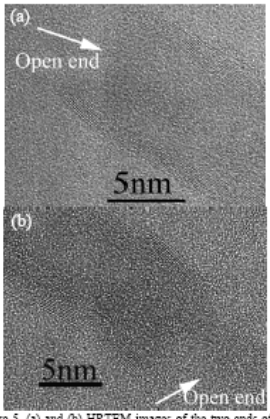


Figure 5. (a) and (b) HRTEM images of the two ends of one nanotube, showing that the two ends are open.

Zhu et al, ECTC'06

Placement of Aligned CNTs for Packaging

(Kyoung-Sik Moon, ECTC'08; Zhu et al, ECTC'06; Soga et al, ECTC'08)

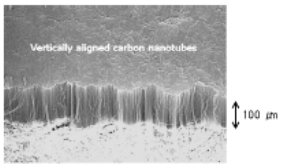


Figure 1: SEM image of the vertically aligned CNTs

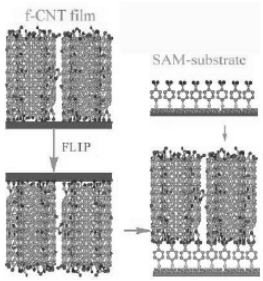


Fig. 1 Chemical anchoring technology

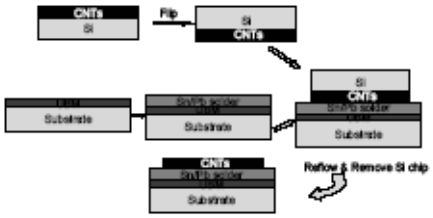


Figure 6. Schematic diagram of "CNT transfer technology". UBM: under bump metallization. See the text for detailed explanations.

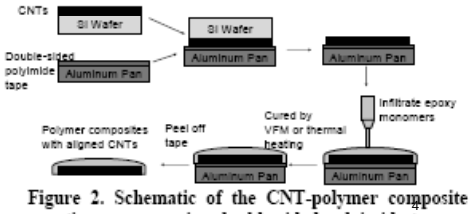
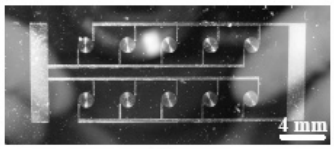


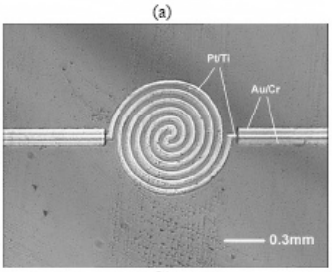
Figure 2. Schematic of the CNT-polymer composite preparation process using double-sided polyimide tape as a transferring layer.

CNT Growth on Si: Localized heating

(Ting Xu et al, ECTC'08) ΔT~400°C



(a)



(b)

Figure 2. Optical image of the fabricated micro-heater. (a) micro-heater array; (b) detailed view of an individual heater.

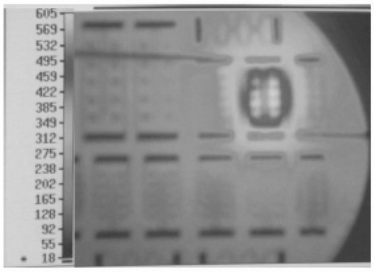
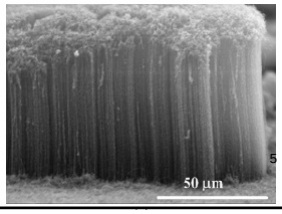
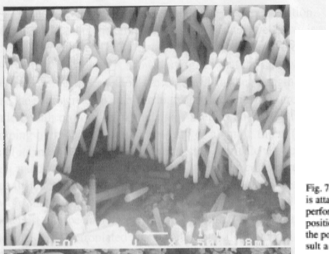


Figure 3. Temperature distribution on the wafer after the DC voltage was supplied to the micro-heaters.



Ni Nanowire Contacts [IEEE Trans CPT (2008)]



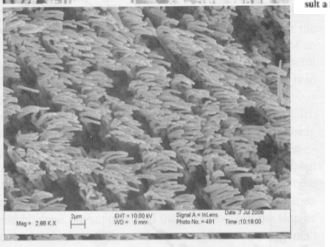


Fig. 9. SEM images of Nickel Nanowires: 0.2 × 20 μm nickel nanowires (top) are fabricated from polycarbonate filters, and 0.2 × 10 μm curved nickel nanowires (bottom) are fabricated by polishing.

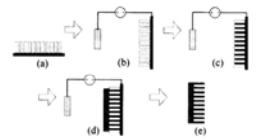


Fig. 7. Electrodeposition process of nickel nanowires. (a) A porous membrane is attached to a sacrificial conductive substrate. (b) Nickel electrodeposition is performed. (c) Nickel nanowires are formed inside the membrane. (d) Electrodeposition continues to build a nickel substrate above the porous membrane after the pores are completely filled. (e) The porous membrane is etched away to result a final product.

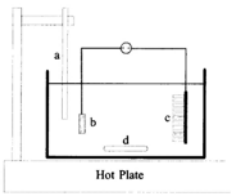
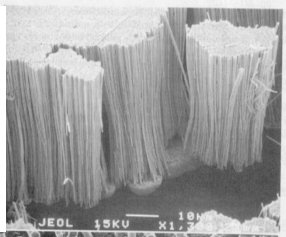


Fig. 8. Schematic of electrodeposition apparatus. (a) External temperature probe. (b) Nickel anode. (c) Cathode with a filter attached. (d) Magnetic stir rod.



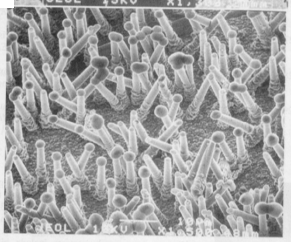


Fig. 13. Scanning electron microscope (SEM) Images of nickel nanowires. 0.2 × 60 μm nickel nanowires (top) are fabricated from an alumina filter and 2.0 × 20 μm nickel nanowires with a sphere at the tip (bottom) are fabricated by replating.

Ni Nanowire Contacts

[IEEE Trans CPT (2008)]

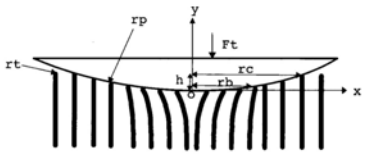
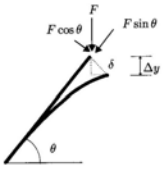


Fig. 4. Ideal Elastic Columns Model: nanowires are considered to be vertical columns.



ntilever deflected at the base with an angle θ has vertical stil

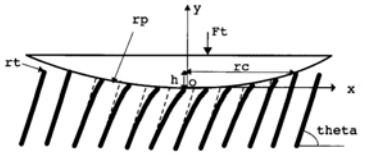


Fig. 1. Inclined Cantilever Model: nanowires are considered to be inclined at the base wi

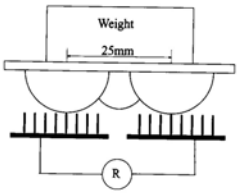
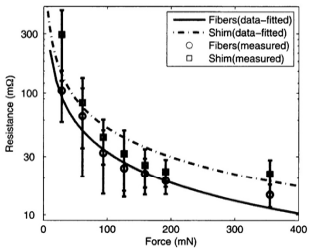


Fig. 10. Apparatus for resistance measurement between a spherical tip probe and an array of nickel nanowires.



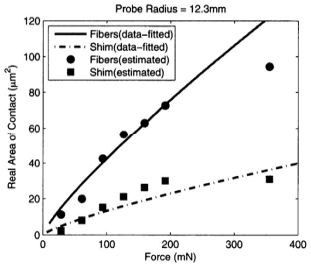
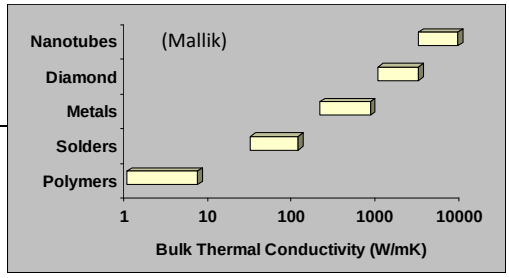


Fig. 11. Resistance of an array of $0.2 \times 10\ \mu$m nickel nanowires and the resistance of a nickel shim were measured by a micro-ohmmeter (15 measurements per load). The squares and the circles are the data points and vertical bars represent one standard deviation. Data-fitted curves are the best fit to data using oxide thickness of 6.4 Å (fibers) and 5.8 Å (shim), Fermi Level 7.0 eV, dielectric constant 4 (see text).

CNT Thermal Interface

(Zhang et al, ECTC'06)



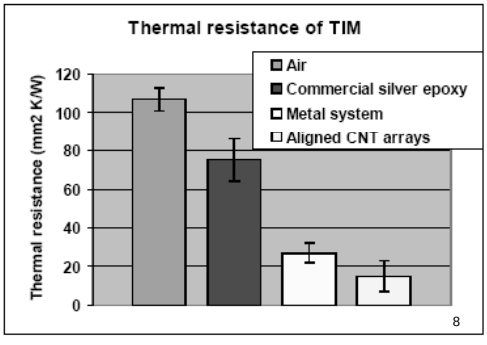
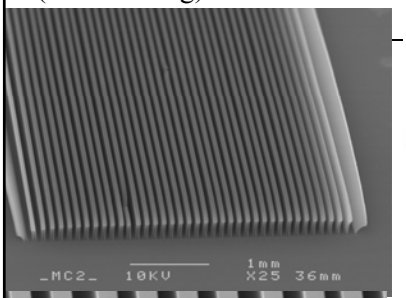
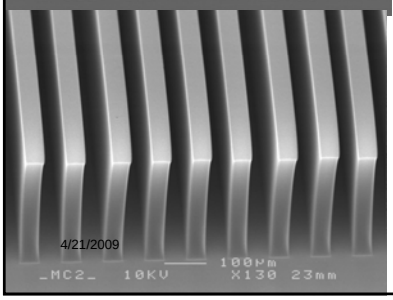


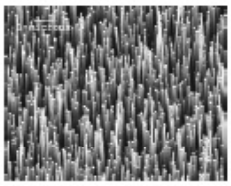
Fig.8 Measured thermal resistance of different TIM

CNT Heat Sink

(Liu & Wang)







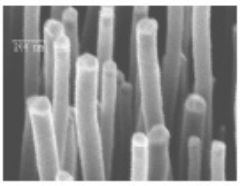
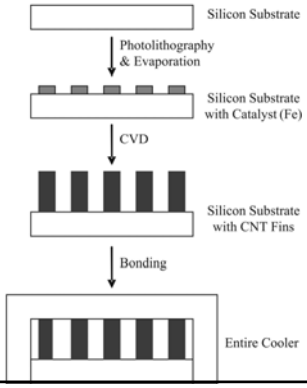
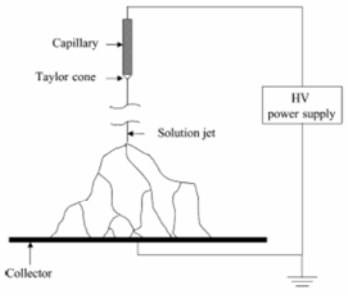


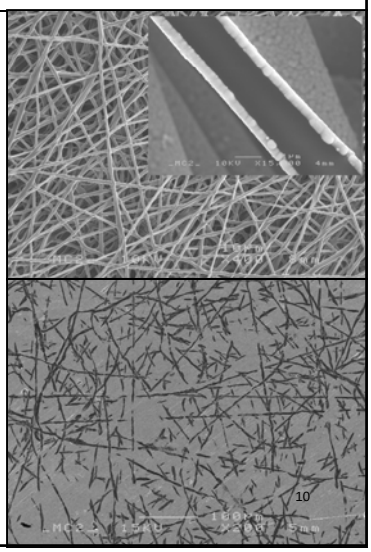
Fig. 1. SEM image of MWCNT from plasma deposition. The scale bar on the left is 1 micron and the one on the right is 200 nm.



Electrospun Thermal Interface Material

(Recent developments: electroplated surfaces, LMP alloy "filler")





(Liu & Wang)

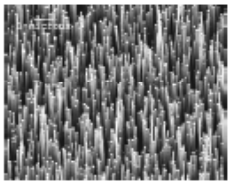
Results – Reference Comparison/Evaluation

Four state-of-the-art commercial thermal adhesive pastes were evaluated for reference purposes

Material	Test Time (hrs)	Pressure (kPa)	BLT (µm)	R_{th} (Kmm^2W^{-1})	K_{eff} ($Wm^{-1}K^{-1}$)
Material A	1.5	200 ± 1	16 ± 2	20.8 ± 1.2	0.77 ± 0.11
Material B	1.5	200 ± 1	54 ± 2	14.4 ± 1.2	3.75 ± 0.34
Material C	1.5	200 ± 1	60 ± 2	16.8 ± 1.2	3.56 ± 0.28
Material D	1.5	200 ± 1	22 ± 2	7.4 ± 1.2	3.05 ± 0.74
SMIT Center	1.5	200 ± 1	74 ± 2	10.0 ± 1.2	7.90 ± 0.89

Thermal conductivity with C-fibers & CNTs

[Zhong et al, APM'05]



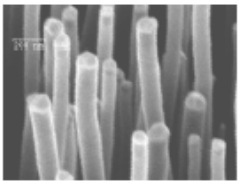
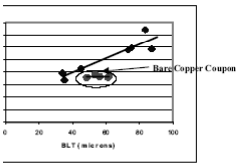


Fig. 1. SEM image of MWCNT from plasma deposition. The scale bar on the left is 1 micron and the one on the right is 200 nm.



rformance with CNT-coated copper (diamonds) versus e TIM used was commercial grade US3282 from GE

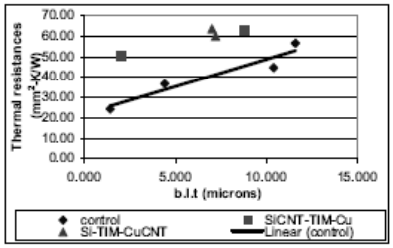


Fig 10. Thermal performances with CNT-coated copper (triangles) or silicon (squares) substrates. The adhesive used was unfilled ECC4865 from GE Silicones, Waterford.

CNT arrays for superhydrophobic surfaces for MEMS stiction avoidance [Zhu et al, ECTC'06]

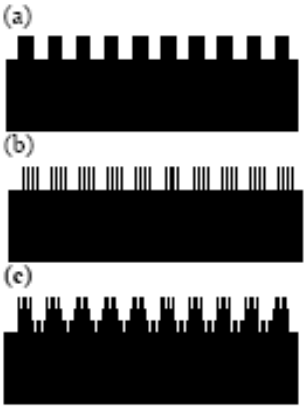


Figure 1. Schematic representations of (a) micro-scale roughness created by photolithography; (b) aligned CNT arrays that establish two-tier roughness; (c) aligned CNT films on patterned silicon surfaces.

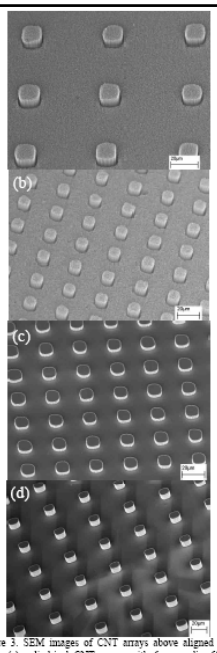


Figure 3. SEM images of CNT arrays above aligned CNT films: (a) cylindrical CNT arrays with 6 μm radius,60 μm pitch, and 4 μm height; (b) cylinder CNT arrays with 6 μm radius, 30 μm pitch, and 9.5 μm height. SEM images of cylindrical silicon arrays: (c) Si arrays with 6 μm radius, 30 μm pitch, and 4 μm height, (d) Si arrays with 6 μm radius, 60 μm pitch, and 9.5 μm height.