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Effects of non-ideal switches in PWM switching converters

WISAM M. MOUSSA† and JAMES E. MORRIS‡

This paper presents new models that account for the non-ideal properties of semiconductor BJT switches responsible for the switching action in PWM converters. These models can be used for both the DC and small-signal AC analyses of PWM switching regulators. Terminal voltages and currents of the switching elements of the converter are related using switching functions which account for the non-ideal characteristics of the semiconductor switches, such as delay, rise, storage, fall and reverse recovery times. Models have been derived and used in DC and AC small-signal analysis of the three basic topologies: buck, boost, and buck-boost converters operating in the continuous conduction mode. The switching times of the semiconductor switches result in a change of the duty cycle which affects both the DC and small-signal performance of the converters. The change in the DC conversion ratio due to the switching times is shown for the three converters. It is also shown that a resistance is introduced into the AC model. This resistance can be positive, which increases the damping in the system, or can be negative, leading to instability.

1. Introduction

Modelling of switching converters in most cases assumes ideal switches in the analysis. But with recent increases in switching frequencies, the non-ideal characteristics of the switches have become more pronounced, and play an increasing role in the performance of the converter. The state-space averaging technique (Middlebrook and C'uk 1977) is used for the DC and AC analyses of switching converters, its drawback being its limitation to ideal switches only. Rim *et al.* 1988) used an extension of the state-space method to analyse non-ideal converters. State equations were written and the analyses carried out using matrix operations. This method lacks modelling capabilities. The PWM switch technique, recently introduced by Vorperian (1990), is very versatile and requires only conventional circuit analysis. This technique can incorporate non-ideal parameters of the circuit by modifying its model, but a separate analysis is performed to account for non-ideal parameters, such as the storage time of the switching device. New models are derived below which account for the non-ideal characteristics of the semiconductor switches such as delay, rise, storage fall, and reverse recovery times. These models can be used for the DC and small signal AC analyses of the three basic converters: buck, boost, and buck–boost converters operating in the continuous conduction mode of operation. The derivations of the DC and AC models are presented in Section 2. It is shown that an AC resistance is introduced in the small-signal model which depends not only on the storage time of the switching transistor as reported by Polivka *et al.* (1980) but also on the delay, rise, fall, and reverse recovery times of the semiconductor switches. In Section 3 the DC model is used to compute the DC

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†IBM Corp. T78/4-4-392, Endicott, NY 13760, U.S.A.

‡Department of Electrical Engineering, State University of New York—Binghamton, Binghamton, NY 13902, U.S.A.

conversion ratios for the converters. Finally the AC model is used to compute the small-signal transfer functions for the three converters in Section 4.

2. Development of the model

The power stage of the three basic converters, buck, boost and buck-boost, operating in continuous conduction mode are shown in Fig. 1. Following the designations by Vorperian (1990), terminal assignments are indicted for the currents and voltages of the circuit responsible for the switching action within a power converter. The designations of the terminals *a*, *p* and *c* refer to active (transistor), passive (diode) and common, respectively. The switching waveforms of the assigned terminals are shown in Fig. 2. The instantaneous relationship between terminal currents and terminal voltages can be deduced from Fig. 2 and are given by:

$$v_{ac}(t)=s_1(t)v_{ap}(t) \tag{1}$$

and

$$i_p(t)=s_2(t)i_c(t) \tag{2}$$

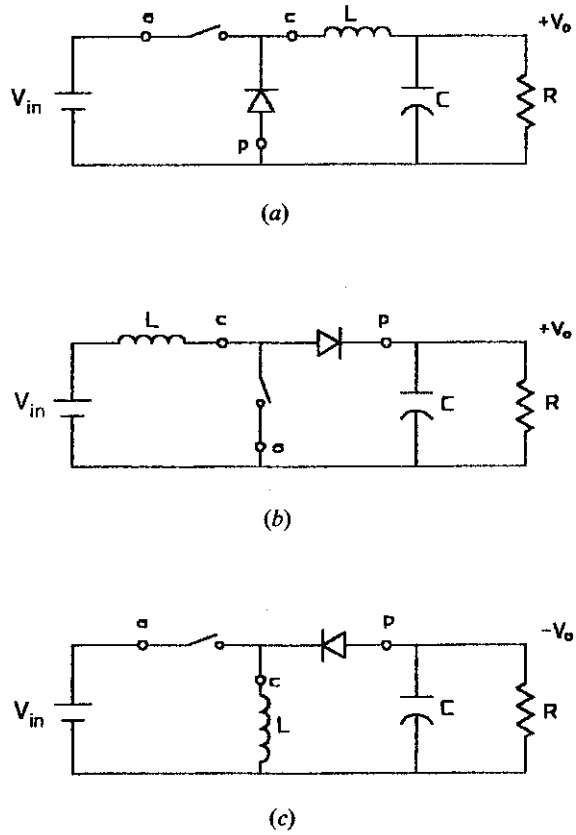

Figure 1. PWM switching converters. (*a*) buck converter; (*b*) boost converter; (*c*) Buck-boost converter.

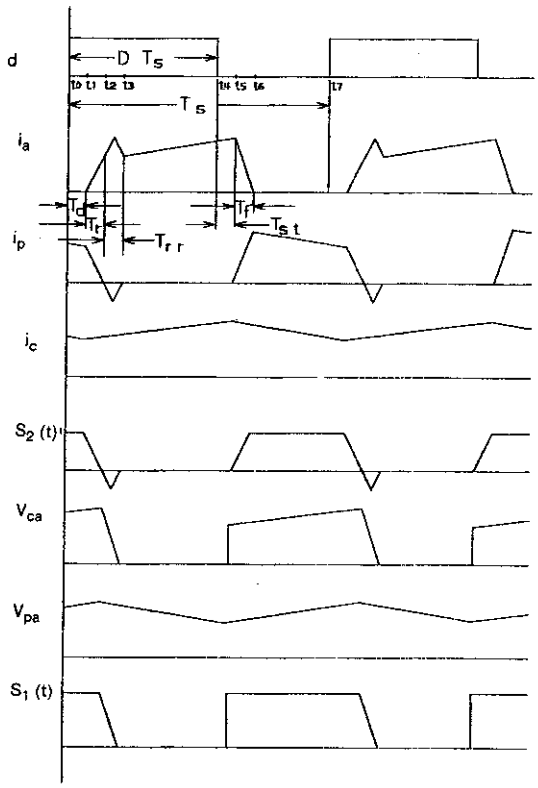

Figure 2. Switching waveforms of terminal currents and voltages.

where $s_1(t)$ and $s_2(t)$ are referred to as the switching functions. These switching functions account for all the non-ideal characteristics present in the switching circuit, and can be determined once all the switching times and all the voltage drops of the semiconductor devices are known.

2.1. *Averaging*

For a well designed power converter under steady-state operation, the state variables, the inductor current and the capacitor voltage, have very small ripple quantities on top of their steady-state operating points. This requires that the corner frequency of the output filter, f_o, be well below the switching frequency, f_s, ($f_o \ll f_s$), hence, the expansion of the Fourier series of the signals of interest are dominated by their DC component (the average over the switching cycle). Therefore (1) and (2) can be replaced by their averaged quantities, and are given by:

$$\langle v_{ac}(t)\rangle = \frac{1}{T_s}\sum_{i=1}^{7}\int_{t_{i-1}}^{t_i} s_1(t)v_{ap}(t)\,dt \tag{3}$$

where

$$\sum_{i=1}^{7} t_i - t_{i-1} = T_s \tag{4}$$

where the angle brackets $\langle . \rangle$ denote an average taken over a single switching cycle.

Assuming a low ripple voltage, substituting the corresponding values for $v_{ap}(t)$ and $s_1(t)$ for each interval from Fig. 2, (3) can be written as:

$$\langle v_{ac}(t) \rangle \simeq \langle s_1(t) \rangle \langle v_{ap}(t) \rangle \tag{5}$$

where

$$\langle v_{ap}(t) \rangle = V_{ap} \tag{6}$$

and

$$\langle s_1(t) \rangle = S_1(D, I_c = D' + T_1 f_s = 1 - D + T_1 f_s \tag{7}$$

where

$$T_1(I_c) = T_d + T_r + T_{rr} - T_{st}. \tag{8}$$

T_d, T_f, T_r, T_{rr} and T_{st} are the delay, fall, rise, reverse recovery and storage times of the switching devices, respectively. D is the duty ratio of modulation, defined as the ratio of the turn ON time, T_{on}, of the PWM pulse to the switching period, T_s, $D' = 1 - D$, f_s is the switching frequency ($f_s = 1/T_s$). The switching times of the semiconductor switches are functions of the common terminal current, I_c.

Similarly, averaging for (2), assuming low ripple current in $i_c(t)$:

$$\langle i_p(t) \rangle \simeq \langle s_2(t) \rangle \langle i_c(t) \rangle \tag{9}$$

where

$$\langle i_c(t) \rangle = I_c \tag{10}$$

and

$$\langle s_2(t) \rangle = S_2(D, I_c = D' + T_2 f_s = 1 - D + T_2 f_s \tag{11}$$

where

$$T_2(I_c) = T_d + \frac{T_r}{2} - \frac{T_{rr}^2}{4T_r} - \frac{T_f}{2} - T_{st} \tag{12}$$

It can be seen from (7) and (11) that S_1 and S_2 reduce to the ideal values of D' if all the switching times are neglected.

2.2. *Small-signal perturbation and linearization*

If the above circuit undergoes a small perturbation around a steady-state operating point given by:

$$\begin{aligned} v_{ac} &= V_{ac} + \hat{v}_{ac} \quad i_c = I_c + \hat{i}_c \\ v_{ap} &= V_{ap} + \hat{v}_{ap} \quad d = D + \hat{d} \end{aligned} \tag{13}$$

where upper case letters represent DC quantities and lower case letters with a circumflex represent small-signal AC quantities.

Assuming the perturbations are small enough such that:

$$\frac{\hat{v}_{ac}}{V_{ac}} \ll 1 \quad \frac{\hat{i}_c}{I_c} \ll 1$$
$$\frac{\hat{v}_{ap}}{V_{ap}} \ll 1 \quad \frac{\hat{d}}{D} \ll 1 \tag{14}$$

The perturbed quantities can be approximated by the first two terms of their Taylor series expansion around the operating points V_{ac}, V_{ap}, and I_c. Substituting (13) in (5) results in:

$$(V_{ac}+\hat{v}_{ac})=\left[S_1(D,I_c)+\frac{\partial S_1(D,I_c)}{\partial D}\hat{d}+\frac{\partial S_1(D,I_c)}{\partial I_c}\hat{i}_c\right](V_{ap}+\hat{v}_{ap}) \tag{15}$$

Expanding (15) and neglecting second- and higher-order terms, a DC solution is found, given by:

$$V_{ac}=S_1(D,I_c)V_{ap} \tag{16}$$

and a small-signal AC solution given by:

$$\hat{v}_{ac}=S_1(D,I_c)\hat{v}_{ap}+V_{ap}\frac{\partial S_1(D,I_c)}{\partial D}\hat{d}+V_{ap}\frac{\partial S_1(D,I_c)}{\partial I_c}\hat{i}_c \tag{17}$$

Substituting (7) in (17) results in:

$$\hat{v}_{ac}=S_1(D,I_c)\hat{v}_{ap}-V_{ap}\hat{d}+R_m i_c \tag{18}$$

where R_m has dimensions of resistance, and is referred to as the modulation resistance, given by:

$$R_m=V_{ap}f_s\frac{\partial T_1}{\partial I_c} \tag{19}$$

where the value of R_m depends on the operating point, V_{ap}, which can be determined from the DC analysis prior to the small-signal analysis. It is also dependent on the switching frequency, f_s, and the rate of change of T_1 with respect to the common terminal current, I_c.

Similarly for (9):

$$(I_p+\hat{i}_p)=\left[S_2(D,I_c)+\frac{\partial S_2(D,I_c)}{\partial D}\hat{d}+\frac{\partial S_2(D,I_c)}{\partial I_c}\hat{i}_c\right](I_c+\hat{i}_c) \tag{20}$$

from which the DC solution is given by:

$$I_p=S_2(D,I_c)I_c \tag{21}$$

and an AC solution is given by:

$$\hat{i}_p = S_k \hat{i}_c - I_c \hat{d} \tag{22}$$

where

$$S_k = S_2(D, I_c) + k_i = D' + T_2 f_s + k_i \tag{23}$$

and

$$k_i = +I_c f_s \frac{\partial T_2}{\partial I_c} \tag{24}$$

and where k_i is a dimensionless quantity which is a function of the operating point I_c, the switching frequency, f_s, and the rate of change of T_2 with respect to the common terminal current I_c.

From (16) and (21), (18) and (22), DC and AC models are generated and shown in Figs. 3 and 4, respectively. These models represent the DC and the linearized small-signal behaviours of the converter over the full switching cycle, and can be substituted in the circuit for calculating steady-state and small-signal transfer functions.

It should be noted that in the small-signal model a voltage source and a current source are circuit dependent sources which the other sources are controlled through the duty cycle. Also, in the AC model a resistance, R_m has been introduced which is dependent on the switching times of the devices, such as the rise time, storage time and reverse recovery time of the diode. This resistance has been shown to exist by Polivka *et al.* (1980), who modified the state-space averaging technique to include the storage time effect in order to account for conspicuous discrepancies in the phase shifts between predicted and measured values. The value of R_m depends, not only on the storage time as reported by Polivka *et al.*, but also on the delay, rise, fall and reverse recovery times of the switching devices. This resistance can be positive, which increases the damping in the system, or negative leading to instability (Thottuvelil *et al.* 1988), the conditions which determine these alternatives are fully analysed elsewhere (Polivka *et al.* 1980).

3. DC analysis

Examples are shown below of the use of each model, with the aim of bringing out their essential features. DC analysis for the three basic converters, buck, boost and buck-boost can be carried out by simply replacing the switching elements in these converters with the DC model shown in Fig. 3, while maintaining the respective

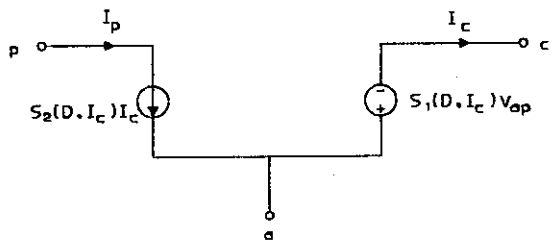

Figure 3. DC model equivalent circuit.

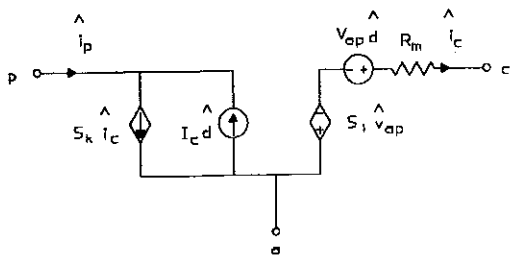

Figure 4. AC model equivalent circuit.

terminals as defined in Fig. 1. It should be noted that reactive elements for the DC analysis are either shorted (inductor) or opened (capacitor). Figure 5 shows the DC model of a buck converter incorporating the DC switching function model. To compute the DC voltage conversion ratio, the DC operating point is determined from Fig. 5:

$$V_{ap}=V_{in} \quad \text{and} \quad I_c=I_o \tag{25}$$

from KVL:

$$V_{in}=S_1V_{ap}+I_oR_L+V_o \tag{26}$$

or

$$V_{in}(1-S_1)=V_o\left[1+\frac{R_L}{R}\right] \tag{27}$$

therefore:

$$M=\frac{V_o}{V_{in}}=(1-S_1)\frac{\mathrm{R}}{R_L+R} \tag{28}$$

and substituting for S_1 from (7):

$$M=[1-(1-D+T_1f_s)]\frac{R}{R_L+R}=(D-T_1f_s)\frac{R}{R_L+R} \tag{29}$$

It can be seen from (29), that the DC conversion ratio for the buck converter reduces to the well-known quantity D times the correction factor of R and R_L when all the

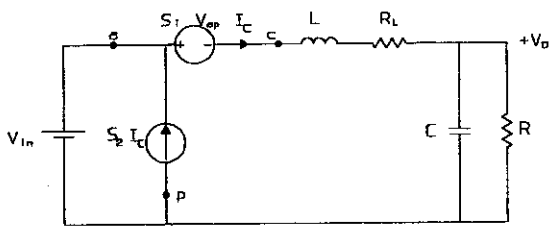

Figure 5. Buck converter DC model.

	M
Buck	$(D-T_1f_s)\dfrac{R}{R_L+R}$
Boost	$\dfrac{D'+T_2f_s}{(D'+T_1f_s)(D'+T_2f_s)+\dfrac{R_L}{R}}$
Buck-boost	$\dfrac{(D-T_1f_s)(D'+T_2f_s)}{\dfrac{R_L}{R}+(D'+T_1f_s)(D'+T_2f_s)}$

Table 1. DC transfer functions.

non-ideal properties (determined through T_1f_s) are ignored. The non-ideal term is frequency dependent and increases as f_s is increased, this is in contrast to the ideal case, where M is a constant and independent of frequency. A summary of the DC conversion ratios of the three converters is given in Table 1.

4. Small-signal AC analysis

The AC analysis is carried out by inserting the equivalent AC model, shown in Fig. 5, in each converter while maintaining the terminals as defined in Fig. 1. The AC model for a buck converter is shown in Fig. 6, where the operating points were computed from the DC analysis and given by (25). To compute the input impedance, defined as $\hat{v}_{in}/\hat{i}_{in}$, from Fig. 7 with $\hat{d}=0$:

$$Z_{in}=\frac{1}{(D-T_1f_s)(D-T_2f_s-k_i)}\frac{\Delta_{buck}}{sC(R+R_c)+1} \tag{30}$$

where

$$\Delta_{buck}=s^2[LC(R+R_c)]+s\{L+[(R+R_c)(R_m+R_L)+RR_c]C\}+R+R_m+R_L \tag{31}$$

This is in contrast to the input impedance derived using ideal switches and given by

$$Z_{in}=\frac{1}{D^2}\frac{\Delta_{buck-ideal}}{sC(R+R_c)+1} \tag{32}$$

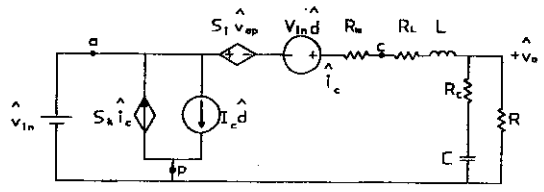

Figure 6. Buck converter AC model.

Audiosusceptibility $\hat{y}_o/\hat{y}_{in}$	$(1-S_1)\dfrac{R(sCR_c+1)}{\Delta_{buck}}$
Output impedance Z_0	$\dfrac{R(sCR_c+1)(R_m+R_L+sL)}{\Delta_{buck}}$
Input impedance Z_{in}	$\dfrac{1}{(1-S_1)(1-S_k)}\dfrac{\Delta_{buck}}{sC(R_c+R)+1}$
Control to output $\hat{v}_o/\hat{d}$	$V_{in}\dfrac{R(sCR_c+1)}{\Delta_{buck}}$
Δ_{buck}	$s^2[LC(R+R_c)]+s\{L+[(R+R_c)(R_m+R_L+RR_c]C\}+R+R_m+R_L$

Table 2. Buck small-signal transfer functions.

where

$$\Delta_{buck-ideal}=s^2[LC(R+R_c)]+s\{L+[(R+R_c)R_L+RR_c]C\}+R+R_L \tag{33}$$

From (30), it can be seen that when all non-ideal parameters of the switches are ignored, (30) reduces to the ideal case as given in (32). Tables 2–4 are summaries of the small-signal transfer functions for the three converters. It should be noted that all the transfer functions given in Tables 2–4 reduce to the well-known transfer functions derived using the state space averaging method (Middlebrook and C'uk 1977) for the ideal case. It can also be seen from Tables 2–4, that the buck converter is the least susceptible of the three converters to the non-ideal characteristics of the switches, as it has minimum changes in the locations of either the poles or the zeros due to the non-ideal parameters.

Audiosusceptibility $\hat{v}_o/\hat{v}_{in}$	$S_k\dfrac{R(sCR_c+1)}{\Delta_{boost}}$
Output impedance Z_0	$\dfrac{R(sCR_c+1)(R_m+R_L+sL)}{\Delta_{boost}}$
Input impedance Z_{in}	$\dfrac{\Delta_{boost}}{sC(R_c+R)+1}$
Control to output $\hat{v}_o/\hat{d}$	$\dfrac{V_o}{S_2}\dfrac{(1+sCR_c)(sL+R_L+R_m-S_2S_kR)}{\Delta_{boost}}$
Δ_{boost}	$s^2[LC(R+R_c)]+s\{L+[(R+R_c)(R_m+R_L+S_1S_kRR_c]C\}+S_1S_kR+R_m+R_L$

Table 3. Boost small-signal transfer functions.

Audiosusceptibility $\hat{v}_o/\hat{v}_{in}$	$S_k(1-S_1)\dfrac{R(sCR_c+1)}{\Delta_{buck-boost}}$
Output impedance Z_0	$\dfrac{R(sCR_c+1)(R_m+R_L+sL)}{\Delta_{buck-boost}}$
Input impedance Z_{in}	$\dfrac{1}{(1-S_1)(1-S_k)}\dfrac{\Delta_{buck-boost}}{sC(R_c+R)+1}$
Control to output $\hat{v}_o/\hat{d}$	$\dfrac{V_o}{S_2S_k(1-S_1)}\dfrac{(1+sCR_c)[S_2R+S_1S_k-R(sCR_c+1)(R_L+R_m+sL)]}{\Delta_{buck-boost}}$
$\Delta_{buck-boost}$	$s^2[LC(R+R_c)]+s\{L+[(R+R_c)(R_m+R_L+S_1S_kRR_c]C\}$ $+S_1S_kR+R_m+R_L$

Table 4. Buck-boost small-signal transfer functions.

5. Conclusions

A new model for PWM switching converters was derived using switching functions that include non-ideal characteristics of the switches. It can be used to analyse the tree basic topologies, the buck, boost, and buck-boost converters. It is shown that the non-ideal parameters of the switches introduce an AC resistance in the circuit, confirming earlier predictions (Polivka *et al.* 1980). This resistance value can be positive which increases the damping or it can be negative, potentially leading to instability. It is also shown that the value of this resistance depends on the delay, rise, storage, fall, and reverse recovery times of the switching devices.

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References

Middlebrook, R. D., and C'uk, S., 1977, A general unified approach to modelling switching converter power stages. *International Journal of Electronics*, **42**, 521–550.

Polivka, W. M., Chetty, R. P. K., and Middlebrook, R. D., 1980, State-space average modeling of converters with parasitics and storage-time modulation. *I.E.E.E. PESC Conference Record*, pp. 219–243.

Rim, C. T., Joung, G. B., and Cho, G. H., 1988, A state-space modeling of non-ideal DC–DC converters. *I.E.E.E. PESC Conference Record*, pp. 943–950.

Thottuvelil, V., Wilson, T., and Owen, H., 1988, Study of oscillations due to turn-off-delay variations in DC-to-DC converters employing BJT. *I.E.E.E. PESC Conference Record*, pp. 951–959.

Vorperian, V., 1990, Simplified analysis of PWM converters using the model of the PWM switch, Parts I and II. *I.E.E.E. Transactions on Aerospace and Electronic Systems*, **26**, 490–505.