New method of modelling a multipeak resonant tunnelling diode

C. Y. Huang, J. E. Morris, Y. K. Su and T. H. Kuo

Indexing terms: Resonant tunnelling devices, Semiconductor device models

The authors report an improved approach to modelling the I-V characteristics of a multipeak resonant tunnelling diode (RTD). The merit of this new RTD model is demonstrated.

Introduction: Multistable memory systems with anywhere from three- to nine-state RTD circuits have been developed [1–3]. These multivalued memory (MVM) circuits usually consist of RTDs in series, in parallel, or in integrated circuit form, with a resistor or a depletion MESFET device as a load element. To demonstrate the features of these RTD-based MVM circuits, SPICE simulation has often been used [1, 4]. By using a piecewise linear (PWL) approximation technique, in which multiple breakpoints can be easily inserted, this new RTD model has been successfully implemented in a three-state MVM circuit, and shown good agreement with the simulated results of the two-peak RTD I-V curve, load lines, and switching operation waveforms in [1].

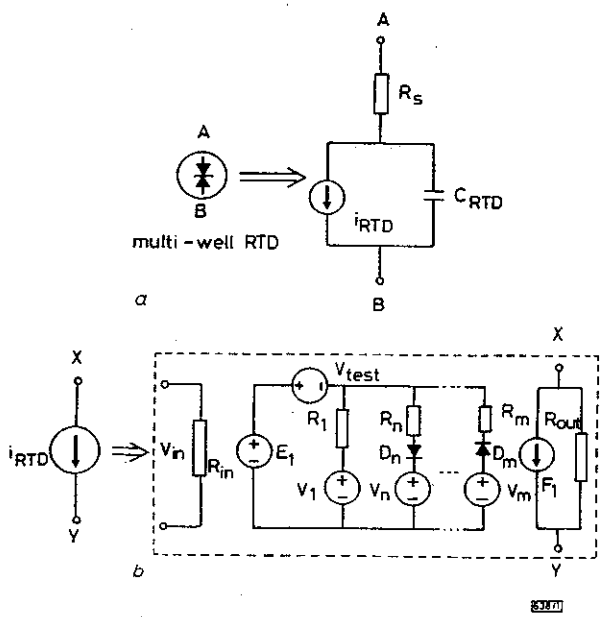

Fig. 1 *Proposed new multipeak RTD model, and equivalent circuit to implement the PWL technique in the voltage-controlled current source of the new multipeak RTD mode*

a RTD model
b Equivalent circuit

Model: Fig. 1*a* shows that a multipeak RTD can be modelled by its parasitic resistance R_s in series with the parallel combination of its intrinsic capacitance C_{RTD} and a voltage-controlled current source $i_{RTD}(v)$ which represents the PWL I-V characteristics of the multipeak RTD as shown in Fig. 1*b* that consists of input, function, and output stages. Resistors R_{in} and R_{out} represent the input and output resistance of the RTD-based MVM circuit and can both be designated as 1MΩ for SPICE simulation. With unity gain, E_1 is identical to the input voltage V_{in} which represents the sweeping DC voltage range of the multipeak RTD I-V curve. A dummy voltage source V_{test} measures the output current flowing through the RTD. F_1 is a linear dependent current source, which has unity gain and reflects the RTD current V_{test} to the output stage. The branches R_1, V_1 and R_n, D_n, V_n represent the positive resistance sections of the RTD I-V curve, and the branches of R_1, V_1 and R_m, D_m, V_m form the negative resistance sections. The element values of R_1 and V_1 can be calculated by using the Kirchhoff circuit theorem in the PWL equivalent circuit. V_n ... V_m are the chosen breakpoint voltages of the RTD I-V curve. R_n ... R_m are obtained from the following equations:

$$R_n = \frac{1}{M_B - M_A}$$

where M_A and M_B are the slopes of two adjoining upward linear segments of the RTD I-V curve with $M_B > M_A$, and

$$R_m = \frac{1}{M_C - M_D}$$

where M_C and M_D are the slopes of two adjoining downward linear segments of the RTD I-V curve with $M_C > M_D$.

We now compare this new multipeak RTD model with the Kuo model [5]. The new model requires 16 and 34 circuit elements in the PWL equivalent circuit for the SPICE simulation of one-peak and four-peak RTD I-V curves, respectively. However, the Kuo RTD model requires 18 and 102 elements for one-peak and four-peak RTD I-V curves, respectively. As for the corresponding SPICE code, this model necessitates 18 and 36 normal job cards for one-peak and four-peak simulations, respectively, compared with the Kuo model's 21 and 120 normal job cards for the one-peak and four-peak cases, respectively.

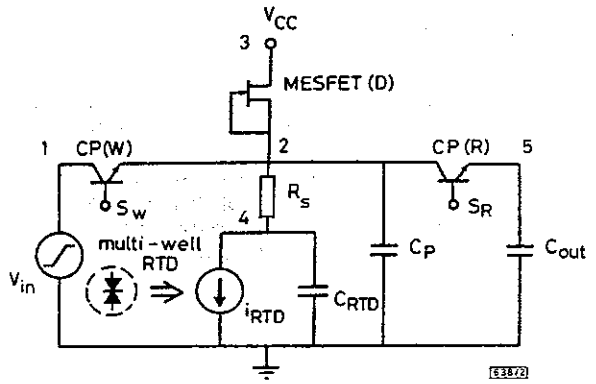

Fig. 2 *Equivalent circuit model for three-state RTD-based MVM circuit*

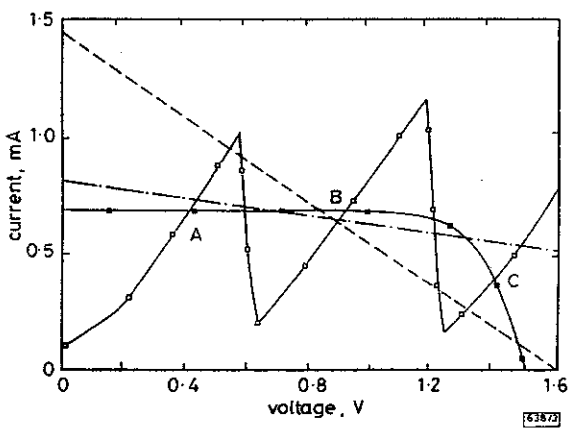

Fig. 3 *Simulated I-V characteristics of two-peak I-V curve for three-state RTD-based MVM circuit with MESFET depletion load, and with resistor loads of R_L = 1.1 and 6.5kΩ*

– – – – R_L = 1.1kΩ
—·— R_L = 6.5kΩ

Results: Simply using the PWL breakpoint feature in SPICE, and the related parameters and I-V data from [1], Fig. 3 shows the simulated results of two-peak RTD I-V characteristics from a three-state MVM circuit shown in Fig. 2, together with the load line from a constant current source implemented by the source-gate connected depletion mode MESFET. The constant current can be calculated directly from the Curtice SPICE model for modelling GaAs MESFETs [6], as

$$I_{DS} = \beta(1 + \lambda V_{DS})(V_{GS} - V_{TO})\tanh(\alpha V_{DS}) \quad (1)$$

The load line for resistor R_L = 1.1kΩ is plotted by the dashed line for the same supply voltage of 1.6V as that of MESFET load. It can intersect the positive resistance sections of the two-peak RTD I-V curve at three operation points A, B, and C. These three operation points represent three memory states of the MVM circuit. If the larger load resistor of ~6.5kΩ is chosen, of which the

load line is also drawn by the long-dashed line, then the noise margin for all three states could be approximately the same as obtained with the MESFET depletion-load case, but a larger supply voltage of ~5V is required.

To demonstrate the storage property of the MVM circuit, the circuit of [1] is used along with the new multipeak RTD model as illustrated in Fig. 2. The input of write and read pulse signals, $CP(W)$ and $CP(R)$, respectively, alternately turn the two *npn* transistors (switch model) on and off. When the write switch S_W controlled by write pulse $CP(W)$ is on, the corresponding state V_N is written into the MVM circuit where $1 \leq N \leq 3$.

$CP(R)$ controls the read switch S_R and gate the V_{in} to the output of the circuit C_{out}. By choosing the proper MESFET drain current to be midway between the peak and valley currents of the RTDs, set to the maximum drain current of the MESFET of ~0.7mA calculated from eqn. 1, and the typical parameters $R_S = 6\Omega$, $C_{RTD} = 0.02$pF, $C_p = 0.1$pF, $C_{out} = 0.1$pF for simulation, we can obtain three operating points A, B and C with their corresponding values of ~0.45, ~0.9, and ~1.4V as depicted in Fig. 3. Fig. 4 shows the simulated results of the corresponding voltage waveforms of V_{out} at output node 5. We find that the values of A to C in Fig. 3 match very closely with those of Fig. 4.

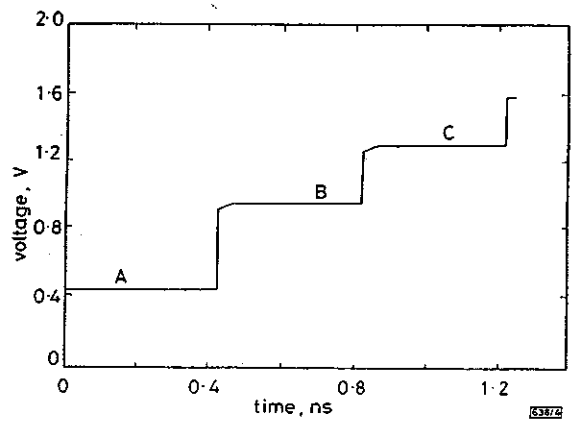

Fig. 4 *Simulated results of logic operation waveforms for three-state MVM circuit*

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C. Y. Huang and J. E. Morris (*Department of Electrical Engineering, State University of New York at Binghamton, Binghamton, New York, 13902-6000, USA*)

Y. K. Su and T. H. Kuo (*Department of Electrical Engineering, National Cheng Kung University, Tainan, Taiwan*)

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