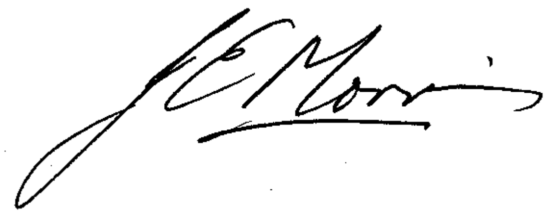

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ELECTRICAL PERFORMANCE MODELING FOR THE CALCE CADMP-II ELECTRONICS PACKAGE RELIABILITY SOFTWARE

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Abstract

The CALCE CADMP-II software package is well known for its physics-of-failure approach to the problem of reliability lifetime prediction for microelectronics packages, including plastic DIL and hermetic devices, MCMs and single-chip carriers, PTH and SMT, PGA and BGA, etc. In making mechanical and materials design changes to a package for reliability improvements, the designer inevitably also makes changes to the electrical performance of the package. As an enhancement to the existing software capability, performance information is being made available to the designer within CADMP. The emphasis is on speed and accessibility, so the models employed are approximate, with three selectable levels of accuracy. The first includes worst-case estimates of delta-I (simultaneous switching) noise, crosstalk, and EMI potential, with calculations based on extracted geometrical parameters being performed and displayed automatically. Transmission line delay effects are included at this level only if the chip-carrier substrate contains a ground plane. The second level calculates delta-I noise and crosstalk for the entire lead set, but modeled simply as parasitic and mutual inductive elements. The third level invokes SPICE for more accurate modeling of the various noise types, with a much more complete set of lead material parameters, but limited to interactions between single line pairs. A feature of the electrical modeling approach is its flexibility in dealing with multiple package types within a single, simple system, and especially in dealing with multiple co-planar lead/ground lines.

Keywords: *CADMP, physics-of-failure, reliability, lifetime prediction, delta-I, simultaneous switching, crosstalk.*

I. INTRODUCTION:

The CADMP electronics packaging reliability software is well established for physics-of-failure based reliability lifetime prediction for electronics packages. Electrical performance algorithms are being incorporated to set up quick approximate models to indicate to a user testing changes for reliability enhancement whether those changes will have significant impact on electrical performance. The goal is to provide a quick, approximate "early warning system" on the effects mechanical and materials design changes may have on the existing design performance.

The noise mechanisms considered include:

(1) Delta-I switching noise, which causes the power-to-ground supply voltage to sag with supply current transients due to the effect of parasitic line inductance, $\Delta I = L.dI/dt$. Also known as "ground bounce!"

(2) Crosstalk between lines due to capacitive and inductive coupling by electric and magnetic fields, associated (respectively) with the "driven" source signal voltage and current, leads to spurious signals on the "quiet" line.

(3) Reflections on the transmission line structures formed by the interconnect lines and the current return paths may lead to signal "overshoot" or "undershoot" depending on source and load impedance mis-matches. Line delays are significant for the larger current packages functioning at higher frequencies. For CMOS devices, the typical line load is a gate capacitance, which may be approximated by an open circuit (since gate charging times Z_0C_g<<line delays, where Z_0 is the line characteristic impedance).

(4) Electromagnetic emissions from the package, and susceptibility to environmental fields, are due to the formation of effective antennas by the package wiring.

The simulations also provide for two more detailed analyses:

(1) An inductive crosstalk model which has the advantage that it can provide a noise figure for every interconnect line, with specified currents in any or every line, but with no provision for capacitive effects, series resistance, time delays, etc.

(2) SPICE modeling, which has the potential for the greatest modeling accuracy, but is strictly limited in the number of lossy and/or coupled lines it can handle. It can therefore only simulate the effect of one line on one other at a time.

Environmental effects (e.g. temperature coefficient of resistance for metals, or the influence of humidity on polymer dielectric constants (e.g. 20% for polyimides)) are included via the CADMP environmental data-base. These will affect the transmission line parameters Z_0, line loss, coupling coefficients, etc.

II. PACKAGE SEGMENTATION:

The core CADMP package models include pin-through-hole (PTH) types, (both dual-in-line (DIL) and single-in-line packages (DIPs & SIPs) and pin-grid array (PGA)), and surface mount technology (SMT) devices (SMDs,) (with leaded or leadless chip carriers (LCC, LLCC), in land grid array (LGA) or ball-grid array (BGA) configurations, and quad flat-packs (QFPs), etc). Future technologies such as chip-scale packages (CSP), chip-on-board (COB) or direct-chip-attach (DCA) are also accommodated. Two additional packages, the leadframe plastic DIP and multichip module (MCM) are also covered, but need some special consideration. In order to handle the variety of technologies, and their combinations, the package interconnect is sectioned as shown in Figure 1, with each section modeled separately. Although one can obviously break the interconnect down further, a maximum of these four sections seems to provide an adequate approximation for all packages considered. In principle, all sections might need to be represented as transmission lines, but this is precluded by the limitations on circuit complexity and coupled lossy lines in SPICE, so the inner and outer bonds, (which tend to be shorter than the others), are approximated by lumped R-L sections, and the levels 2 and 4 by transmission lines. The number of lossy lines in SPICE is also limited, so the lead is represented as an ideal lossless line and the substrate metallization as a lossy line, based on the assumption that the metallization thickness is always significantly less than lead thicknesses, and hence will display the more significant resistance.

Interconnect sub-sections:-

1. Inner to die (TAB/flip-chip/wire-bond)
2. Substrate (Metallization/NA)
3. Outer to lead (Wire-bond/via/NA)
4. Lead (BGA/lead)

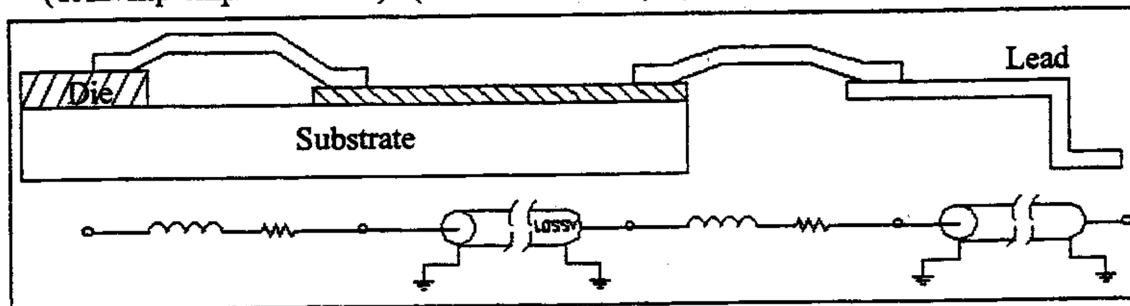


Figure 1. Segmentation of package interconnect for modeling

Four examples of how this sectioning system would work for specific packages are shown in Figure 2, summarized in Table 1. In Figure 2a, (plastic DIP) the leads are modeled as two transmission lines, and the die and leads are encapsulated in plastic, Figure 2b represents high performance hermetic devices, and quad peripheral packages. Figures 2c and 2d represent the shift to contact arrays, which create some difficulties in the automated determination of appropriate lead lengths.

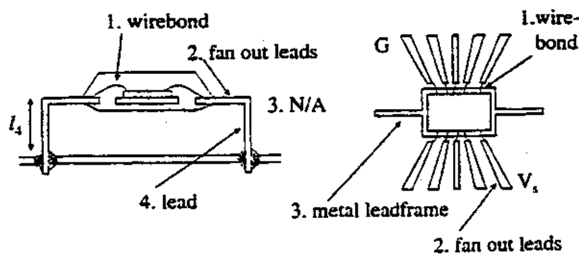


Figure 2(a): DIL

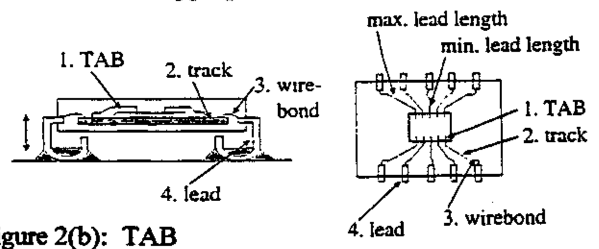


Figure 2(b): TAB

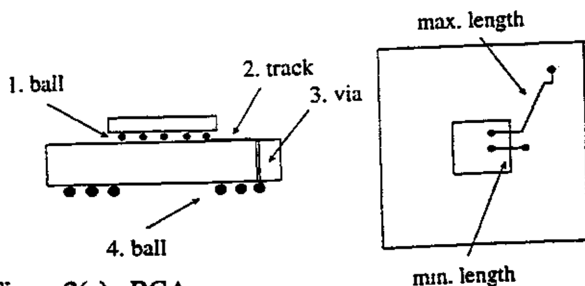


Figure 2(c): BGA

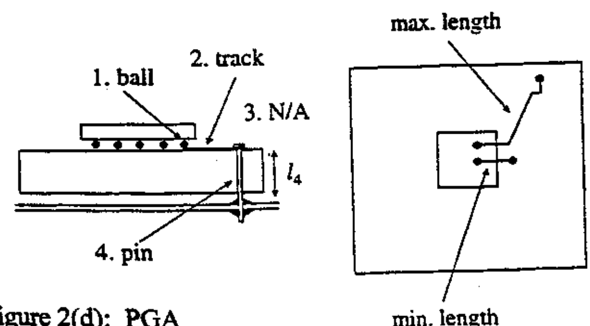


Figure 2(d): PGA

Figure 2. Package interconnect segmentation examples

Package type	1 Inner bond	2 Substrate	3 Outer bond	4 Lead
Plastic DIP	Wire bond	Fan-out lead	None	PTH lead
QFP LCC LLCC	Wire bond TAB Flip-chip	Thin/thick film on ceramic chip carrier	Wire bond	J-lead Gullwing Package pads
PGA BGA		MLC	None (PGA) Via* (BGA)	Pin BGA
CSP	Wire bond Flip-chip	Various	Wire bond Via	BGA etc
MCM-Si MCM-D MCM-C MCM-L	Wire bond TAB Flip-chip	HDI Cu on polymer film MLC Cu on FR4	Wire bond Via	PGA BGA Leads

* Vias may connect to inner or outer bonds or both; model total via lengths.

Table 1. Interconnect system segmentation detail.

III. CO-PLANAR LINES:

There is an issue with how to handle interconnects (for multiple package geometries) which require transmission-line treatments, since their propagation delay times exceed signal times of interest, but which do not have well-defined and tightly coupled ground returns, as assumed in elementary transmission-line theory. CADMP has not needed to include ground planes in the past (except for the MCM model) since the relatively thin metal ground layers are not mechanically significant, but they are easily added for state-of-the-art high frequency packages. But even if the substrate contains a ground plane, the external leads may not form the traditional textbook transmission line structure. In these cases there is a coplanar array of coupled transmission lines, where the ground reference is remote from the signal lines in question (Figure 3a), which are more tightly coupled to each other than to ground (giving rise to significant crosstalk noise). It is possible to model such a system in SPICE, (Section VI), but for only two lines plus the implied ground, or for the whole array with a lumped model (Section V.) But first the electrical line parameters (Figure 3b, where L_i is the self-inductance of an individual "isolated" wire,) must be transformed to an equivalent ground return model. See Figure 3c, where only the inductances are shown; these include mutual inductances (Figure 3d.)

Referencing all lines to v_n, and taking as $v_n = 0$ to define ground, (subscript "g")

$$L_s = L_i' = L_i + L_g - M_{ig} - M_{gi}$$

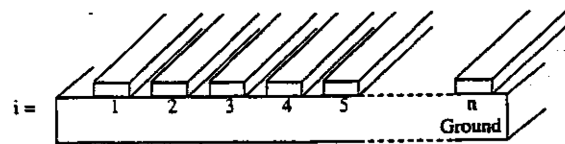
Where $M_{ig} = M_{gi}$, and if the lines are identical, $L_i = L_g$, so

$$L_i' = 2(L_i - M_{ig}).$$

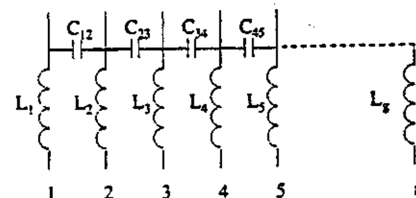
For the purposes of evaluating crosstalk in the transmission line system, the mutual inductances become

$$M_{ij}' = M_{ij} + (L_g - M_{ig} - M_{jg})$$

Note: The self-inductance L_s includes both internal and external inductances $L_s = L_{si} + L_{se}$, where L_{si} varies with frequency (skin effect.)

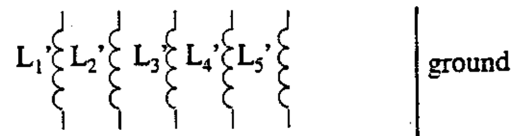


(a) Co-planar lines

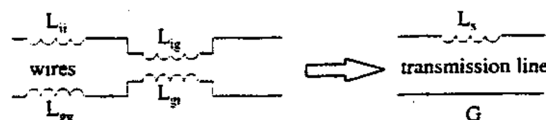


plus mutual inductance M_{ij}

(b) Electrical parameters



(c) Inductance transformation



(d) Process includes mutual inductance

Figure 3 Multiple co-planar line transformation

The determination of line to ground capacitances is trivial, apart from the problem of determining an effective dielectric constant for surface films. Line inductances and capacitances must be determined for each specific geometry, and appropriate formulae can be found in standard references. But note that few allow for skin effects.

IV. WORST-CASE ANALYSIS:

(1) Worst-case lumped-parameter models:

(a) Δ-I noise (Figure 4a)

$$\Delta V = \Delta I.R_P + L_P.\Delta I/t_P - \Delta I.t_P/(C_P/2)$$

R_p is usually ignored. C_p represents the distributed line capacitance, approximated by two lumped end-sections.

(b) Crosstalk (Figure 4b)

The model assumes weak coupling, i.e. mutual inductance L_m << self inductance L_P,.

At die: $V_{CT_D}=[Z_D Z_P/(Z_D+Z_P)][C_m\Delta V+L_m\Delta I/Z_P]/t_P$

At PWB: $V_{CT_P}=[Z_D Z_P/(Z_D+Z_P)][C_m\Delta V+L_m\Delta I/Z_D]/t_P$

(c) EMC/EMI (Figure 4c)

Emissions At "far field" distance r (≥λ=c/f) from the line of length L and area A=Ld, the radiated electric field strength is $E=E_D+E_{CM}$, where E_D due to the differential current I_D is

$$E_D=131.6x10^{-16}f^2AI_D/r \text{ V/m}$$

& E_{CM} from common mode current I_{CM} is (for L≤λ)

$$E_{CM}=4\pi x10^{-7}fLI_{CM}/r \text{ V/m}$$

where $I_D=(I_1+I_2)/2$ and $I_{CM}=(I_1-I_2)/2$. Common mode currents are ideally zero, but small values can lead to CM dominance over differential. For the differential current, the maximum value can be taken to be the supply current, but the user must specify a non-ideal common mode estimate. For digital systems, use $f=2\pi/t_r$. There are many different standards for EM radiation limits, but for guidance the EU limit is E≤100μV/m at r=10m (class A) or 3m (class B).

Susceptibility For the line shown, with capacitance C per unit length the induced voltages are

$$V_S = -j\omega\,[R_L R_S/(R_L + R_S)]\,[Ld]\,[C - (\mu_0/\eta_0)/R_L]$$

$$V_L = -j\omega\,[R_L R_S/(R_L + R_S)]\,[Ld]\,[C + (\mu_0/\eta_0)/R_S]$$

where $E=E_t=\eta_0 H_n$, and $\eta_0=120\pi=377\Omega$.

As an example of an EU standard, the device must function in a field of E=3V/m.

(2) Worst-case transmission line: The previous section models all four interconnect sub-sections as RLC networks, but better approximation is possible if a ground plane transmission line structure exists, still using only direct substitution formulae.

(a) Reflections (Figure 4d)

An estimate of mis-match reflection problems, can be gained by calculation of the initial load transient at V_L

$$V_{trans} = 2\,V_{sig}/[(1 + R_S/Z_0)\,(1 + Z_0/R_L)]$$

If signal amplitude equals supply voltage, the transient can exceed supply. For the package, the line may be transmitting to or from the chip, so one must consider both R_S & $R_L = R_{DIE}$ & R_{PWB}

(b) Crosstalk (Figure 4e)

Crosstalk on a transmission line exhibits line delay effects. Quiet line far-end and near-end voltages are

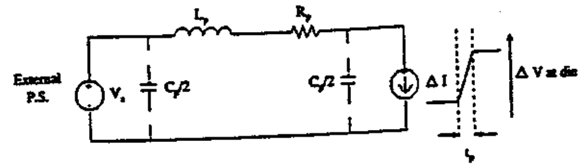
$$V_{FE} = [(C_m Z_0 - L_m Z_0)/2]\,V_{sig}$$

$$V_{NE} = [(C_m Z_0 + L_m Z_0)\,(4\varepsilon_r^{1/2}/c]\,V_{sig}$$

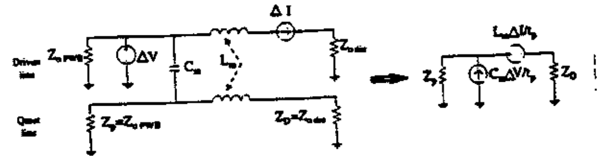
This saturation value of V_{NE}, is reached only if line length $l > cT_R/2\sqrt{\varepsilon_r}$, otherwise near-end noise voltage peals at

$$V_{NE}'=V_{NE}(2l\sqrt{\varepsilon_r}/cT_R).$$

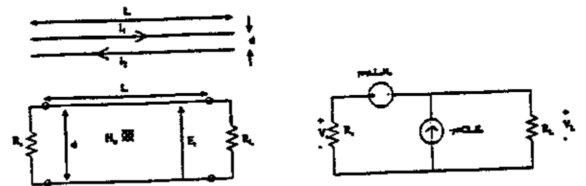
These values are for perfect matching $R_S=R_L=Z_0$, multiply by $2R/(R+Z_0)$, with $R=R_L$ or R_S, to include the initial mis-match effect.



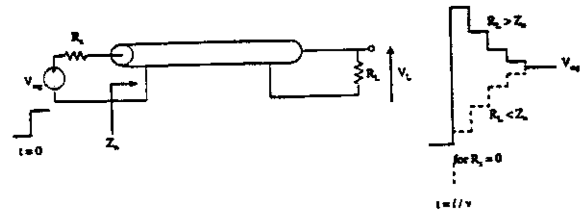
(a) Delta-I (simultaneous switching) noise



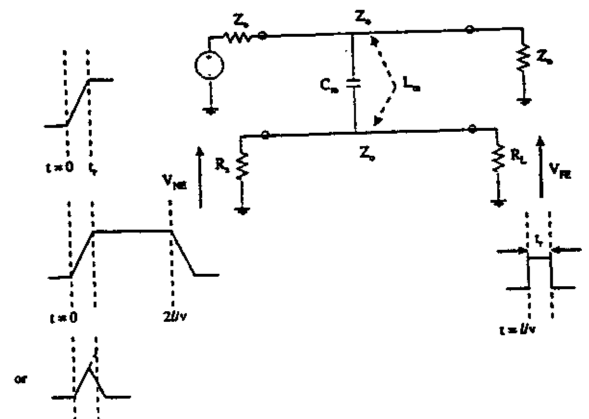
(b) Lumped parameter crosstalk



(c) Electromagnetic compatibility/interference



(d) Transmission line reflections



(e) Transmission line crosstalk

Figure 4. Worst case modeling

These calculations are performed and the outcomes are posted automatically, but the user must call the next two.

V. INDUCTIVE NOISE MATRIX:

This treatment expands and generalizes the model presented in Poon. Lines are treated by their lumped self and mutual inductances, so transmission line effects are lost. But the benefit of this particular calculation is that the inductive noise levels are calculated for all lines simultaneously, to show how the noise varies from line to line, and which ones are most at risk. The algorithm is especially useful for the co-planar line systems characteristic of the outer (peripheral) leads and substrates without ground planes.

Part of the algorithm is devoted to the identification of n_P power and n_G ground leads per side, and their arrangement, with $n_P=n_G=n$, for simplicity, and $n_S=N-2n$ signal lines per side (Figure 5). The same system can be used for ΔI noise and crosstalk, which differ only in the source signal. For ΔI noise, set all signal currents $I_s=0$ and define total power current I_p; for crosstalk, $I_p=0$ and define I_s on one or more signal lines.

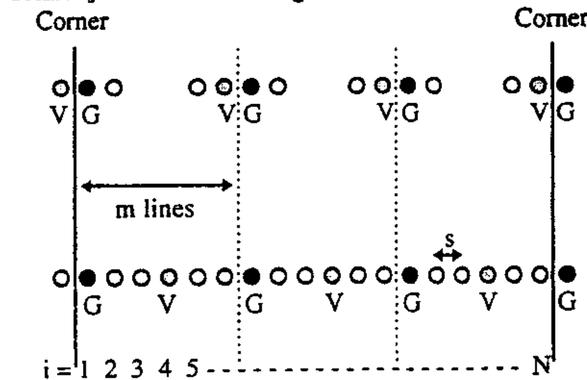


Figure 5. Power , ground and signal layouts.

For each line i=1,2,.....N, the inductive noise is: $v_i = \sum_{j=1}^{N} L_{ij}\, dI_j/dt$, in matrix form (writing $i_j=dI_j/dt$):

$$\begin{vmatrix} v_1\\ v_2\\ v_3\\ \vdots\\ v_N\\ \hline 0 \end{vmatrix} = \begin{vmatrix} L_{11} & L_{12} & \cdots & L_{1N}\\ L_{21} & L_{22} & & L_{2N}\\ \vdots & & \ddots & \vdots\\ L_{N1} & \cdots & \cdots & L_{NN}\\ \hline 1 & 1 & 1 \cdots & 1 \end{vmatrix} \begin{vmatrix} i_1\\ i_2\\ \vdots\\ i_N \end{vmatrix}$$

The solutions of all v_i are trivial if all L_{ij} and dI_i/dt are known, but a more useful result is sought. In practice the power supply and ground currents will NOT be equally distributed. Redistribution can be permitted by setting the local ground (or power) fluctuations to be equal, i.e. effectively assuming a "solid" ground of equal voltage at all points. In practice this is not quite so either, but we can get estimates of both extreme approximations by forcing the power supply currents to be equal (to determine the noise voltage range) and the ground voltages to be equal (to determine the current variations.) So the equations need to be rearranged so that the I_P's and I_s's form (N-n) "known" quantities, and n I_G's, v_G, and (N-n) v_i's ($\neq v_G$) make up (N+1) unknowns. (The (N+1)th equation is $\sum I=0$.) Reorganization of the matrix gives the result below, (with $v_1=v_G$ and n=1 for illustrative purposes), which is of the form

$$|A|\,|y| = |X|\,|x|,$$

with solution

$$|y| = |A|^{-1}\,|X|\,|x|.$$

$$\begin{vmatrix} 1 & 0 & 0 & \cdots & 0 & 0 & -L_{11} & \cdots & \cdots\\ 1 & 0 & \cdots & \cdots & \cdots & 0 & & & \\ \vdots & \vdots & & & & \vdots & & & \\ 1 & 0 & \cdots & \cdots & \cdots & 0 & & & \\ \hline 0 & 1 & 0 & 0 & & 0 & & & \\ 0 & 0 & 1 & 0 & & & & & \\ & 0 & 0 & 1 & & & & & \\ & & & & \ddots & & & & \\ & & & & 1 & 0 & & & \\ 0 & 0 & & & 0 & 1 & -L_{N1} & \cdots & \cdots\\ \hline 0 & 0 & 0 & \cdots & 0 & 0 & -1 & -1 \cdots & -1 \end{vmatrix} \begin{vmatrix} V_1\\ \hline V_2\\ \vdots\\ V_N\\ \hline I_1\\ \vdots\\ \vdots \end{vmatrix} = \begin{vmatrix} L_{12} & \cdots & L_{1N}\\ \vdots & & \vdots\\ \vdots & & \vdots\\ L_{N2} & \cdots & L_{NN}\\ \hline 1 \quad 1 & & 1 \quad 1 \end{vmatrix} \begin{vmatrix} I_2\\ \vdots\\ \vdots\\ I_N \end{vmatrix}$$

VI SPICE MODELING:

The SPICE template solves the circuit shown, in Figure 6 for crosstalk or delta-I noise. The user can over-ride the assumption of identical lines. The user determines whether the two lines selected are adjacent (default) or remote. Note that three interconnect lines are being modeled here, including the ground reference The PWB impedance will be the PWB line characteristic impedance, but assignment of the die impedance depends on die technology. C_{DIE} accommodates both line and gate capacitances. R_{DIE} must be adjusted for signal or power leads.

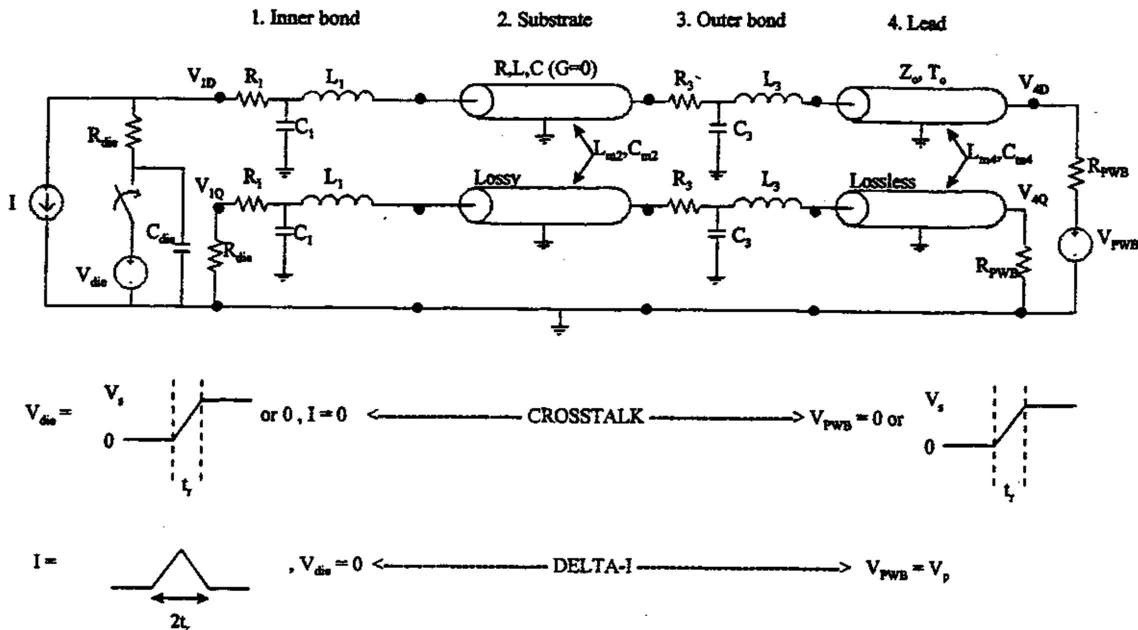


Figure 6 SPICE circuit for modeling template

(S closed unless: CMOS Delta-I [$R_{DIE} \rightarrow \infty$] or CMOS PWB source crosstalk)

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