Nanopackaging:
Nanotechnologies and Electronics Packaging

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Abstract

Nanotechnologies are being applied to microelectronics packaging, primarily in the applications of nanoparticle nanocomposites, or in the exploitation of the superior mechanical, electrical, or thermal properties of carbon nanotubes. Composite materials are studied for high-k dielectrics, electrically conductive adhesives, conductive "inks," underfill fillers, and solder enhancement. These trends are demonstrated by paper presentations over the past few years at various conferences, which show research to be concentrated in relatively few laboratories, with little work being done on the packaging requirements of the new nanoelectronics technologies

Introduction

Nanotechnologies have already yielded everyday consumer benefits beyond stain-resistant clothing and transparent sun-block, and are moving in on electronics packaging. The definition of nanotechnology is usually taken to be where the size of the functional element falls below 100nm or 0.1µm, and with 90nm CMOS in production, the nanoelectronics era is already here. Nanotechnology drivers are the varied ways in which materials properties change at low dimensions. Electron transport mechanisms at small dimensions include ballistic transport, severe mean free path restrictions in very small nanoparticles, various forms of electron tunneling, electron hopping mechanisms, and more. Other physical property changes include:

- Melting point depression, i.e. the reduction of metal melting points at small sizes, typically under 5nm
- Sintering by thermally activated surface self-diffusion
- The Coulomb blockade effect
- Theoretical maximum mechanical strengths in single grain material structures
- Optical scattering by nanoparticles 1 to 2 orders smaller than the wavelength of visible light
- The enhanced chemical activities of nanoparticles, which make them effective as catalysts, and other effects of the high surface-to-volume ratio

Computer modeling

The modeling of two-part composite materials must include both phases, as a general principle of inclusion of the nanoscale structural detail in expanded material models, and the material properties of both must be known at the nanoscale.

Nanoparticles

(a) High-*k* dielectrics: Embedded passive components need high dielectric constant materials for low area capacitors, which can be achieved by the inclusion of high

dielectric constant particulates at minimal thickness. The particles may be ceramic, i.e typically barium titanate, or metallic for a target *k* of 50-200. *k*~150 has been achieved, but with high leakage. Aluminum particles reduce leakage due to the native oxide coating.

(b) Electrically conductive adhesives: The addition of Ag nanoparticles does not necessarily improve conductance, due to mean free path restrictions and added interface resistances, but can achieve dramatic results, however, by sintering wide area contacts between flakes.

(c) Interconnect : Surface electrical interconnect for board and package can be achieved by screen or ink-jet printing nanoscale metal colloids in suspension, with electrical continuity established by sintering.

(d) Silica filler in underfill: Nanoscale silica particles in underfill resist settling and may permit UV optical curing.

(e) Solder: The addition of Pt, Ni, or Co nanoparticles to SnAgCu solders eliminates Kirkendall voids, reduces intermetallic compound (IMC) growth, and reduces IMC grain sizes, significantly improving drop test performance. Similarly, Ni or Mo nanoparticles promote finer grain growth, increased creep resistance, and better contact wetting. Nanoparticles in the grain boundaries also inhibit grain boundary sliding and thermomechanical fatigue.

Carbon Nanotubes

(a) Solder: The addition of carbon nanotubes (CNTs) to solder can also have beneficial effects, e.g. 30-50% improvements in tensile strength.

(b) Thermal: The high thermal conductivity of CNTs is being exploited for microelectronics chip cooling both directly in conductive cooling and indirectly in convective cooling systems. For conductive systems, the key is to establish CNT alignment, since the thermal conductivities of random arrays (of CNTs and carbon fibers alike) fall far short of expectation, showing no advantages over conventional materials. Vertical CNTs are first grown on both the aluminum heat sink and silicon chip surfaces, which are then positioned ~μm apart in a CVD furnace, enabling the CNTs from the two surfaces to grow further and connect with each other. The use of a liquid crystal resin matrix can impose structural order on the CNT alignment to yield a seven-fold improvement in thermal conductivity.

So far, convective CNT cooling has been limited to the use of μm-scale clusters of vertically grown nanotubes. These clusters define micro-channels for coolant flow which look very much like the metal or silicon structures they aim to replace, with similar thermal performances. The problem is that the flowing coolant is only in contact with the outermost CNTs of the clusters, and the internal CNTs are not even in good contact with each other.

(c) Electrical: If CNT ends are opened after growth, the open ends permit better wetting by Sn/Pb for improved electrical contact. Metal and carbon loaded polymers have long been used for high-frequency conductors in electromagnetic shielding, and multi-walled CNTs have been studied in polymer matrices for the purpose. CNT replacement of ICA metal filler does not even match the electrical conductivity of standard materials, but 10-50μm long Ag/Co nanowires of 200nm diameter can be maintained in a parallel vertical orientation by a magnetic field while polymer resin flows around them, to form an anisotropic conductive film for z-axis contacts.

Nanoscale Structures

The micro-spring contacts originally developed at PARC-Xerox have been down-sized to 10nm wide cantilevers, still 10μm long, for biological sensing.

Conclusion

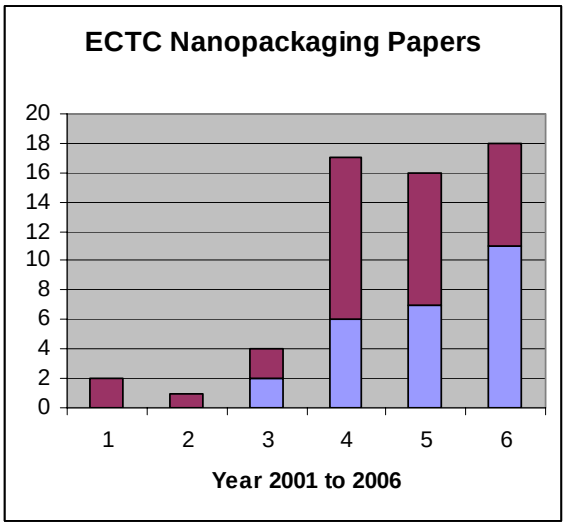
The importance of nanoelectronics and "electro-nanotechnologies" in the future is sufficiently well recognized to have become the subject of industrial and government policy roadmaps, and the academic world is responding with graduate level courses, (but few textbooks.)

One of the surprising observations to come out of this survey has been that there is almost no work reported on the development of packaging for candidate next-generation nanoelectronics technologies, (e.g. single-electron transistors, quantum automata, molecular electronics, etc.) These are generally hyper-sensitive to dimensional change, if based on quantum-mechanical electron tunneling, and this is just one example of how appropriate packaging will be essential to the success or failure of these technologies. Packaging strategies must therefore be developed in parallel with the basic nanoelectronics device technologies in order to make informed decisions as to their commercial viabilities.

Another observation is that the work, at least as reported at ECTC, is highly concentrated in a few laboratories, especially so far at Georgia Tech. Other active organizations include:

- University of Arkansas
- Hong Kong University of Science & Technology
- National University of Singapore/Institute of Microelectronics
- Chalmers University of Technology/SMIT Center, Shanghai University
- Industrial Technology Research Institute, Taiwan
- Endicott Interconnect Technologies, Inc

New materials are emerging from small companies and university labs all the time, and with diverse applications beyond those discussed above.



The growth of the nanopackaging field is shown at left by the number of ECTC papers.
The top of each bar represents Georgia Tech papers, (including those with co-authors from elsewhere,) with all others below