

Conductive Adhesive Applications to Imprint Circuitry

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Abstract

This paper presents the application of isotropic conductive adhesive (ICA) interconnect to imprint surface mount circuit boards. The standard imprint board technology is reviewed, and the ICA modification is described. The research reported here is focused on the ICA properties, with the imprinted boards represented by milled test patterns in epoxy substrates. The electrical, mechanical and reliability properties of the ICA materials system are systematically characterized

Keywords: Imprinted circuits; conductive adhesive; ICA.

Introduction

The availability of conductive adhesives and imprint patterning technologies has opened up possibilities of new ways to manufacture circuit boards. The combination of the two technologies can eliminate many of the traditional processes of microelectronics manufacturing, including imaging, photoresist deposition and developing. Eventually, imprint board technology could replace the traditional Printed Wiring Board (PWB) because of its low-cost of manufacturing and “clean” processes. The complementary application of the conductive adhesive as both solder and interconnect replacement for flip-chip attachment and surface mount technology (SMT) further simplifies the manufacturing sequence.

Conductive adhesive technology [1] is finding increased applications in electronics packaging fields such as smart-card and surface mount applications etc. The potential advantages of low temperature processing, low-cost and superior

fine pitch reliability are attracting increased industrial attention.

Accompanying the conductive adhesive, the technology of imprint patterning has been developed [2-4]. Imprint patterning is a low-cost process to make a dimensional circuitry by stamping die on the board to form “U” shaped grooved traces. This process can produce fine pitch lines and spaces, leading to HDI (high density interconnect) circuitry with reduced process steps.

The current research objective is to develop and examine the application of ICA circuit board interconnect. The research is divided into three phases: the first phase is to apply conductive adhesive interconnect to single layer boards, and to establish the manufacturing technique with a flexible test pattern. The second phase is that materials system is systematically characterized for electrical, mechanical, and reliability properties. The third phase will extend those processes to microvias and the demonstration of a low-cost, multi-layer board system. The final phase will be dedicated to specific

studies indicated by earlier results. This paper presents the results from the research on the first two phases.

Imprint Patterning

Industrial researchers have developed imprint patterning to produce three-dimensional circuit boards, and have shown the technique to be one of the most efficient and low-cost ways to make PWBs [2]. Not only is this method reproducible, but it also has the ability of generating finer lines or spaces with precision.

Basically the imprint patterning can be done in the following steps:

1. Make a master by using an electroforming or electroplating process.
2. Press the master to the surface of the dielectric board, and leave an imprinted groove in the board (Figure 1(a)). In practice, the imprinted grooves are “U” shaped.
3. Cure the board.

The primary imprint technology for copper laminate is shown in Figure 1(b). The imprint process leaves depressed channels, which are then filled by squeegeed etch resist. Etching and resist removal leaves Cu-filled channels for interconnect.

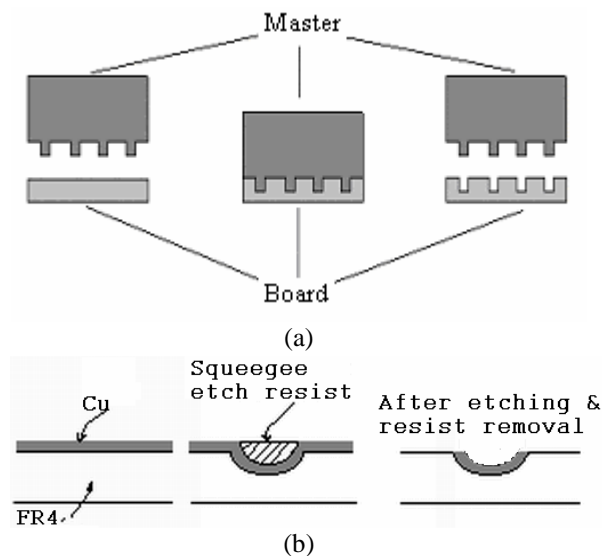


Figure 1. (a) Imprinting of channels. (b) Copper laminate imprint

The imprint patterning is quite simple, but it is hard to find a proper dielectric material to fit the specification at reasonable cost. Some researchers have suggested film-form epoxy “laminare” for the

board material [5]. The reliability and compatibility of such a material with the isotropic conductive adhesive are subjects for future investigation.

Squeegee Printing

The process of filling the groove of interconnection on the board can be done by the squeegee, as is shown in Figure 2.

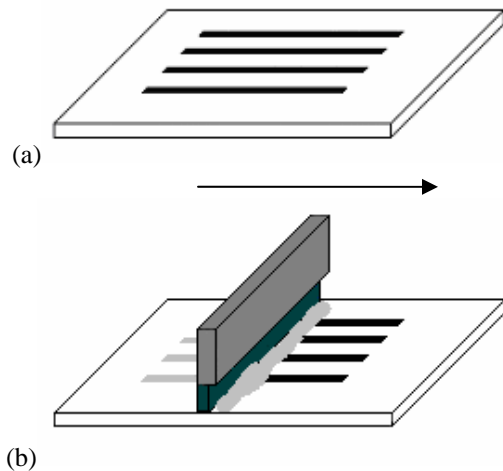


Figure 2. Squeegee printing (a) Board with channels (b) ICA filling

Normally, the squeegee is made of rubber. The one used in this project turned out to be not hard enough. It will squeeze down below the board surface and take the adhesive paste out of the channels. Squeegees made of harder materials are recommended, because they could be applied to higher pressure to remove more surface residue but would not go down below the surface in the channels. Observations of the channel surface are shown in Figure 3.

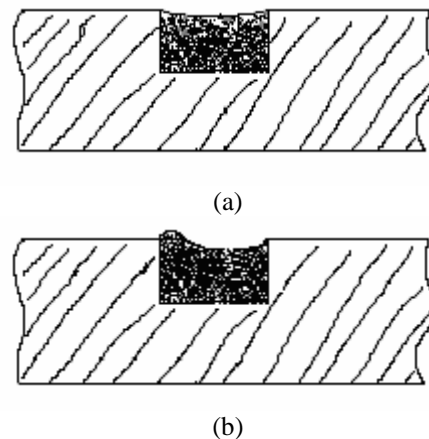


Figure 3. Observations of channel surface (a) with filling by the squeegee run along the channel (b) squeegee sweep across the channel

ICA Properties

ICAs are two-phase mixtures of epoxy and Ag. The ICA used for this research is ABLEBOND 8175, which is specially designed for solder replacement and interconnections, with the following basic properties:

Table 1 – Properties of ABLEBOND 8175

| Property | Values |
|--|---------------------------|
| Viscosity @ 25°C | 55,000 cps |
| Work Life @ 25°C | 2 weeks |
| Cure Condition | 1 hour @ 150°C |
| Cure Option | 1/2 hour @ 175°C |
| Volume Resistivity | 5×10^{-4} ohm-cm |
| Glass Transition Temperature (T_g) | 90°C |
| Coefficient of Thermal Expansion (TMA) | Below T_g 55ppm/°C |
| | Above T_g 200ppm/°C |
| Thermal Conductivity @ 121°C | 3.20W/mK |

This conductive adhesive has capability for fine pitch resolution at 500 μ m. Two major influences on ICA resistivity are the size effect and the layering effect. The size effect causes the ICA resistivity along the channel to increase at lower thickness, approaching the percolation coherence length. The layering effect decreases ICA resistivity due to the alignment of particles along the surface of channels during the processing of the squeegee print or by surface tension.

Manufacturing Technique

Combining the techniques of the imprint patterning, squeegee printing and surface mount, a manufacturing technique can be established. The flow of the manufacturing of the circuit board can be divided into five steps:

1. Imprint pattern to the board;
2. Fill the channels with the isotropic conductive adhesive by using squeegee;
3. Clean up the smudge left on the surface of the board by using materials like fine surface paper under pressure with a thin metal plate;
4. Mount the chips to surface of the board;
5. Cure the board with the chip under certain temperature and time as shown in Table 1.

The traditional methods of Cu clad circuit board manufacturing include such steps as production phototooling, photoresist, light source and

developing. Using ICA as alternative to Cu, the above process could be eliminated, while their products function similarly. A 3-D view of conventional Cu clad board and ICA filled board is shown in Figure 4.

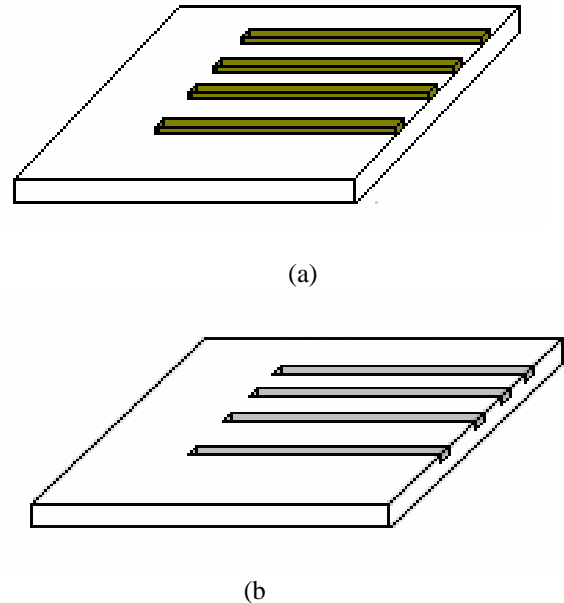
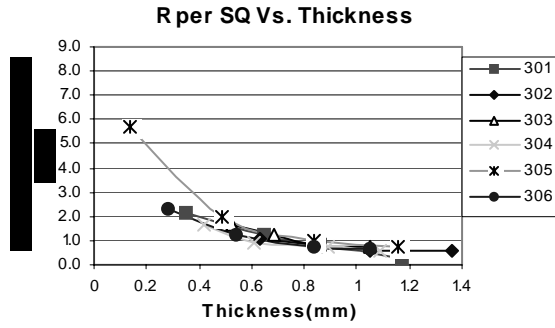


Figure 4. Comparison between (a) conventional Cu laminate and (b) ICA filled board.

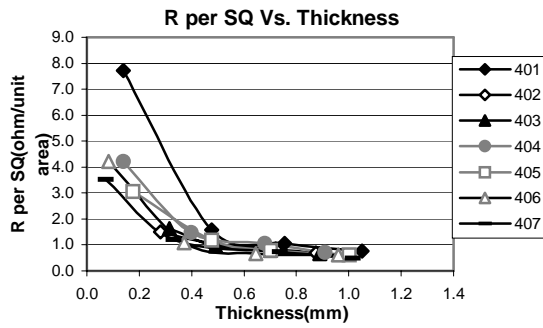
Electrical and Reliability Properties

To test the electrical properties, straight lines are milled in the board by using a milling machine instead of by the imprint patterning method, since suitable materials for the imprint patterning are still under development. The milling machine is controlled by NC code and it has no ability to detect the board surface and the board is mounted to the machine manually, which can cause the potential problem of the imprecision of the depth of the channels. Then conductive adhesive is applied to those milled channels. After they are cured, four terminal measurement methods are used to obtain the resistance, eliminating the contact resistance.

The data obtained from the measurements show the relationship between the resistance and thickness of the channels as can be seen from Figure 5, converted to resistivity in Figure 6.



(a)



(b)

Figure 5. Relationship between resistance per square area and thickness of channels (a) 0.75mm width channels (b) 1mm width channels

An alternative way to investigate the relationship between the resistivity and thickness of the channel is to use the plot of resistance per square vs. the thickness. From the resistance equation:

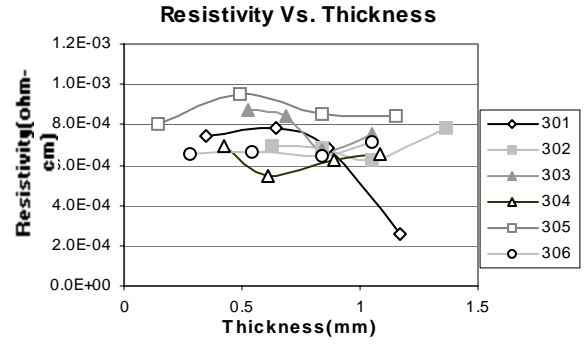
$$R = \rho \frac{l}{A} = \rho \frac{l}{wt}$$

Where ρ is resistivity, l is length of channel, w is width of channel and t is thickness of channel. A channel with length l and width w has l/w squares; consequently, the equation reduces to:

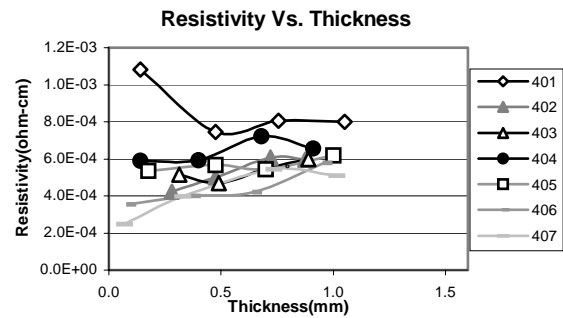
$$\frac{R}{SQ} = \frac{\rho}{t}$$

Where SQ is square.

As can be seen from Figure 5, when the thickness of channels increases, the scatter points tend to converge. This result reflects the greater influence of structural fluctuations with printing non-uniformities on the thinner channels



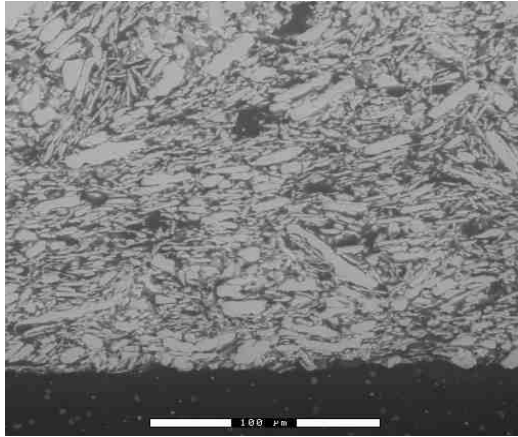
(a)



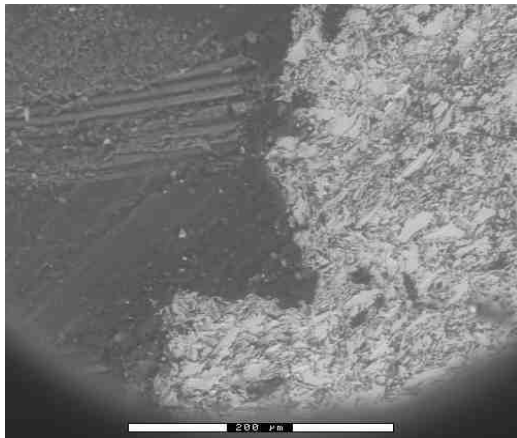
(b)

Figure 6. Relationship between resistivity and thickness of channels (a) 0.75mm width channels (b) 1mm width channels

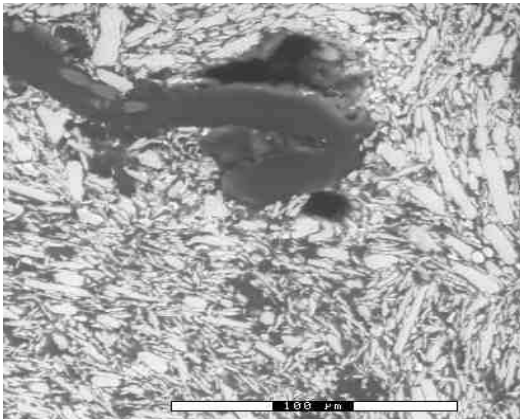
The electricity is mainly conducted by aligned flakes in the surface part of the channel (Figure 7(a)), which seems to dominate the size effect in most samples. This should lead to the resistivity of the channel increasing with the thickness, eventually reaching a constant value. The results show considerable scatter in the resistivity at low channel thickness. Investigation has shown that the apparent scatter is due to a lack of precision in the milling machine that mills the channels in the board. It did not produce the precise channel as desired as shown in (Figure 7(b)) (left edge of channel). In addition, there is air included in the channel during the squeegee print process, which also contributes to error in the effective thickness of channels. It has more effect on the thinner channels than the thicker ones. The air in the channel is shown in (Figure 7(c)). These printing artifacts should be removable by print parameter optimization, specifically in control of paste viscosity.



(a)



(b)



(c)

Figure 7. Scanning electron micrographs of ICA in Channels (a) Surface alignment. (b) Rough edge of channel. (c) Air in channel.

To test the mechanical reliability of the component attachment, 60-inch drop tests were conducted at room temperature, following the NCMS standard. It was expected that physical positioning of the pin below the board surface, with the ICA squeezed up alongside, would provide good impact resistance, but the results were disappointing. The 6 small chips (74F299 13mm x 7.5mm x 2.6mm, 20 pins, JEDEC MS-013) were mounted with the board and the pins 0.1-0.3 mm below the board surface. They failed after 1 to 4 drops. The large one (PLCC 68 – DC 24.1mm x 24.1mm x 4.5mm, 68 pins, JEDEC MO-47) with pins 0.25mm below the surface failed after 5 to 7 drops. The difference is a reversal of the expected trend. The cleanliness of the chip pins is a possible reason. The adhesive bonding of the conductive adhesive requires a short-range distance of about a few angstroms for the electronic interactions, so the surface cleanliness of the adherent is critical to the strength of adhesion. The big chips have more pins to contact with ICA. They increase the contact area of the adherent as well as the adhesive strength. Basic research has identified the drop test problem to lie with the low epoxy loss modulus and not with lack of adhesive strength [6]

Future Work

The project will be extended to the use of imprint patterning instead of milling the channels so that the accuracy of depth of the channel can be improved. Second, the materials for imprint patterning need to be examined. Third, the squeegee print process can be improved with a harder squeegee to make a more reliable channel without air being captured in the channel. Fourth, the effect of the coefficient of the thermal expansion is to be tested in thermo-mechanical cycling. And finally, frequency response of the circuit is to be investigated. The interconnect resistance will clearly be higher than for copper, and RC high frequency performance may dominate transmission time delay.

Conclusion

With the technology of imprint patterning and conductive adhesive, a flow manufacturing process has been established. The electrical and mechanical reliability has been investigated. The electrical resistivity is influenced by size effect and layering effect. The mechanical reliability has failed drop test due to the cleanliness of the adherent surface, large size of the adhesive flake and low epoxy loss modulus.

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Biography



James E. Morris is an IEEE Fellow, and has recently joined Portland State University as Professor and Chair of Electrical & Computer Engineering. His B.Sc. and M.Sc. (with 1st Class Honors in Physics) degrees are from the University of Auckland, New Zealand,

and the Ph.D. in Electrical Engineering is from the University of Saskatchewan, Canada. Professor Morris is IEEE-CPMT Vice-President for Conferences and an IEEE-CPMT Distinguished Lecturer. He is an Associate-Editor of the IEEE Transactions on Components and Packaging Technology, and has edited three books on electronics packaging. He was General Chair of the Adhesives in Electronics conference in 1998, and of the 2001 International Symposium & Exhibition on Advanced Packaging Materials. His research activities are currently focussed on the electrical conduction mechanisms in discontinuous thin metal films, with application to single-electron transistor nanoelectronics, and in electrically conductive adhesives.



Liye Fang is currently studying towards his Bachelor's Degree in Electrical Engineering in the T. J. Watson School of Engineering and Applied Science of the State University of New York at Binghamton. He was granted an undergraduate research fellowship from the International Microelectronics and Packaging Society (IMAPS) to work on the subject of isotropic conductive adhesive circuit board interconnect, as reported in the paper.