Nanopackaging: Nanotechnologies and Electronics Packaging

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Abstract

Nanotechnologies are being applied to microelectronics packaging, primarily in the applications of nanoparticle nanocomposites, or in the exploitation of the superior mechanical, electrical, or thermal properties of carbon nanotubes. Composite materials are studied for high-k dielectrics, electrically conductive adhesives, conductive "inks," underfill fillers, and solder enhancement. These trends are demonstrated by paper presentations over the past few years at ECTC and other conferences, which show research to be concentrated in relatively few laboratories, with little work being done on the packaging requirements of the new nanoelectronics technologies. Future needs (predictably) include education and software development.

Introduction

It may seem that the media hype surrounding the term "nanotechnology" is all too reminiscent of the past promises of cold fusion and high-temperature superconductivity, but nanotechnologies have already yielded everyday consumer benefits beyond stain-resistant clothing and transparent sun-block. So it would not be surprising to discover active research programs in nanotechnology applications to electronics packaging, and amongst the traditional electronics packaging conferences, this trend is most evident in the papers presented at the annual *Electronics Component & Technology Conference* (ECTC,) the IEEE's flagship event in packaging. The proceedings of recent and forthcoming ECTC events [1-3], and of two more IEEE Components, Packaging, and Manufacturing Technology Society conferences, (i.e. the 5th *International IEEE Conference on Polymers & Adhesives in Microelectronics & Photonics* (Polytronic 2005) [4] and the 10th *International IEEE Symposium & Exhibition on Advanced Packaging Materials* (APM'05) [5],) demonstrate the range and progress of this research.

The definition of nanotechnology is usually taken to be where the size of the functional element falls below 100nm or 0.1μm. Of course, according to this definition, and with 90nm CMOS in production, the nanoelectronics era is already here. Furthermore, with metallic grain sizes typically below this limit, one might also argue that solder has always qualified as a nanotechnology, along with many thin film applications. So, the requirement that the specific function depend upon this nanoscale dimension is conventionally added to the definition. According to this *caveat*, MOSFET technology, for example, would not qualify by simple device shrink, but would at dimensions permitting ballistic charge transport.

Nanotechnology drivers are the varied ways in which materials properties change at low dimensions. Electron transport mechanisms at small dimensions include ballistic transport, severe mean free path restrictions in very small nanoparticles, various forms of electron tunneling, electron hopping mechanisms, and more. Other physical property changes include:

- Melting point depression, i.e. the reduction of metal nanoparticle melting points at small sizes [1], although this is unlikely to be a factor in packaging applications with even 10% reductions typically requiring dimensions under 5nm [2]
- Sintering by surface self-diffusion, which is thermally activated, with net diffusion away from convex surfaces of high curvature [3]
- The Coulomb blockade effect, which requires an external field or thermal source of electrostatic energy to charge an individual nanoparticle, and is the basis of single-electron transistor operation [4]
- Theoretical maximum mechanical strengths in single grain material structures [5]
- Unique optical scattering properties by nanoparticles one to two orders smaller than the wavelength of visible light [6]
- The enhanced chemical activities of nanoparticles, which make them effective as

catalysts, and other effects of the high surface-to-volume ratio

Computer modeling

The use of composite materials is well established for many applications. But while overall effective macroscopic properties are satisfactory for computer modeling of automotive body parts, for example, they are clearly inadequate for structures of dimensions similar to the particulate sizes in the composite. The modeling of such microelectronics (or nanoelectronics) packages must include two-phase models of the composite structure, and this general principle of inclusion of the nanoscale structural detail in expanded material models must be extended to all aspects of package modeling [7]. The extended computer models can be based on either the known properties of the constituent materials, (and hopefully known at appropriate dimensions,) or the measured nanoscale properties (e.g. by a nano-indenter [8, 9] or atomic-force microscope (AFM) [10].)

Nanoparticles: Fabrication

Noble metal nanoparticles have been fabricated by an ultrasonic processing technique [11], and Ag/Cu with "polyol" [12]. Alternatively, a pre-cursor may be used, e.g. $AgNO_3$ for Ag nanoparticles, and there are techniques to control the particle shapes, e.g. spherical, cubic, or wires [14].

Nanoparticles: High-*k* dielectrics

The move towards embedded passive components at both on-chip and PWB levels has prompted a search for high dielectric constant materials for low area capacitors. High dielectric constants can be achieved by the inclusion of high dielectric constant particulates and minimal thickness. The latter requirement pushes one towards nanoscale particulates, with examples of the former covering ceramic [15-17], silicon [18], and metal [19-23]. The ceramic particles are generally barium titanate, e.g. applied to organic FETs with composite k around 35 [16]; in such materials the particle surface energy must be reduced to avoid aggregation [17].

The target k is 50-200, and while k~150 has been achieved, it is at the expense of high leakage (dielectric loss.) Similar structures have been studied in the past as "cermets," (ceramic-metal composites,) for high resistivity materials for on-chip resistors [24], which conduct by electron tunneling between particles. At low fields, the nanoparticles can act as Coulomb blocks to minimize DC leakage if they are sufficiently small [20], but still do not eliminate it at finite temperature [25]. It is the AC performance which is more important, however, and inter-particle capacitance will bypass the block unless pseudo-inductive effects develop at capacitor thicknesses which permit even short nanoparticle chains [26].

An alternative approach to leakage is to use aluminum particles, to take advantage of the native oxide coating [21], with k~160 achieved [22]. Ag/Al mixtures have also been studied [23].

Nanoparticles: Electrically conductive adhesives

The addition of smaller μm diameter silver powder to 10μm silver flakes in isotropic conductive adhesives reduces resistance by inserting bridging particles between the flakes. The simple addition of nanoparticles does not improve conductance, due to mean free path restrictions and added interface resistances, and the same principles limit the performance of alumina loaded thermal composites [27]. The addition of silver nanoparticles does achieve dramatic reductions, however, by sintering wide area contacts between flakes [28], a principle also applicable to via fill [29]. Filler nanoparticle sintering can also improve anisotropic conductive adhesive performance [13], aided by contact conductance enhancement by the addition of self-assembly molecular surface treatments [28, 30, 31]. Sintering effects have also been shown to improve contacts in materials with sufficiently low filler content as to be regarded as non-conductive adhesives [32].

Nanoparticles: Interconnect

Surface electrical interconnect for board and package levels can be achieved by screen-printing nanoscale metal colloids in suspension [33], and there has been recent effort to achieve the same effect by ink-jet printing [34, 35]. Electrical continuity is established by sintering, e.g. of 5-10nm silver particles [36]. As a variation, magnetic composite films, (e.g. of Co/SiO_2 in BCB and Ni/ferrite in epoxy,) have been screen-printed for antennas [37]. Sn/Ni bumps have also been grown on Sn from a nm Ni slurry [38].

Nanoparticles: Silica filler in underfill

The key advantage of nanoscale silica particles in underfill formulations is that they resist settling [39]. They also scatter light less, permitting UV optical curing, and providing a dual photoresist function from a single material [40], and other advantages of optical transparency [41]. The higher viscosity of the nano-filled material can be reduced by silane surface treatments [42].

Nanoparticles: Solder

The addition of Pt, Ni, or Co nanoparticles to no-Pb S-Ag-based solders eliminates Kirkendall voids, reduces intermetallic compound (IMC) growth, and reduces IMC grain sizes, significantly improving drop test performance [43]. Similarly, Ni or Mo nanoparticles promote finer grain growth, increased creep resistance, and better contact wetting [44]. Nanoparticles in the grain boundaries also inhibit grain boundary sliding and thermomechanical fatigue, but a similar function can be provided by 1.5nm $SiO_{1.5}$ polyhedral oligomeric silsesquioxane structures with surface-active Si-OH groups [45].

Carbon Nanotubes: Solder

The addition of carbon nanotubes (CNTs) to solder can also have beneficial effects, e.g. 30-50% improvements in tensile strength [46].

Carbon Nanotubes: Thermal

The high thermal conductivity of CNTs is being exploited for microelectronics chip cooling both directly in conductive cooling and indirectly in convective cooling systems. For conductive systems, the key is to establish CNT alignment [46], since the thermal conductivities of random arrays (of CNTs and carbon fibers alike) fall far short of expectation, showing no advantages over conventional materials, often also because of CNT fracture at the substrate [47]. In one of the most advanced techniques, vertical CNTs are first grown on both the aluminum heat sink and silicon chip surfaces, which are then positioned ~μm apart in a CVD furnace, enabling the CNTs from the two surfaces to grow further and connect with each other [46]. Composites incorporating CNTs have also been studied for thermal interface materials, e.g. CNT/carbon-black mixtures in epoxy resin [48]. The use of a liquid crystal resin matrix can impose structural order on the CNT alignment to yield a seven-fold improvement in thermal conductivity [49].

So far, convective CNT cooling has been limited to the use of μm-scale clusters of vertically grown nanotubes [50, 51]. These clusters define micro-channels for coolant flow which look very much like the metal or silicon structures they aim to replace, (Figure 1), with similar thermal performances. The problem is that the flowing coolant is only in contact with the outermost CNTs of the clusters, and the internal CNTs are not even in good contact with each other. The system has been modeled [51], and the solution is clearly to spread the CNTs apart by an optimal separation to permit coolant contact with each one [50]. The problem then is whether individual CNTs can withstand the coolant pressure without detaching from the substrate.

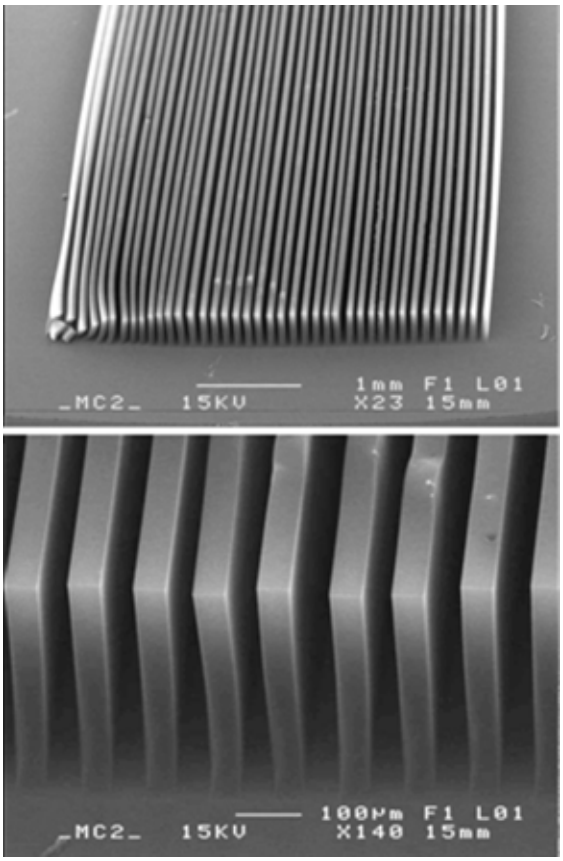


Figure 1. CNT clusters as microelectronics cooling fins; individual CNTs are typically 50nm (1nm to 100nm) in diameter, about 200nm apart. [50] (With permission.)

Carbon Nanotubes: Electrical

An important development has been the ability to open CNTs after growth [52], since the open ends permit better wetting by Sn/Pb, (and presumably other metals,) for improved electrical contact. Au and Ag incorporation into CNTs and fullerenes has also been studied for electrical contacts with minimal galvanic corrosion [53]. Metal and carbon loaded polymers have long been used for high-frequency conductors in electromagnetic shielding, and multi-walled CNTs have been studied in polymer matrices for the purpose [54], but CNT replacement of metal filler in isotropic conductive adhesives does not even match the electrical conductivity of standard materials [55]. However, 10-50μm long Ag/Co nanowires of 200nm diameter can be maintained in a parallel vertical orientation by a magnetic field while polymer resin flows around them [56], to form an anisotropic conductive film for z-axis contacts.

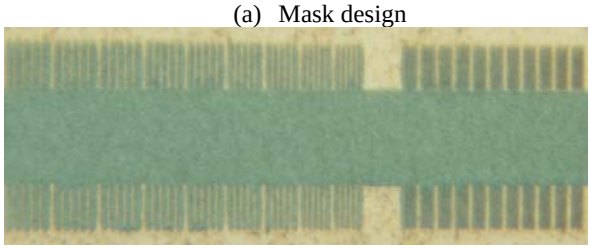
Carbon Nanotubes: Fabrication

CNT growth can be accomplished for both electrical and thermal applications by chemical vapor deposition [57], with satisfactory solder wetting of the CNTs for electrical contacts.

Nanoscale Structures

The incorporation of nano- diamond particles into an electroless Ni film coating on an electro-thermal actuator [58] can improve cantilever performance by changing the thermal and mechanical properties. In a truly impressive development, the micro-spring contacts originally developed at PARC-Xerox have been down-sized to 10nm wide cantilevers, still 10μm long, for biological sensing [59] (Figure 2.) Nano-imprinting technology is also being used to fabricate optical interconnect waveguides in organic PCBs [60].

(a) Mask design



(b) e-beam evaporated cantilevers

Figure 2. Nanoscale cantilevers have been made for interconnect and bio-sensor applications, with widths down to 10nm. (a) Mask design; (b) e-beam evaporated cantilevers. [59] (With permission.)

"Nano-interconnects"

The "nano-interconnect" terminology is applied to interconnect structures which are clearly μm-scaled [61-68]. The ITRS Roadmap calls for 20-100μm pitch interconnects for nanoelectronics systems of feature size under 100nm [64], which has prompted studies of nano-grain solders [61] or copper [63], nanocrystalline copper and nickel [64], and nano-scale via fillers [62], all for applications at around 30-35μm pitch [61, 63]. Some nano-interconnect options are reviewed in reference [66]. Other technologies can be included in this group, too, e.g. metal-coated polymer posts on a similar scale [65], and embedded micro- or nano-electrodes for biological flow sensing [67]. Control of the interfacial surface charge on the nano-electrode in contact with the fluid can be used to control the flow [68].

Conclusion

The importance of nanoelectronics and "electro-nanotechnologies" in the future is sufficiently well recognized to have become the subject of industrial and government policy roadmaps [69]. Similarly, the academic world is responding with graduate level courses, (although with few textbooks so far.) As for electronics packaging, the field requires students to be "subject multilingual" [70].

One of the surprising observations to come out of this survey, in full agreement with prior comment [71], has been that there is almost no work reported on the development of packaging for future nanoelectronics technologies. The "nano-interconnect" work [61-66] is directed towards continued Moore's Law shrinkage of silicon, but only one paper specifically addresses the impact of the package on the device [72], specifically of organic flip-chip packaging of 110nm CMOS. Candidate next-generation nanoelectronics technologies, (e.g. single-electron transistors, quantum automata, molecular electronics, etc.,) are generally hyper-sensitive to dimensional change, if based on quantum-mechanical electron tunneling, and this is just one example of how appropriate packaging will be essential to the success or failure of these technologies. Packaging strategies must therefore be developed in parallel with the basic nanoelectronics device technologies in order to make informed decisions as to their commercial viabilities.

Another observation is that the work, at least as reported at ECTC, is highly concentrated in a few laboratories. This is reflected in Figure 3, where the number of nanotechnology papers presented at ECTC is tracked, with those originating at Georgia Tech highlighted. Other organizations with participation in more than one nanopackaging paper in the conferences referenced include:

- University of Arkansas
- Hong Kong University of Science & Technology
- National University of Singapore/Institute of Microelectronics
- Chalmers University of Technology/SMIT Center, Shanghai University
- Industrial Technology Research Institute, Taiwan
- Endicott Interconnect Technologies, Inc

New materials are emerging from small companies and university labs all the time, and with

diverse applications beyond those discussed above [73].

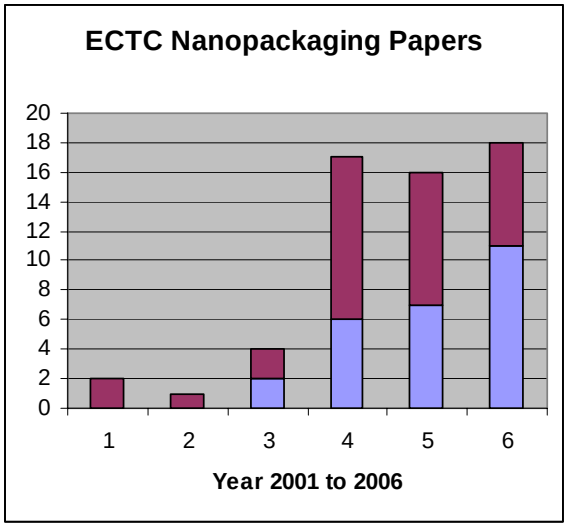


Figure 3.The growth of the nanopackaging field is shown by the number of ECTC papers. The (red) top of each bar represents Georgia Tech papers, (including those with co-authors from elsewhere,) with all others below (in blue.)

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