EE415/515 Fundamentals of Semiconductor Devices Fall 2012

Lecture 15:
Power Devices
(Chapter 15.4-15.6)

Vertical power BJT

Compare small signal BJTs before

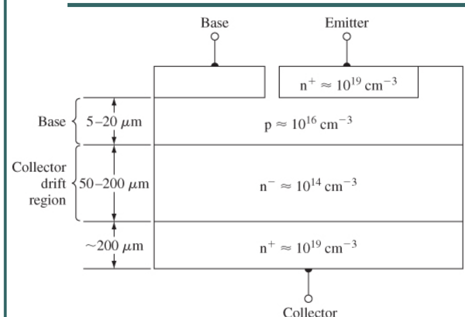


Figure 15.10 | Cross section of typical vertical npn power BJT.

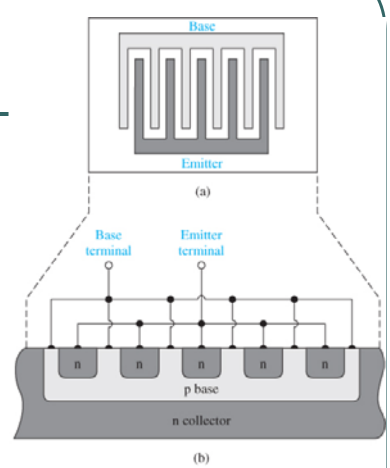


Figure 15.11 | An interdigitated bipolar transistor structure showing the top view and cross-sectional view.

Vertical structure maximizes junction areas
Small N_C (n^-) permits large V_{CB} before avalanche; n^+ for min contact R
Large BW (reduced gain) permits large V_{CB} before punch-through
Interdigitated emitter minimizes emitter crowding

Power BJT characteristics vs small signal

Table 15.1 | Comparison of the characteristics and maximum ratings of small-signal and power BJTs

Parameter	Small-signal BJT (2N2222A)	Power BJT (2N3055)	Power BJT (2N6078)
V_{CE} (max) (V)	40	60	250
T_C (max) (A)	0.8	15	7
P_D (max) (W) (at $T = 25°C$)	1.2	115	45
β	35–100	5–20	12–70
f_T (MHz)	300	0.8	1

Large base width (punch-through) decreases β
Large area reduces f_T
I_c(max) due to connecting wires, I_C for β_{min}, or max power in saturation
V_{CE}(max) usually due to avalanche

Power BJT characteristics

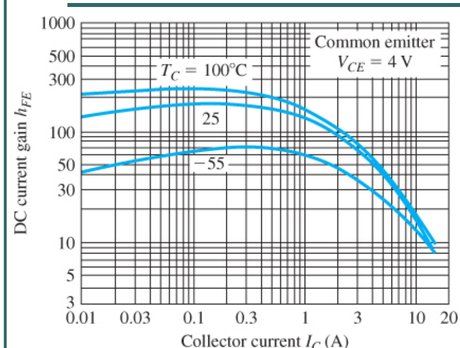


Figure 15.12 | Typical dc beta characteristics (h_{FE} versus I_C) for 2N3055.

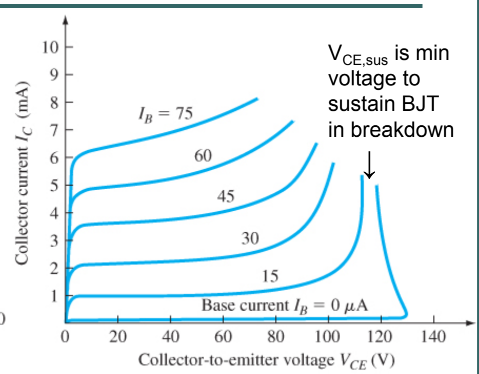


Figure 15.13 | Typical collector current versus collector–emitter voltage characteristics of a bipolar transistor, showing breakdown effects.

Safe operating area (SOA)

$P_T = V_{CE} I_C$ neglects $V_{BE} I_B$

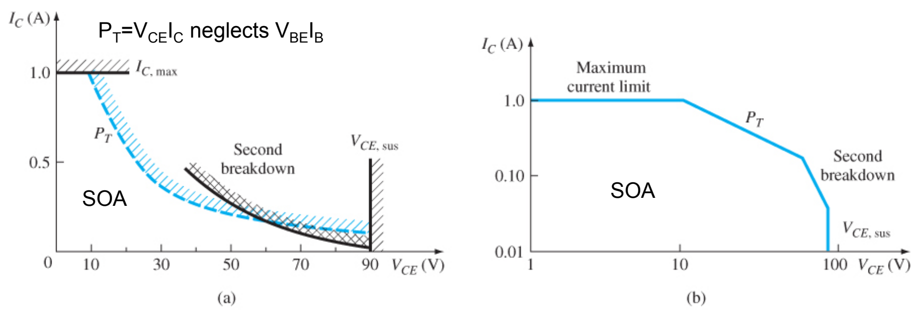


Figure 15.14 | The safe operating area (SOA) of a bipolar transistor plotted on (a) linear scales and (b) logarithmic scales.

Secondary breakdown:
local irregularities → local hot spots → incr local minority carriers → incr local gain → positive feedback → thermal runaway

Ex 15.1 Assume BJT in Fig 15.15 has $I_{C,max}$=5A, $V_{CE,max}$=75V & P_T=30W. Find minimum R_L for Q-point within the SOA for V_{CC} (a) 60V, (b) 40V, & (c) 20V, and find max I_C, V_{CE} for each case. Neglect second breakdown.

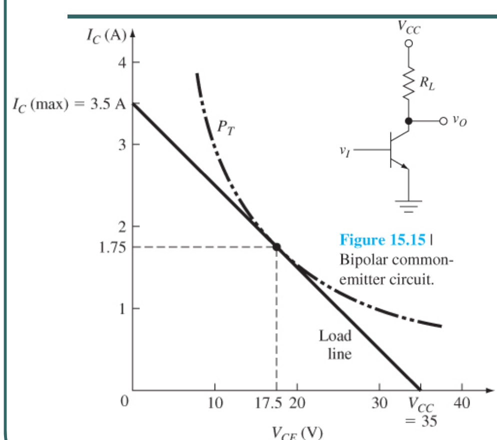


Figure 15.15 | Bipolar common-emitter circuit.

Figure 15.16 | Load line and maximum power curve for Example 15.1.

(a) $V_{CEQ} = \frac{V_{CC}}{2} = 30\,\text{V}$

$P_T = I_{CQ} \cdot V_{CEQ}$

$30 = I_{CQ}(30) \Rightarrow I_{CQ} = 1\,\text{A}$

$I_C(\max) = 2I_{CQ} = 2\,\text{A}$

$R_L = \frac{V_{CC}}{I_C(\max)} = \frac{60}{2} = 30\,\Omega$

(b) $V_{CEQ} = \frac{V_{CC}}{2} = 20\,\text{V}$

$P_T = I_{CQ} \cdot V_{CEQ}$

$30 = I_{CQ}(20) \Rightarrow I_{CQ} = 1.5\,\text{A}$

$I_C(\max) = 2I_{CQ} = 3\,\text{A}$

$R_L = \frac{V_{CC}}{I_C(\max)} = \frac{40}{3} = 13.3\,\Omega$

(c) $V_{CEQ} = \frac{V_{CC}}{2} = 10\,\text{V}$

$P(\max) = \left(\frac{1}{2} \cdot I_{C,\max}\right) \cdot V_{CEQ} = \left(\frac{5}{2}\right)(10)$

$= 25\,\text{W}$

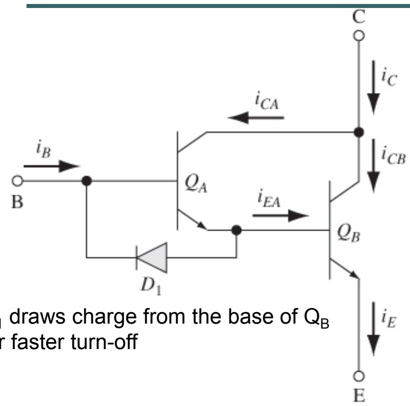
$I_C(\max) = 5\,\text{A}$

$R_L = \frac{V_{CC}}{I_C(\max)} = \frac{20}{5} = 4\,\Omega$

Darlington pair

$i_C = i_{CA} + i_{CB}$
$= \beta_A i_B + \beta_B i_{EA}$
$= \beta_A i_B + \beta_B (1+\beta_A) i_B$

So $\beta = i_C/i_B = \beta_A \beta_B + \beta_A + \beta_B$



D_1 draws charge from the base of Q_B for faster turn-off

Figure 15.17 | An npn Darlington pair configuration.

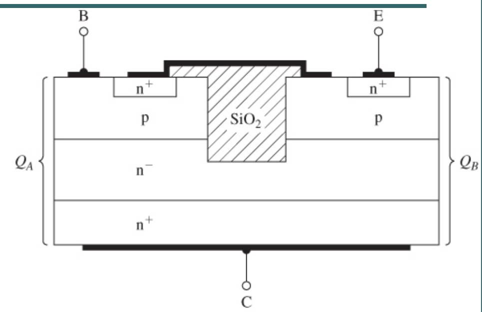


Figure 15.18 | An integrated circuit implementation of the npn Darlington pair configuration.

Power MOSFET structures

Small gate currents control large I_D

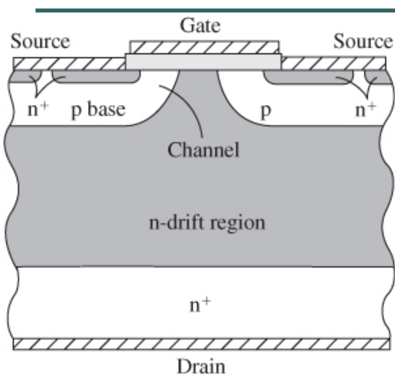


Figure 15.20 | Cross section of a double-diffused MOS (DMOS) transistor.

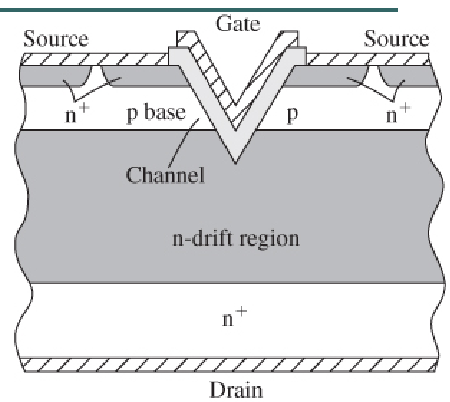


Figure 15.21 | Cross section of a vertical channel MOS (VMOS) transistor.

Parallel DMOS cell structure

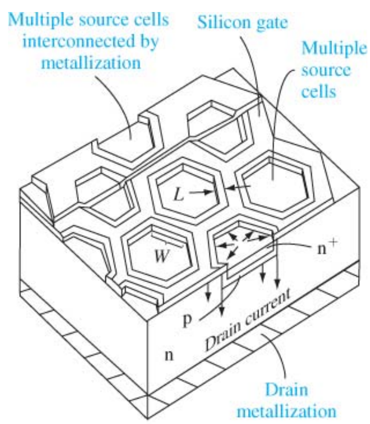
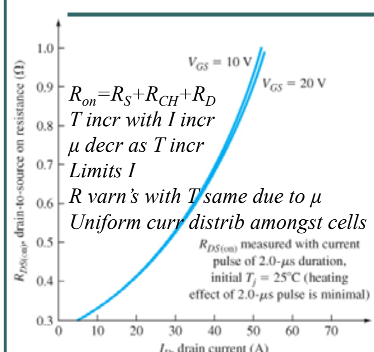


Figure 15.22 | A HEXFET structure.

Power MOSFET characteristics

Table 15.2 | Characteristics of two power MOSFETs

Parameter	2N6757	2N6792
V_{DS}(max) (V)	150	400
I_D(max) (at T = 25°C)	8	2
P_D(W)	75	20



$R_{on}=R_S+R_{CH}+R_D$
T incr with I incr
μ decr as T incr
Limits I
R varn's with T same due to μ
Uniform curr distrib amongst cells

Figure 15.23 | Typical drain-to-source resistance versus drain current characteristics of a MOSFET.

$$R_{CH}=\frac{L}{W\mu_n C_{ox}\left(V_{GS}-V_T\right)}$$

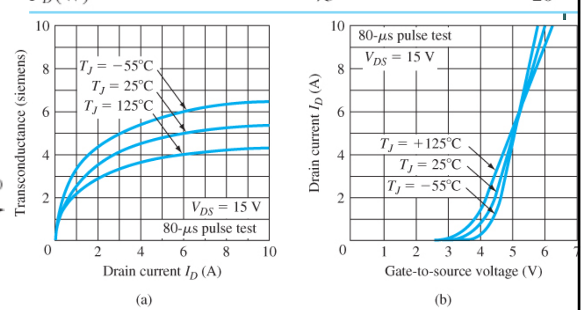


Figure 15.24 | Typical characteristics for high-power MOSFETs at various temperatures: (a) transconductance versus drain current; (b) drain current versus gate-to-source voltage.

Note I_D decr with T incr at high V_{GS}

Power MOSFET SOA

Compare BJT:
No secondary breakdown
Faster switching
Stable gain wrt T

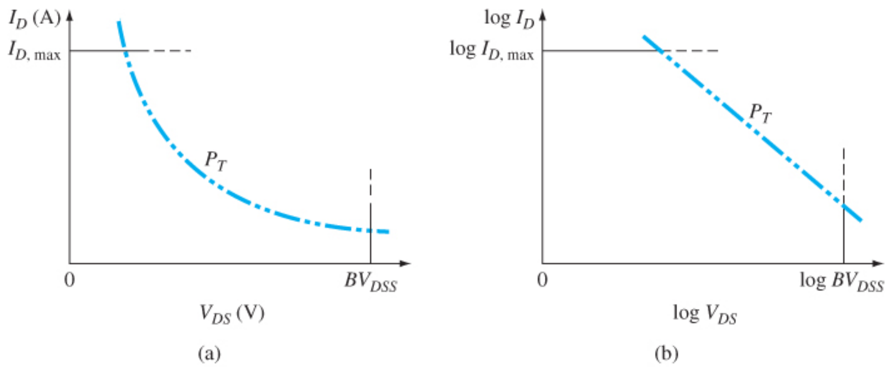


Figure 15.25 | The safe operating area (SOA) of a MOSFET plotted on (a) linear scales and (b) logarithmic scales.

Ex 15.2 For common-source circuit in Fig 15.26, determine required current, voltage, and power ratings of the MOSFET for (a) R_D=12Ω, V_{DD}=24V, & (b) R_D=8Ω, V_{DD}=40V.

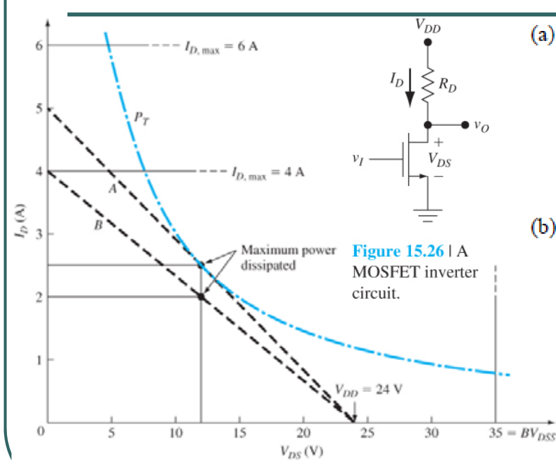


Figure 15.26 | A MOSFET inverter circuit.

(a) $BV_{DSS} = V_{DD} = 24\text{ V}$

$$I_{D,\max} = \frac{V_{DD}}{R_L} = \frac{24}{12} = 2\text{ A}$$

$$P_T = \left(\frac{1}{2}\cdot I_{D,\max}\right)\left(\frac{1}{2}\cdot V_{DD}\right) = \left(\frac{2}{2}\right)\left(\frac{24}{2}\right)$$

$$= 12\text{ W}$$

(b) $BV_{DSS} = V_{DD} = 40\text{ V}$

$$I_{D,\max} = \frac{V_{DD}}{R_L} = \frac{40}{8} = 5\text{ A}$$

$$P_T = \left(\frac{1}{2}\cdot I_{D,\max}\right)\left(\frac{1}{2}\cdot V_{DD}\right) = \left(\frac{5}{2}\right)\left(\frac{40}{2}\right)$$

$$= 50\text{ W}$$

Figure 15.27 | Safe operating area and load lines for devices in Example 15.2.

Parasitic BJT in the MOSFET

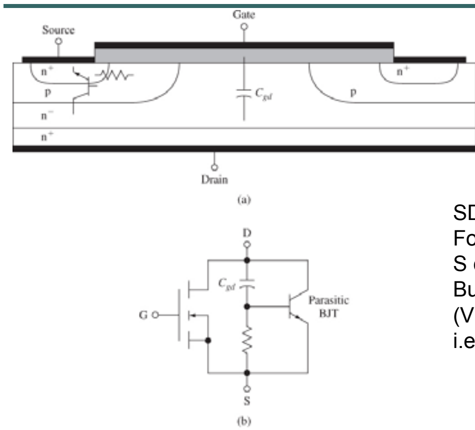


Figure 15.28 | (a) Cross section of vertical MOSFET showing parasitic BJT and distributed resistance; (b) equivalent circuit of MOSFET and parasitic BJT with distributed parameters.

SD channel width = BJT base width
For BJT cut-off, need V_{BE}=$V_{CH\text{-}S}$~0
S contact straddles channel, so OK
But turn-on possible by OFF transient
(V_{DS} incr, i_{Cgd} in R may turn on BE, i.e. "snapback" breakdown)

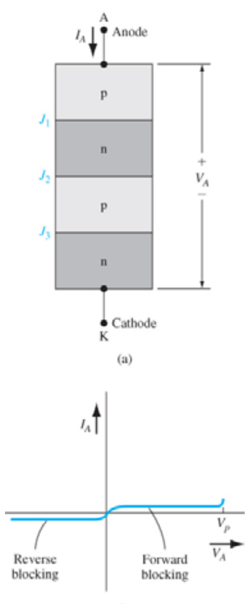


Figure 15.29 | (a) The basic four-layer pnpn structure. (b) The initial current–voltage characteristic of the pnpn device.

Thyristors:
(PNPN 4-layer devices)
Shockley diode

OFF states:

Forward blocking: J_1 fwd biased
J_2 rev biased
J_3 fwd biased
i.e. two forward, one reverse

Reverse blocking:
J_1 rev biased
J_2 fwd biased
J_3 rev biased
i.e. one forward, two reverse

Hence I_A is the diode reverse saturation current

Forward blocking ⟶ forward conducting when J_2 avalanches
⟶ forward conducting at V_P

4-layer (PNPN) devices
(Shockley diode)

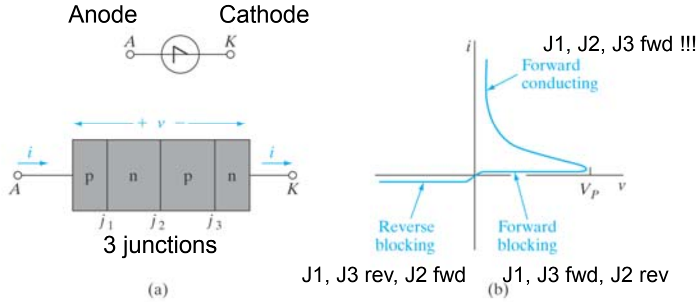


Figure 10.10

A two-terminal p-n-p-n device: (a) basic structure and common circuit symbol; (b) I–V characteristic.

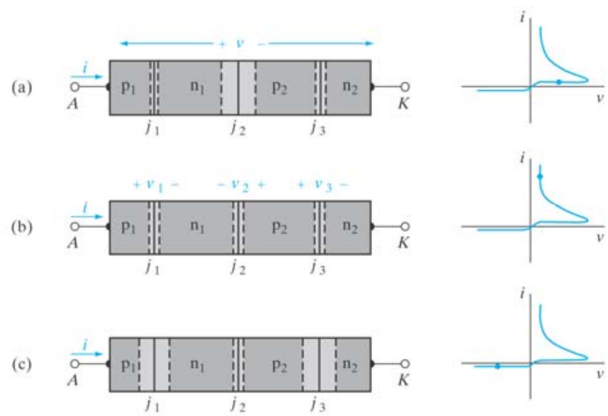


Figure 10.12

Three bias states of the p-n-p-n diode: (a) the forward-blocking state; (b) the forward-conducting state; (c) the reverse-blocking state.

2-BJT model

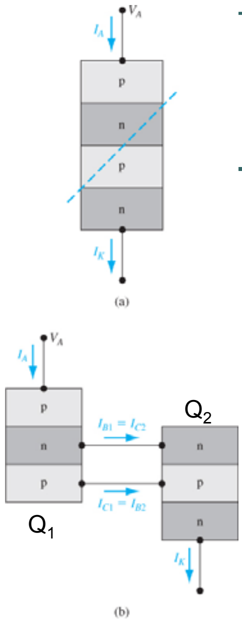


Figure 15.30 | (a) The splitting of the basic pnpn structure. (b) Two two-transistor equivalent circuit of the four-layer pnpn device.

$I_{C1} = \alpha_1 I_A + I_{C01} = I_{B2}$
$I_{C2} = \alpha_2 I_K + I_{C02} = I_{B1}$

$I_A = I_K = I_{C1} + I_{C2} = (\alpha_1 + \alpha_2) I_A + I_{C01} + I_{C02}$

so $$I_A = \frac{I_{C01} + I_{C02}}{1 - (\alpha_1 + \alpha_2)}$$

Current gains α_1 & α_2 increase with I_C, so increase I_C, e.g. by avalanche at V_P, so

$(\alpha_1 + \alpha_2) \rightarrow 1$

and $I_A \rightarrow \infty$

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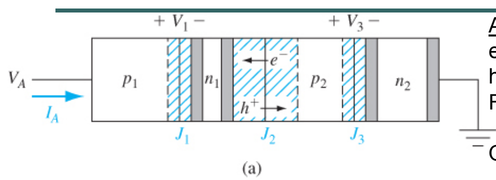
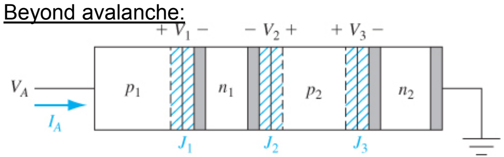
J_2 at avalanche and beyond



At avalanche:
e⁻s flood into n_1 (I_{B1} in Q_1 base, Q_2 collector)
h⁺s flood into p_2 (I_{B2} in Q_2 base, Q_1 collector)
Fwd B-E voltages V_1, V_3 increase
→ I_A increases → α's increase
Q's driven into saturation

Beyond avalanche:



V_2 (V_{CB}) forward biased,
$V_A \rightarrow V_D$ (one forward diode voltage drop)

Figure 15.31 | (a) The pnpn device when the J_2 junction starts into avalanche breakdown. (b) The junction voltages in the pnpn structure when the device is in the high-current, low-impedance state.

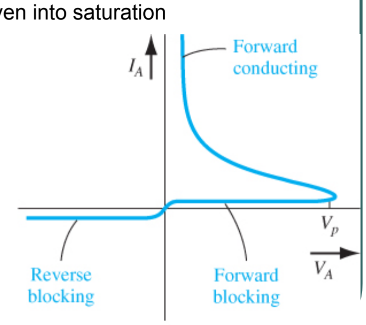


Figure 15.32 | The current–voltage characteristics of the pnpn device.

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PNPN analysis (2-transistor model)

$$i_{C1} = \alpha_1 i + I_{CO1} = i_{B2}$$
$$i_{C2} = \alpha_2 i + I_{CO2} = i_{B1}$$
and $i = i_{C1} + i_{C2}$
$$= \alpha_1 i + \alpha_2 i + I_{CO1} + I_{CO2}$$
$$= \frac{I_{CO1} + I_{CO2}}{1 - (\alpha_1 + \alpha_2)}$$
So $i \rightarrow \infty$ as $\alpha_1 + \alpha_2 \rightarrow 1$

Forward blocking:
J_1, J_3 (both BE junctions) fwd bias
J_2 (CB) rev bias (active normal mode)
but i_B's=i_C's, so α's small
Increase V ($V_{BC1}=V_{CB2}$), current incr, injection γ incr, so α's incr → regenerative action, and then i_B's=i_C's forces Q's into saturation
i.e. J_2 fwd bias, and $V=2V_\gamma - V_\gamma = V_\gamma$

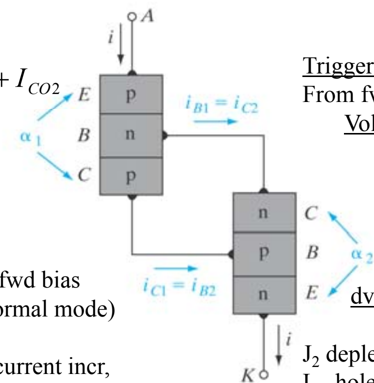
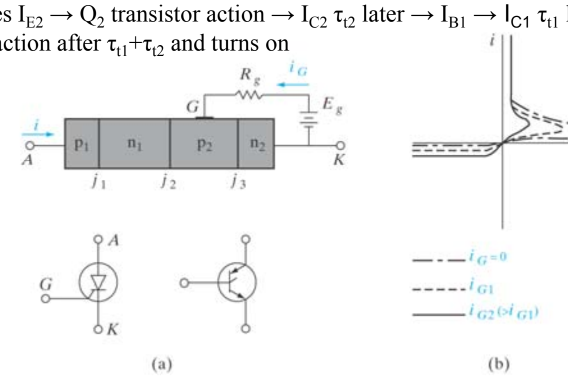


Figure 10.11
Two-transistor analogy of the p-n-p-n diode.

Triggering:
From fwd block → fwd conduct
Voltage triggering: Incr V > V_P
BW narrowing &/or avalanche multiplication ;
J_2 breakdown when $M_p\alpha_1 + M_n\alpha_2 = 1$
(BJT $I_{CEO} \rightarrow \infty$ when $M\alpha = 1$)
dv/dt triggering:
Apply transient fwd V
J_2 depletion grows by I_{B1} electrons & I_{B2} holes; regen action if dv/dt large.

$$i(t) = \frac{d(C_{j2} v_{j2})}{dt} = C_{j2}\frac{dv_{j2}}{dt} + v_{j2}\frac{dC_{j2}}{dt}$$

Silicon Controlled Rectifier (SCR) or Thyristor: PNPN, but with a gate for triggering
Turn on:
I_G (I_{B2}) initiates I_{E2} → Q_2 transistor action → I_{C2} τ_{t2} later → I_{B1} → I_{C1} τ_{t1} later
i.e. transistor action after $\tau_{t1}+\tau_{t2}$ and turns on



Turn off:
Reduce i below "holding current" (minimum required for $\alpha_1+\alpha_2=1$)

Typically $\tau_{t1}+\tau_{t2}$ ~μs, so μs pulse to turn on
Once on, stays on with $I_G=0$

Possible gate turn-off

Figure 10.13
A semiconductor-controlled rectifier: (a) four-layer geometry and common circuit symbols; (b) I–V characteristics.

External trigger: SCR
(semiconductor controlled rectifier)

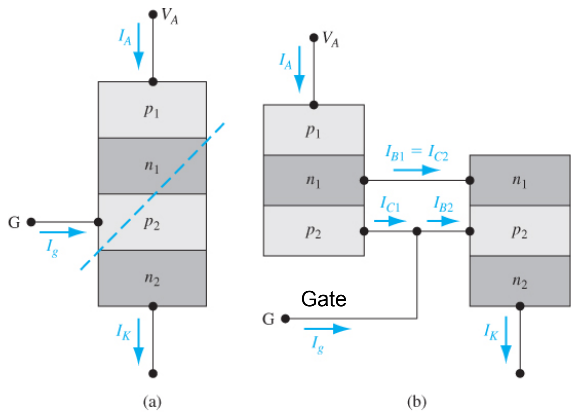


Figure 15.33 | (a) The three-terminal SCR. (b) The two-transistor equivalent circuit of the three-terminal SCR.

$I_{C1} = \alpha_1 I_A + I_{C01} = I_{B2}$
$I_{C2} = \alpha_2 I_K + I_{C02} = I_{B1}$

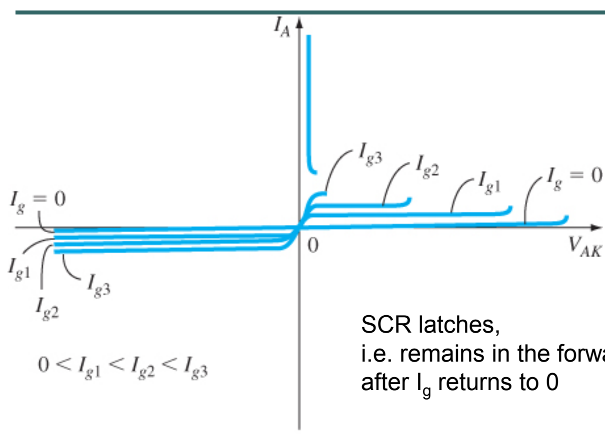
$I_A = I_{C1} + I_{C2}$
$I_K = I_{C1} + I_{C2} + I_g$

$I_A = (\alpha_1+\alpha_2)I_A+\alpha_2 I_g+(I_{C01}+I_{C02})$

so $I_A = \dfrac{(I_{C01}+I_{C02})+\alpha_2 I_g}{1-(\alpha_1+\alpha_2)}$

and I_g can initiate switching by injecting holes into p_2 (Q_1 collector, Q_2 base), i.e. I_{B2}

SCR characteristics



SCR latches,
i.e. remains in the forward conducting state after I_g returns to 0

Figure 15.34 | Current–voltage characteristics of an SCR.

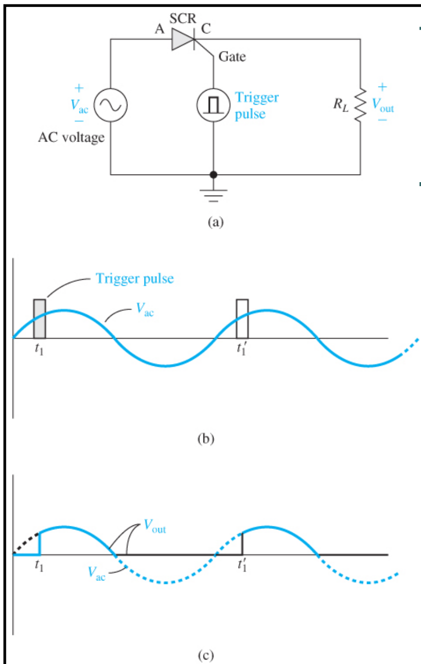


Figure 15.35 | (a) Simple SCR circuit. (b) Input ac voltage signal and trigger pulse. (c) Output voltage versus time.

SCR circuit

SCR turn-off:

Reduce I_A below the "holding current" where $(\alpha_1+\alpha_2) = 1$

e.g. $V_A < 0$

or (possibly) remove holes from p_2, (i.e. turn Q_2 off or take out of saturation)

or short circuit device

Basic SCR structure: $p_1n_1p_2n^+$ with p_2 gate

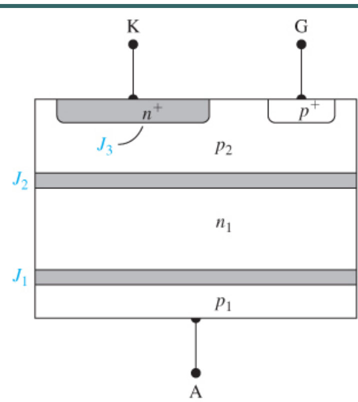


Figure 15.36 | The basic SCR device structure.

Bilateral trigger diode

Anti-parallel connection

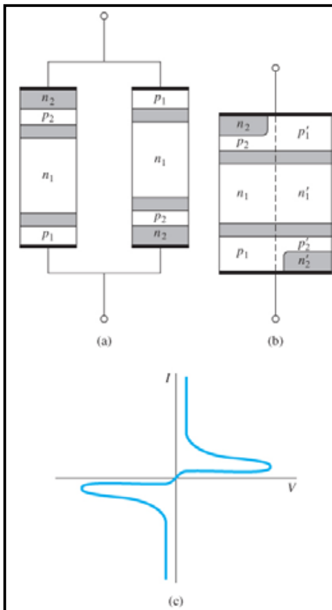


Figure 15.37 | (a) The antiparallel connection of two thyristors to form a bilateral device. (b) The bilateral thyristor as an integrated device. (c) The current–voltage characteristics of the bilateral thyristor. *(From Ghandhi [7].)*

TRIAC: Bilateral SCR

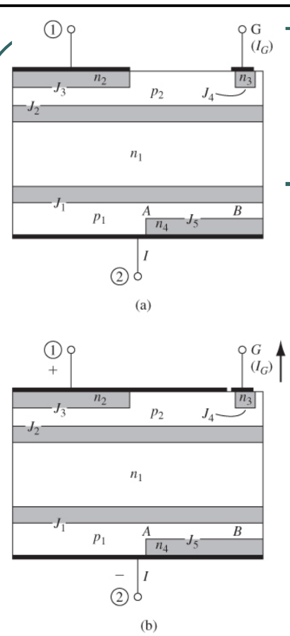


Figure 15.38 | (a) The triac device. (b) The triac with a specific bias configuration. *(From Ghandhi [7].)*

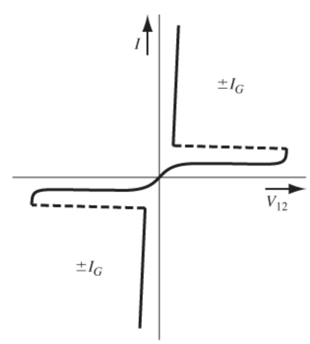


Figure 15.39 | The current–voltage characteristics of the triac.

MOS-gated SCR & MOS turn-off SCR

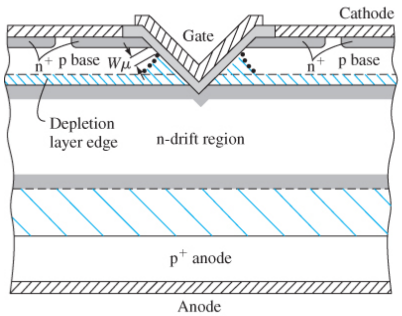


Figure 15.40 | The V groove MOS gated thyristor.
(From Baliga [1].)

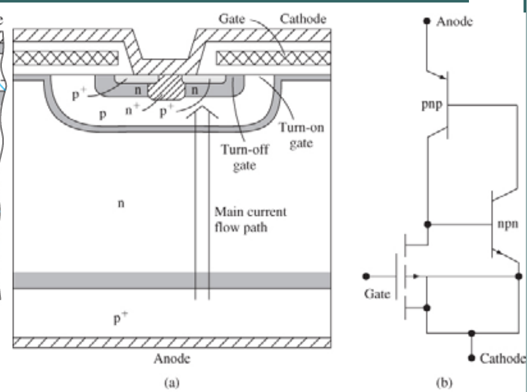


Figure 15.41 | (a) The MOS turn-off thyristor. (b) Equivalent circuit for the MOS turn-off thyristor.
(From Baliga [1].)

<u>IGBT</u> …. Designed to improve on SCR gate turn-off

Structure is an SCR with MOSFET that can connect cathode (E2) to C2/B1

p-channel length
determined by E & B
diffusions, not by gate length
i.e. DMOS:
double-diffused MOSFET

n^- region lightly doped,
i.e. high R
supports large blocking voltage
Becomes low R in ON state with
electrons injected from n+ cathode
(i.e. conductivity modulated FET(COMFET))

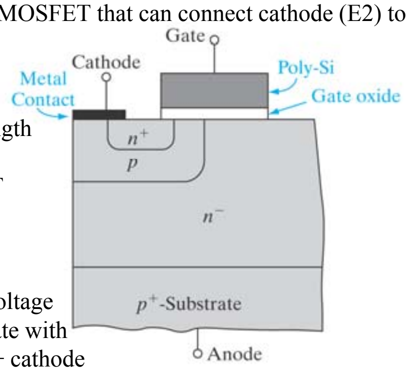
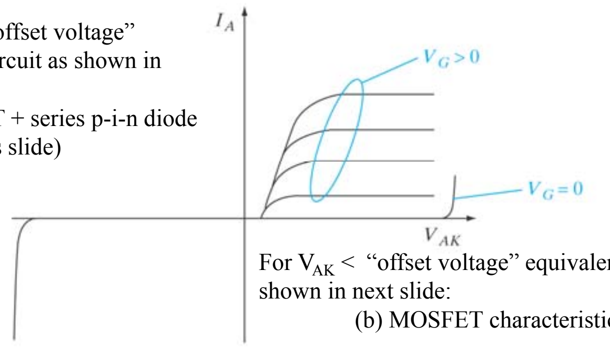


Figure 10.15

Structure of an insulated-gate bipolar transistor.

V_G=0 → PNPN characteristic

For V_{AK} < "offset voltage" equivalent circuit as shown in next slide:
(a) MOSFET + series p-i-n diode (see previous slide)



For V_{AK} < "offset voltage" equivalent circuit as shown in next slide:
(b) MOSFET characteristics x pnp gain

Figure 10.16
Output current–voltage characteristics of an insulated-gate bipolar transistor (n channel).

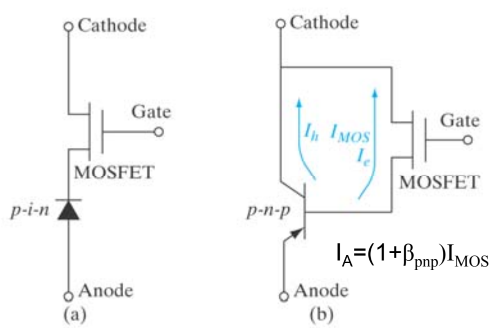


Figure 10.17
IGBT equivalent circuit: (a) below the offset voltage, for low V_{AK};
(b) above the offset voltage, for high V_{AK}.

Assignment 8(a)

15.7
15.8
15.17
15.19