# EE415/515 Fundamentals of Semiconductor Devices Fall 2012

## Lecture 12: Second order MOSFET (Chapter 11)



Reminder:
Here is what the MOSFET looks like

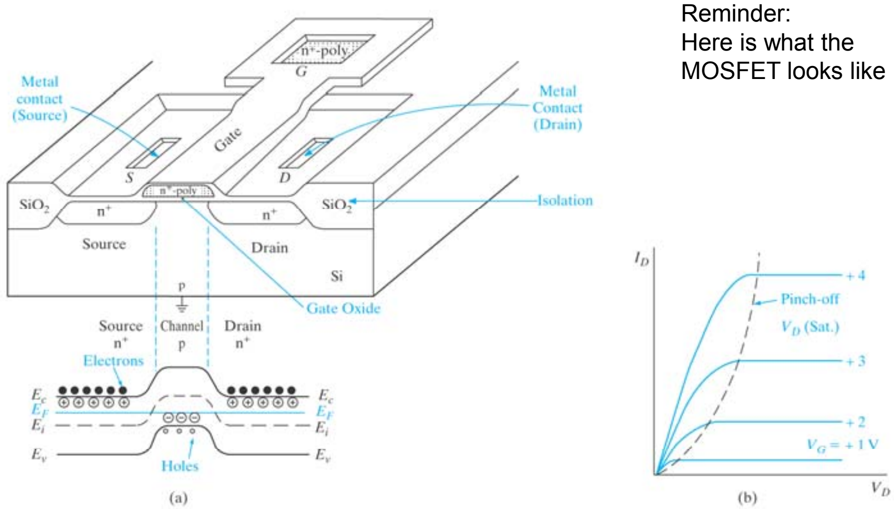


Figure 6.10

An enhancement-type n-channel MOSFET: (a) isometric view of device and equilibrium band diagram along channel; (b) drain current–voltage output characteristics as a function of gate voltage.

## Sub-threshold conduction ($V_{GS}<V_T$)

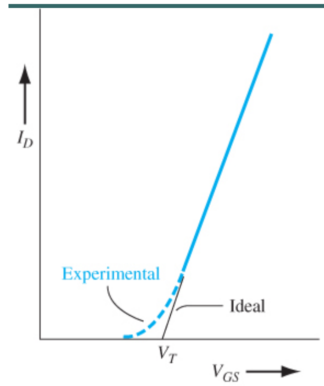


**Figure 11.1** | Comparison of ideal and experimental plots of $\sqrt{I_D}$ versus $V_{GS}$.

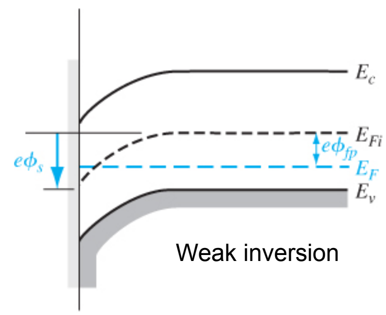


**Figure 11.2** | Energy-band diagram when $\phi_{fp} < \phi_s < 2\phi_{fp}$.



## $V_{GS}$: weak inversion

$$I_D(sub) \propto \left[\exp\frac{eV_{GS}}{kT}\right]\left[1-\exp-\frac{eV_{DS}}{kT}\right]$$

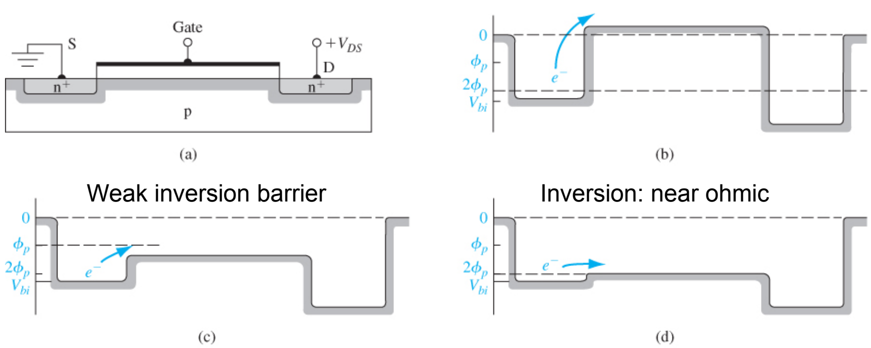


**Figure 11.3** | (a) Cross section along channel length of n-channel MOSFET. Energy-band diagrams along channel length at (b) accumulation, (c) weak inversion, and (d) inversion.

$$I_D(sub) \propto \left[\exp\frac{eV_{GS}}{kT}\right]\left[1-\exp-\frac{eV_{DS}}{kT}\right]$$

$$\Rightarrow \exp\frac{eV_{GS}}{kT} \quad \text{for } V_{DS} >> kT/e$$

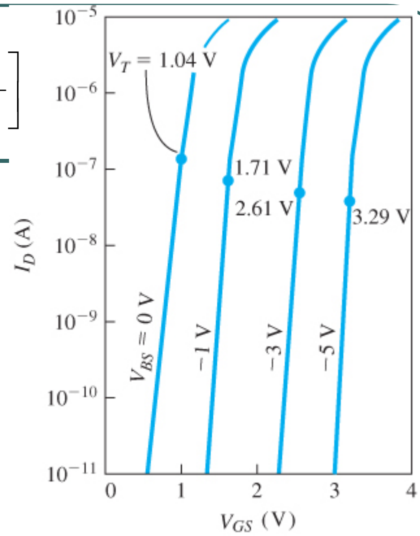


**Figure 11.4** | Subthreshold current–voltage characteristics for several values of substrate voltage (the threshold voltage is indicated on each curve). *(From Schroder [17].)*

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Sub-threshold Characteristics

Current does not abruptly turn off once $V_G < V_T$! There is still the region of ''weak inversion'' where some current still flows.

Surface potential changes between inversion ($\Phi_s = 2\Phi_F$) and flat band ($\Phi_s = \Phi_F$).

Note: $I_D$ depends exponentially on $V_G$.
(Linear semi-log plot)

Influence of $V_D$ is very limited (why?)

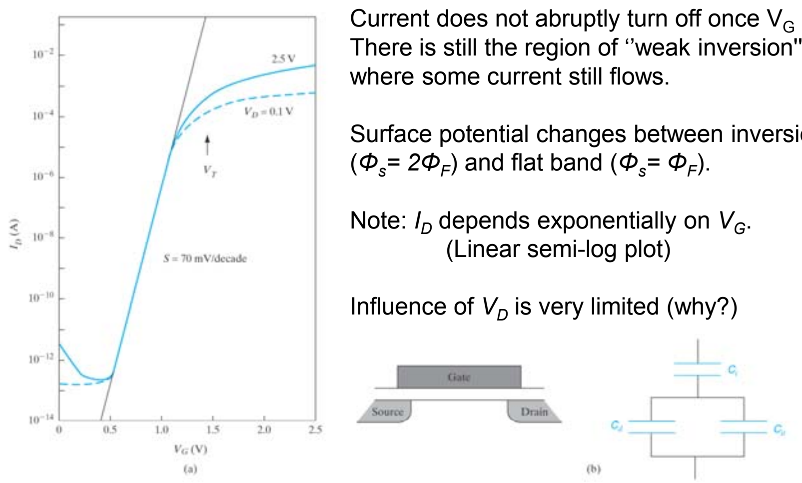


Figure 6.38

Subthreshold conduction in MOSFETs: (a) Semilog plot of $I_D$ versus $V_G$; (b) equivalent circuit showing capacitor divider which determines subthreshold slope.



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## Sub-threshold Characteristics

- Current is actually *diffusion current*

$$I_D = \mu(C_d + C_{it})\frac{Z}{L}\left(\frac{kT}{q}\right)^2\left(1-\exp\frac{-qV_D}{kT}\right)\exp\frac{q(V_G - V_T)}{c_r} \qquad (17)$$

*where* $$c_r = 1 + (C_d + C_{it})/C_i \qquad (18)$$

- Inverse of *log* $I_D$ *vs* $V_G$ slope is *subthreshold slope S* which is measured in mV/decade (of current change).
- Typically, S ≈ 70 mV/decade and at room temperature cannot be less than 65 mV/decade.

$$S = \frac{dV_G}{d(\log I_D)} = \ln 10\frac{dV_G}{d(\ln I_D)} = 2.3\frac{kT}{q}\left[1 + \frac{C_d + C_{it}}{C_i}\right] \qquad (19)$$

- Hand-waving: equivalent circuit is a series combo of oxide and depletion capacitance (+ fast states). Factor $c_r$ measures how much voltage is dropped on oxide, which is where we need it to get charge in the channel → ideal case is that $C_i >> C_d$
- Problem is that $C_d$ increases with substrate doping
- At lowest $V_G$ → no conduction - only p-n junction leakage
- Why is all this important?



## Channel length modulation

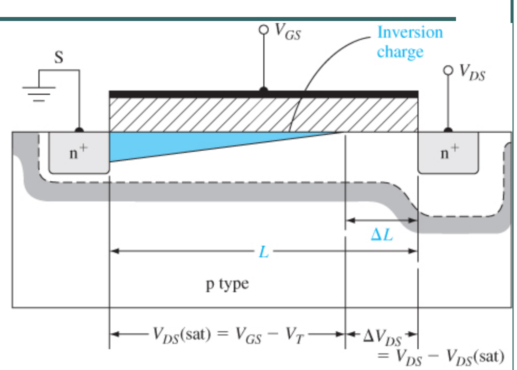



**Figure 11.5** | Cross-section of an n-channel MOSFET showing the channel length modulation effect.

$$x_p = \sqrt{\frac{2\varepsilon_s}{eN_a}(\phi_{fp} + V_{DS})}, \text{ so}$$

$$\Delta L = \sqrt{\frac{2\varepsilon_s}{eN_a}}\left[\sqrt{(\phi_{fp} + V_{DS}(sat) + \Delta V_{DS})} - \sqrt{(\phi_{fp} + V_{DS}(sat))}\right]$$

# Channel length modulation

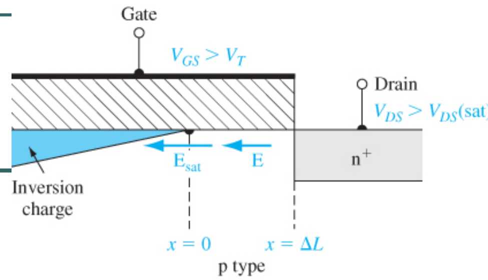



**Figure 11.6** | Expanded view of cross section near the drain terminal of an n-channel MOSFET showing the channel length modulation effect.

For space charge region : $\frac{dE}{dx} = \frac{\rho(x)}{\varepsilon_s} = \frac{-eN_a}{\varepsilon_s}$

$$\Rightarrow E = -\frac{eN_a x}{\varepsilon_s} - E_{sat}$$

$$\phi(x) = -\int E dx = \frac{eN_a x^2}{2\varepsilon_s} + E_{sat}x + V_{DS}(sat)$$

$$so\ V_{DS} = \phi(\Delta L) = \frac{eN_a \Delta L^2}{2\varepsilon_s} + E_{sat}\Delta L + V_{DS}(sat)$$

$$\&\ \Delta L = \sqrt{\frac{2\varepsilon_s}{eN_a}}\left[\sqrt{\phi_{sat} + \left(V_{DS} - V_{DS}(sat)\right)} - \sqrt{\phi_{sat}}\right]$$

$$where\ \phi_{sat} = \frac{2\varepsilon_s}{eN_a}\left(\frac{E_{sat}}{2}\right)^2$$

$$I_D'(actual) = \left(\frac{L}{L - \Delta L}\right) I_D(ideal) \text{ in saturation}$$

$$\Rightarrow \frac{k_n'}{2}.\frac{W}{L}.\left[(V_{GS} - V_T)^2(1 + \lambda V_{DS})\right]$$

$\lambda$ is channel length modulation parameter

$$r_0 = \left(\frac{\partial I_D'}{\partial V_{DS}}\right)^{-1} = \left[\frac{k_n'}{2}.\frac{W}{L}(V_{GS} - V_T)^2 \lambda\right]^{-1} \approx \frac{1}{\lambda I_D}$$



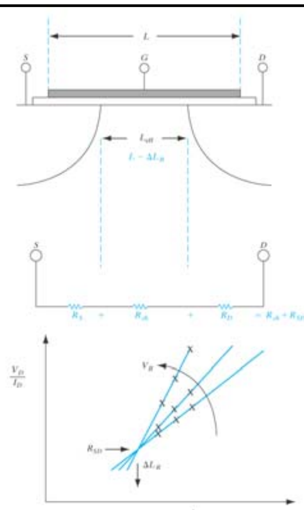


Figure 6.40

Determination of length reduction and source/drain series resistance in a MOSFET. The overall resistance of a MOSFET in the linear region is plotted as a function of channel length, for various substrate biases. The x's mark data points for three different physical gate lengths $L$.

# Short channel effect: experimental

$I_D$ not constant in saturation

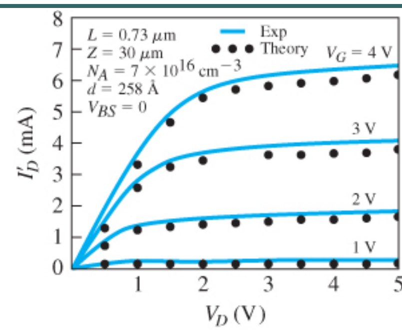



**Figure 11.7** | Current–voltage characteristics of a MOSFET showing short-channel effects.
*(From Sze [22].)*



**Ex 11.1 N-channel MOSFET: $N_a$=2x10$^{16}$/cm$^3$ & $V_T$=0.4V. Bias $V_{GS}$=0.8V & $V_{DS}$=2.5V. Find minimum channel length L so the ratio of actual drain current to ideal drain current due to channel length modulation is no larger than 1.35.**

$$\frac{I'_D}{I_D} = \frac{L}{L - \Delta L} = \frac{1}{1 - \frac{\Delta L}{L}} = 1.35$$

or

$$\frac{\Delta L}{L} = 1 - \frac{1}{1.35} = 0.259$$

From Example 11.1, we have $\Delta L = 0.1807\ \mu$m

Then $L = \frac{\Delta L}{0.259} = \frac{0.1807}{0.259} = 0.698\ \mu$m

## Mobility variation
## 1. Transverse electric field

- Channel mobility is **not** equal to bulk mobility. Observation: as $V_G$ is increased $\mu$ goes down
- This is interpreted to be due to increase *effective transverse electric field* (Streetman & Bannerjee Fig 6.31, slide 15)
- Non-trivial explanation but interesting side-effect is that reduction seems to be independent of technology details (so called “universal mobility curve”)



## Electric field → surface scattering

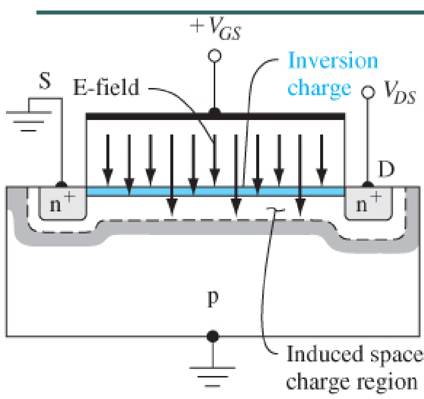



**Figure 11.8** | Vertical electric field in an n-channel MOSFET.

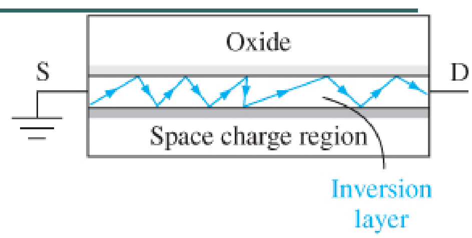



**Figure 11.9** | Schematic of carrier surface scattering effects.

$$E_{eff} = \frac{1}{\varepsilon_s}\left(\left|Q'_{SD}(\max)\right| + \frac{1}{2}Q'_n\right)$$

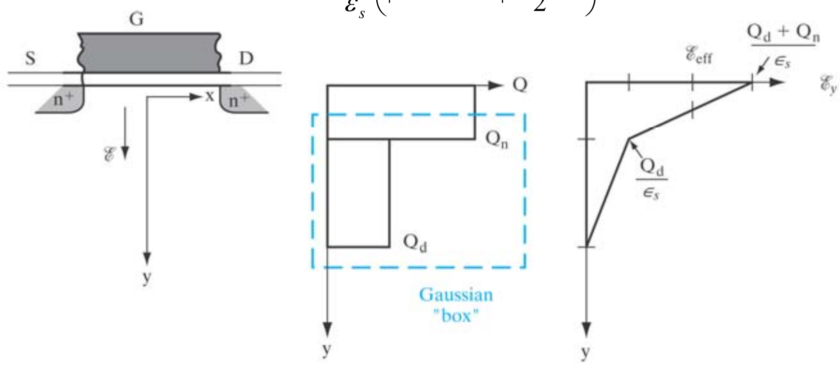



Figure 6.31

Determination of effective transverse field. Idealized charge distribution and transverse electric field in the inversion layer and depletion layer, as a function of depth in the channel of a MOSFET. The region to which we apply Gauss's law is shown in color.





## Effective mobility

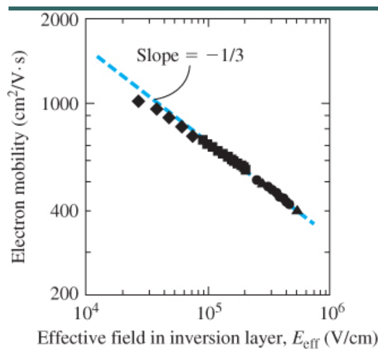
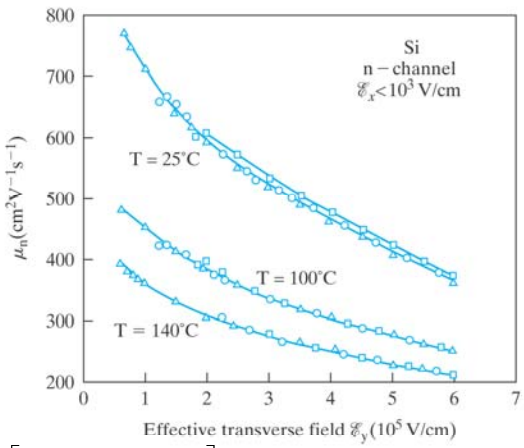



**Figure 11.10** | Measured inversion layer electron mobility versus electric field at the inversion layer.
*(From Yang [25].)*

$$\mu_{eff} = \mu_0\left(\frac{E_{eff}}{E_0}\right)^{-\frac{1}{3}}$$

$\mu_0$ , $E_0$ experimental constants




$$I_D = \frac{\overline{\mu_{ni}} Z C_i}{L[1+\theta(V_G - V_T)]}\left[(V_G - V_T)V_D - \frac{1}{2}V_D^2\right]$$

Figure 6.30 Θ is *mobility degradation parameter*

Inversion layer electron mobility versus effective transverse field, at various temperatures. The triangles, circles, and squares refer to different MOSFETs with different gate oxide thicknesses and channel dopings. (After Sabnis and Clemens, *IEEE IEDM*, 1979.)





**Ex 11.2 Use Fig 11.10 to determine the effective inversion layer electron mobility for a surface field of $E_{eff}$=2x10$^5$V/cm.**

From Figure 11.10, $\mu_n \cong 550$ cm$^2$/V-s

## Mobility variation
## 2. Velocity saturation

- Additional effect: *velocity saturation*. Practically all devices have this and not pinch-off
- As a result, $I_D$ is calculated as $I_D(sat) \approx ZC_i(V_G - V_T)v_s$

  where $Z$ is channel width, and $v_s$ is saturation velocity for longitudinal electric field $\xi > \xi_{sat}$ (Note: $\xi_{max}=(V_D-V_D(sat))/\Delta L$)
- What's the big deal? As shown in S&B Fig. 6.32 $I_D$ increases only **linearly** vs. $V_G$. Is this good or bad?

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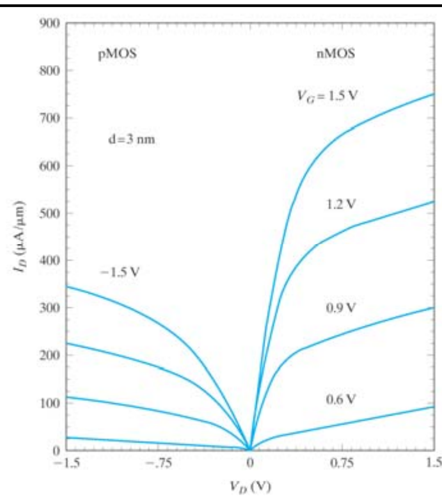


Figure 6.32

Experimental output characteristics of n-channel and p-channel MOSFETs with 0.1-μm channel lengths. The curves exhibit almost equal spacing, indicating a linear dependence of $I_D$ on $V_G$, rather than a quadratic dependence. We also see that $I_D$ is not constant but increases somewhat with $V_D$ in the saturation region. The p-channel devices have lower currents because hole mobilities are lower than electron mobilities.

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# Velocity saturation

$$I_D(sat) \approx WC_{ox}(V_{GS} - V_T)v_{sat}$$

$$\mu \approx \frac{\mu_{eff}}{\left[1 + \left(\frac{\mu_{eff} E}{v_{sat}}\right)^2\right]^{\frac{1}{2}}}$$

$$g_{ms} = WC_{ox}v_{sat}$$

(independent of $V_{GS}$ , $V_{DS}$ once velocity saturates)

$$f_T = \frac{g_m}{2\pi C_G} = \frac{WC_{ox}v_{sat}}{2\pi WLC_{ox}} = \frac{v_{sat}}{2\pi L}$$

Note also: ballistic transport

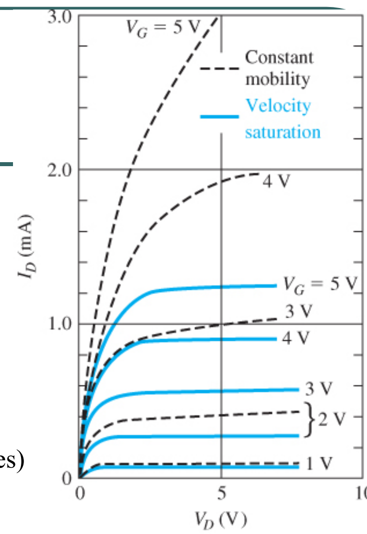



**Figure 11.11** | Comparison of $I_D$ versus $V_D$ characteristics for constant mobility (dashed curves) and for field-dependent mobility and velocity saturation effects (solid curves).
*(From Sze and Ng [22].)*



# Short MOSFET and Scaling

- Long MOSFET I-V plots shown already.
- Problem with velocity saturation already discussed
- What is scaling?
- Think of reducing the size of something on a copy machine. All dimensions are reduced by the same factor.
- However, we need to do something about applied voltage; ideally, it would scale with the same factor, but that has not been possible for some time. This is so-called “constant field" scaling approach. (it has become more like “constant voltage" approach)
- Why scale in the first place? see tables
- New effects with scaling: short-channel effects and hot-electron effects. The latter are (perhaps) not as big a deal now …

# Constant field scaling by k<1

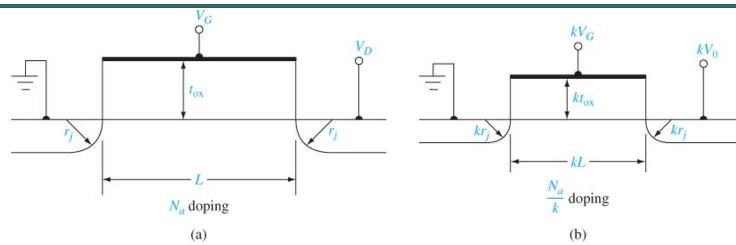



**Figure 11.12** | Cross section of (a) original NMOS transistor and (b) scaled NMOS transistor.

$$\frac{I_D}{W} = \frac{\mu_n \varepsilon_{ox}}{2t_{ox}L}(V_G - V_T)^2 \Rightarrow \frac{\mu_n \varepsilon_{ox}}{2(kt_{ox})(kL)}(kV_G - V_T)^2 \approx \text{constant (Note } \mathrm{V_T})$$

Constant field : $\mathrm{kV_G}$ , etc $\Rightarrow \mathrm{kt_{ox}}$

$$\mathrm{x_D} = \left[\frac{2\varepsilon_s(V_{bi} + V_D)}{eN_a}\right]^{\frac{1}{2}} \Rightarrow k\mathrm{x_D} \approx \left[\frac{2\varepsilon_s(V_{bi} + kV_D)}{e(N_a/k)}\right]^{\frac{1}{2}}$$



# Constant field scaling rules

**Table 11.1** | Summary of constant-field device scaling

| | Device and circuit parameters | Scaling factor ($k < 1$) |
|---|---|---|
| Scaled parameters | Device dimensions ($L$, $t_{ox}$, $W$, $x_j$) | $k$ |
| | Doping concentration ($N_a$, $N_d$) | $1/k$ |
| | Voltages | $k$ |
| Effect on device parameters | Electric field | 1 |
| | Carrier velocity | 1 |
| | Depletion widths | $k$ |
| | Capacitance ($C = \epsilon A/t$) | $k$ |
| | Drift current | $k$ |
| Effect on circuit parameters | Device density | $1/k^2$ |
| | Power density | 1 |
| | Power dissipation per device ($P = IV$) | $k^2$ |
| | Circuit delay time ($\approx CV/I$) | $k$ |
| | Power−delay product ($P\tau$) | $k^3$ |

Source: Taur and Ning [23].

# Constant field scaling rules
## (Streetman)

| Quantity or dimension | Scaling factor |
|---|---|
| Surface dimensions (L, Z) | 1/K |
| Vertical dimensions (d, $x_j$) | 1/K |
| Impurity concentrations | K |
| Current, voltages | 1/K |
| Current Density | K |
| Capacitance (per unit area) | K |
| Transconductance ($g_m$) | 1 |
| Circuit delay time | 1/K |
| Power dissipation | $1/K^2$ |
| Power density | 1 |
| Power-delay product | $1/K^3$ |



# Threshold voltage: short channel

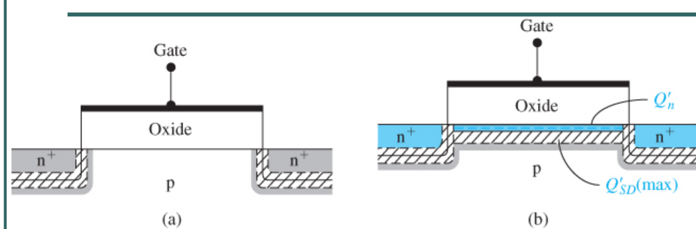



**Figure 11.13** | Cross section of a long n-channel MOSFET (a) at flat band and (b) at inversion.

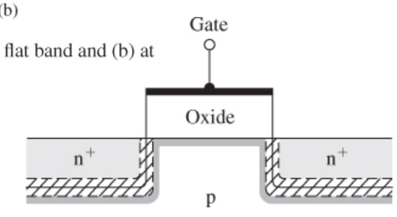
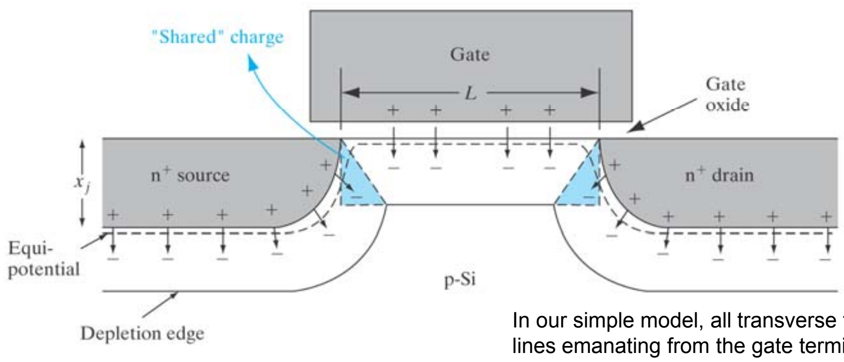



**Figure 11.14** | Cross section of a short n-channel MOSFET at flat band.

Gate controls less of $Q_{SD}'$(max) in the channel depletion region

Reduces $V_T$ by gate charge sharing.




In our simple model, all transverse field lines emanating from the gate terminate on charges in the substrate.

Figure 6.45

Short channel effect in a MOSFET. Cross-sectional view of MOSFET along the length showing depletion charge sharing (colored regions) between the gate, source and drain.

Problem: there is longitudinal field emanating from source and drain, and also terminating on charges inside the depletion layer → Not all $Q_d$ charge is controlled by the gate! Part that is not controlled by the gate has to be taken out of $V_T$ calculation → **reduction again**!





# Short channel $V_T$ reduction

## Potential difference ~$2\varphi_{fp}$ across depletion regions

## Hence $x_s \approx x_d \approx x_{dT} = x_{dT}$

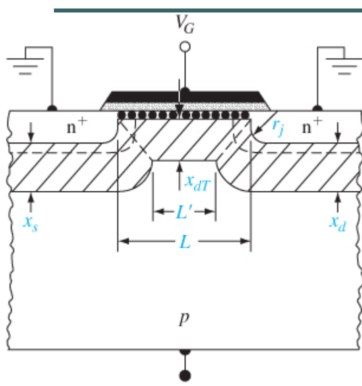



**Figure 11.15** | Charge sharing in the short-channel threshold voltage model. *(From Yau [26].)*

$$\text{Geometry} \Rightarrow \frac{L+L'}{2L} = 1 - \frac{r_j}{L}\left(\sqrt{1+\frac{2x_{dT}}{r_j}} - 1\right)$$

Bulk charge Q in trapezoid :

$$|Q_B'|L = eN_a x_{dT}\left(\frac{L+L'}{2}\right)$$

$$\text{so } |Q_B'| = eN_a x_{dT}\left[\left(1 - \frac{r_j}{L}\left(\sqrt{1+\frac{2x_{dT}}{r_j}} - 1\right)\right)\right]$$

$$\text{Since } |Q_{SD}'(\max)| = eN_a x_{dT}$$

$$\Delta V_T = V_{T(short\ channel)} - V_{T(long\ channel)}$$

$$= -\frac{eN_a x_{dT}}{C_{ox}}\left[\frac{r_j}{L}\left(\sqrt{1+\frac{2x_{dT}}{r_j}} - 1\right)\right]$$

## Channel length

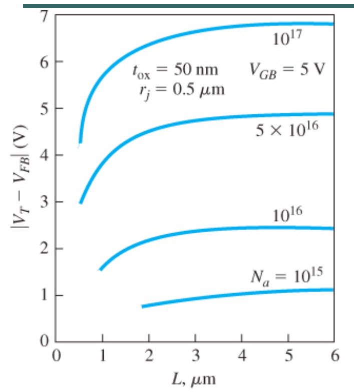



**Figure 11.16** | Threshold voltage versus channel length for various substrate dopings. (*From Yau [26].*)

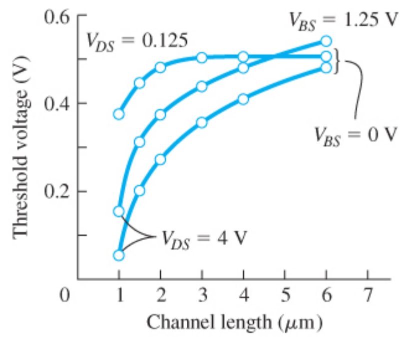



**Figure 11.17** | Threshold voltage versus channel length for two values of drain-to-source and body-to-source voltage. (*From Yang [25].*)



### Ex 11.3 Calculate the threshold voltage shift due to short channel effects for an N-channel MOSFET with $N_a = 10^{16}/cm^3$, $L = 0.75 μm$, $r_j = 0.25 μm$, & $t_{ox} = 12 nm$.

$$C_{ox} = \frac{(3.9)(8.85\times10^{-14})}{120\times10^{-8}} = 2.876\times10^{-7}\ \text{F/cm}^2$$

$$\phi_{fp} = (0.0259)\ln\left(\frac{10^{16}}{1.5\times10^{10}}\right) = 0.3473\ \text{V}$$

$$x_{dT} = \left[\frac{4(11.7)(8.85\times10^{-14})(0.3473)}{(1.6\times10^{-19})(10^{16})}\right]^{1/2} = 0.30\times10^{-4}\ \text{cm}$$

$$\Delta V_T = -\frac{eN_a x_{dT}}{C_{ox}}\left[\frac{r_j}{L}\left(\sqrt{1+\frac{2x_{dT}}{r_j}}-1\right)\right] = -\frac{(1.6\times10^{-19})(10^{16})(0.30\times10^{-4})}{2.876\times10^{-7}}\times\left[\frac{0.25}{0.75}\left(\sqrt{1+\frac{2(0.3)}{0.25}}-1\right)\right]$$

$$\Delta V_T = -0.0469\ \text{V}$$

Hot electron effects: related to gate charge (traps) formation, injection into the gate (current) and substrate leakage current.
Main issue is long-term drift and degradation of characteristics.

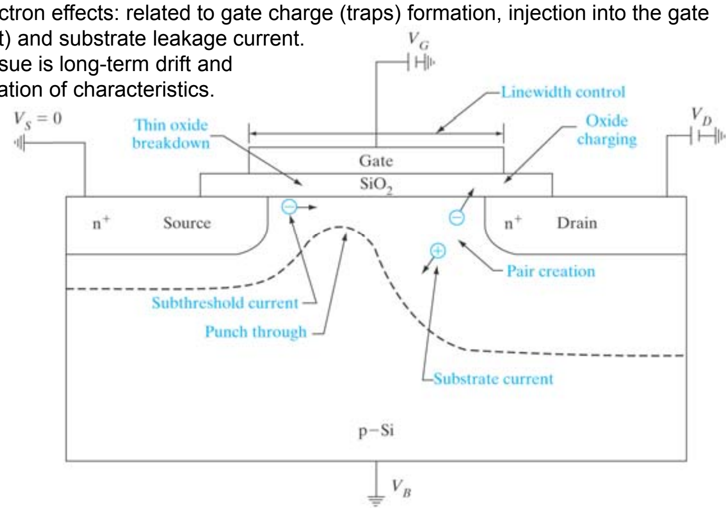



Figure 6.41

Short channel effects in MOSFETs. As MOSFETs are scaled down, potential problems due to short channel effects include hot carrier generation (electron–hole pair creation) in the pinch-off region, punch-through breakdown between source and drain, and thin gate oxide breakdown.



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Hot electrons

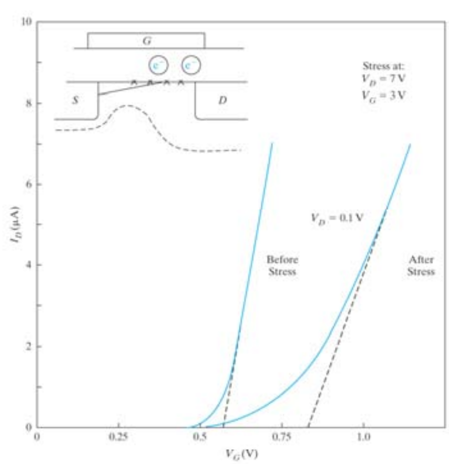


Figure 6.42

Hot carrier degradation in MOSFETs. The linear region transfer characteristics before and after hot carrier stress indicate an increase of $V_T$ and decrease of transconductance (or channel mobility) due to hot electron damage. The damage can be due to hot electron injection into the gate oxide which increases the fixed oxide charge, and increasing fast interface state densities at the oxide-silicon interface (indicated by *x*).



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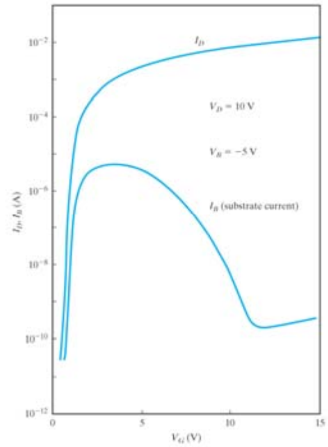


Figure 6.43

Substrate current in a MOSFET. The substrate current in n-channel MOSFETs due to impact-generated holes in the pinch-off region, as a function of gate bias. The substrate current initially increases with $V_G$ because of the corresponding increase of $I_D$. However, for even higher $V_G$, the MOSFET goes from the saturation to the linear region, and the high electric fields in the pinch-off region decrease, causing less impact ionization. (After Kamata, et. al. , *Jpn. J. Appl. Phys*., 15 (1976), 1127.)



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# Narrow channel effects

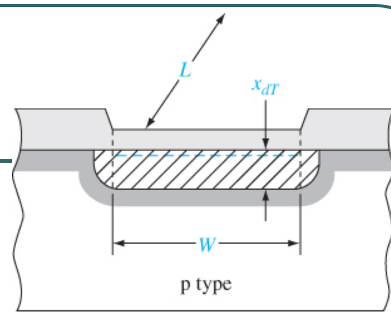


**Figure 11.18** | Cross section of an n-channel MOSFET showing the depletion region along the width of the device.

Gate controlled bulk charge :

$$|Q_B| = |Q_{B0}| + |\Delta Q_B|$$
$$= eN_a WLx_{dT} + eN_a Lx_{dT}(\xi x_{dT})$$
$$= eN_a WLx_{dT}\left(1 + \frac{\xi x_{dT}}{W}\right)$$

where $\Delta Q_B$ is the extra charge at the edges of the channel

and $\xi$ is a fitting parameter for the lateral space charge width

($\xi = \pi/2$ if edges are semi - circular)

$$\Delta V_T = \frac{eN_a x_{dT}}{C_{ox}}\left(\frac{\xi x_{dT}}{W}\right) \Rightarrow \text{incr as W decr}$$

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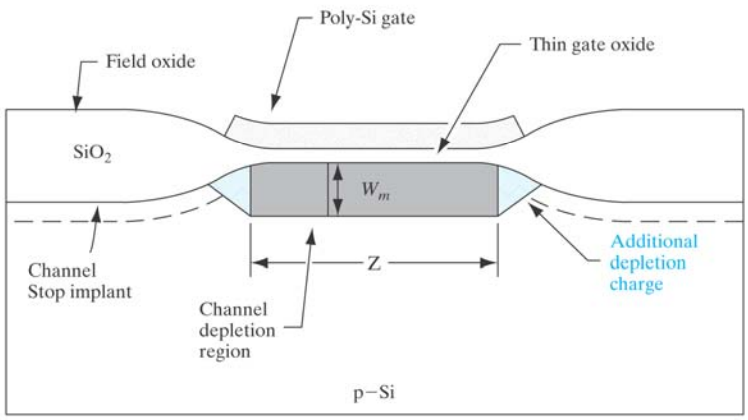


Figure 6.47

Narrow width effect in a MOSFET. Cross-sectional view of MOSFET along the width, showing additional depletion charge (colored regions) underneath the field or the LOCOS isolation regions.





# $V_T$ channel width effect

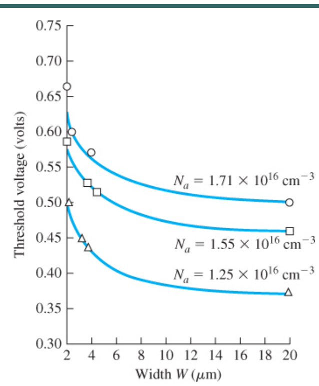


**Figure 11.19** | Threshold voltage versus channel width (solid curves, theoretical; points, experimental).
*(From Akers and Sanchez [1].)*

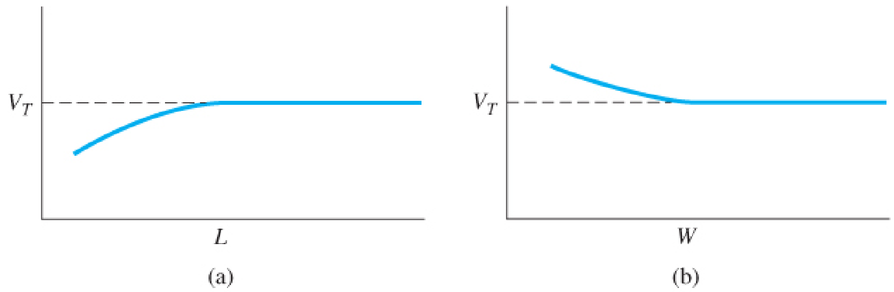


Figure 11.20 | Qualitative variation of threshold voltage (a) with channel length and (b) with channel width.

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Another effect - narrow width effect - works on increasing the $V_T$.

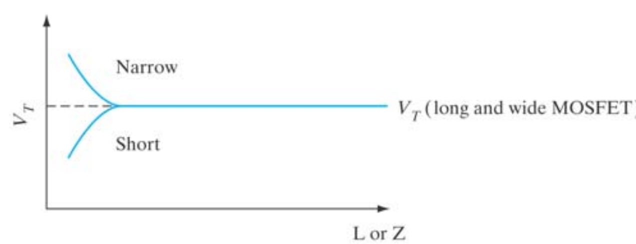


Figure 6.46
Roll-off of $V_T$ with decreasing channel length, and increase of $V_T$ with decreasing width.



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**Ex 11.4 $N_a = 10^{16}/cm^3$ & $t_{ox}$=8nm. Determine the channel width so the threshold voltage shift is limited to $\Delta V_T$=0.1V.**

$$\phi_{fp} = (0.0259)\ln\left(\frac{10^{16}}{1.5\times10^{10}}\right) = 0.3473 \text{ V}$$

$$x_{dT} = \left[\frac{4(11.7)(8.85\times10^{-14})(0.3473)}{(1.6\times10^{-19})(10^{16})}\right]^{1/2} = 0.30\times10^{-4} \text{ cm}$$

$$C_{ox} = \frac{(3.9)(8.85\times10^{-14})}{80\times10^{-8}} = 4.314\times10^{-7} \text{ F/cm}^2$$

$$W = \frac{eN_a(\xi x_{dT}^2)}{C_{ox}(\Delta V_T)} = \frac{(1.6\times10^{-19})(10^{16})\left(\frac{\pi}{2}\right)(0.30\times10^{-4})^2}{(4.314\times10^{-7})(0.1)}$$

$W = 5.243\times10^{-5}$ cm or $W = 0.524\,\mu$m



# Breakdown: Avalanche

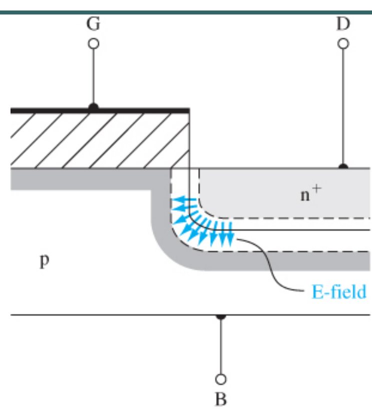



**Figure 11.21** | Curvature effect on the electric field in the drain junction.

Field increased in regions of large curvature

# Parasitic BJT & snapback

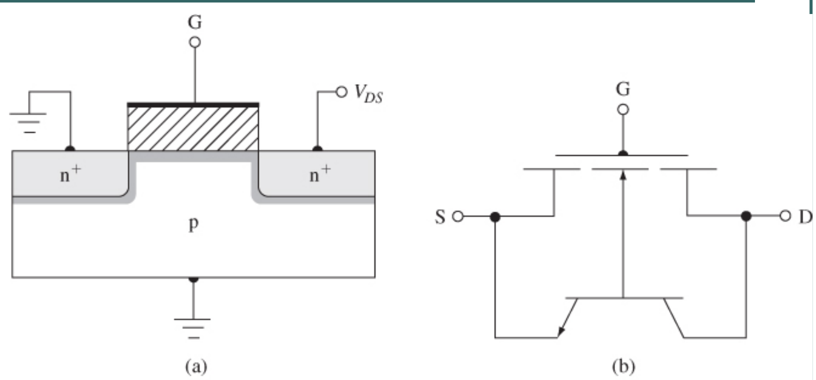
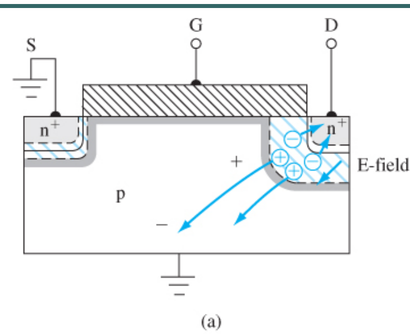



Figure 11.23 | (a) Cross section of the n-channel MOSFET. (b) Equivalent circuit including the parasitic bipolar transistor.



# Parasitic BJT




Drain near-avalanche increases current and ohmic voltage drop increases $V_{BE}$ and turns on BJT

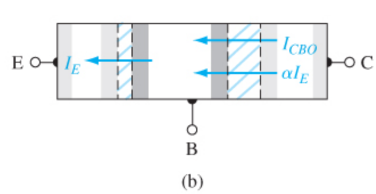



Figure 11.24 | (a) Substrate current–induced voltage drop caused by avalanche multiplication at the drain. (b) Currents in the parasitic bipolar transistor.

## Snapback

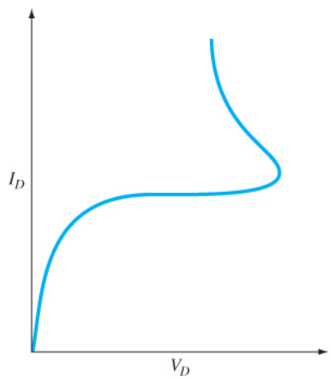



**Figure** 11.22 | Current–voltage characteristic showing the snapback breakdown effect.

For open - base BJT

$$I_C = \alpha I_E + I_{CBO}$$

$$I_C = I_E \text{ so } I_C = \alpha I_C + I_{CBO}$$

$$= \frac{I_{CBO}}{1-\alpha}$$

But at breakdown, $I_C$ multiplied by M

$$\text{so } I_C = M(\alpha I_C + I_{CBO})$$

$$= \frac{MI_{CBO}}{1-\alpha M} \to \infty \text{ when } \alpha M \to 1$$

$$\text{Typically } M = \frac{1}{1 - (V_{CE}/V_{BD})^m}, \text{ m = 3 to 6}$$

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## Drain-induced Barrier Lowering (DIBL)

- Junctions too deep or doping too low → source and drain start "interacting". This results in **reduction of barrier** for electron injection into channel. → reduction in $V_T$ at higher $V_D$
- Think of it as drain voltage "pulling down" the potential on the source side
- Solutions: increased substrate doping and shallow (scaled depth) junctions.
- Uniformly increasing doping has bad side-effects; halo implants could be used, but …..
- How is this reflected in I-V curves and what are the circuit implications?
- What's a model for this? $I_D \propto (L-\Delta L)^{-1} \approx L^{-1}(1+\Delta L/L) = (1+\lambda V_D)/L$

$$I_D = \frac{Z}{2L}\mu_n C_i (V_G - V_T)^2 (1+\lambda V_D)$$

which produces a slope in output characteristics.
- Parameter $\lambda$ is a fitting parameter that includes all possible effects

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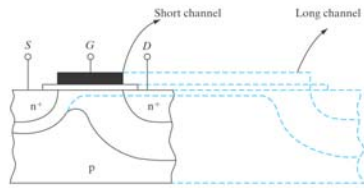
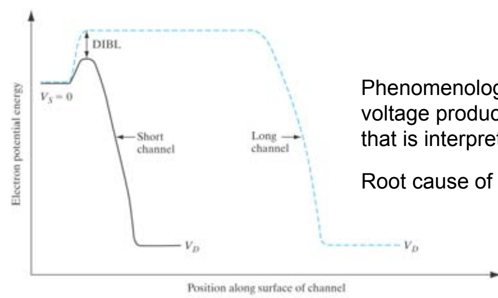



Drain Induced Barrier Lowering
(DIBL)
and charge sharing.




Phenomenologically: change in drain voltage produces an increase in $I_D$ that is interpreted as a change in $V_T$

Root cause of DIBL: see figure

Figure 6.44

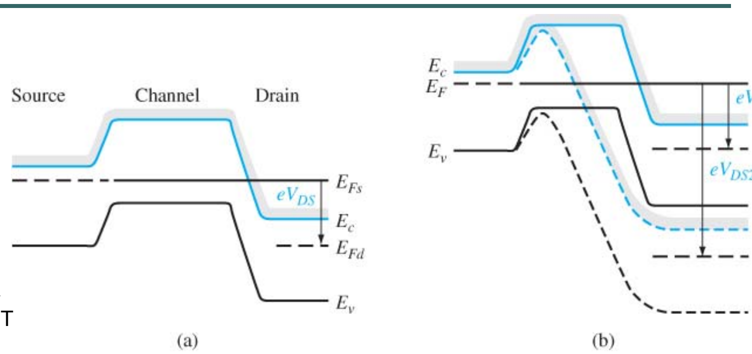
Drain-induced barrier lowering in MOSFETs. Cross sections and potential distribution along the channel for a long channel and short channel MOSFET.





# DIBL: Drain-induced barrier lowering

Punchthrough: Drain & source depletion regions meet, channel barrier → zero.
Near punchthrough: Channel barrier reduced, large currents possible.




$V_{GS}<V_T$

**Figure 11.25** | (a) Equipotential plot along the surface of a long-channel MOSFET. (b) Equipotential plot along the surface of a short-channel MOSFET before and after punch-through.

# DIBL: Drain-induced barrier lowering

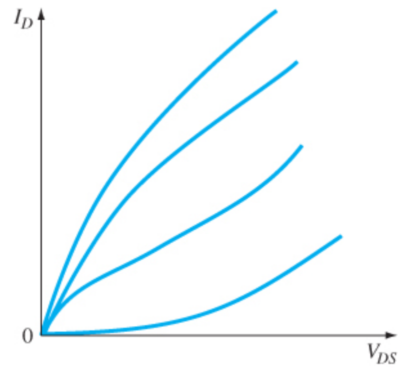



**Figure 11.26** | Typical *I*–*V* characteristics of a MOSFET exhibiting punch-through effects.



And finally:
Gate-induced Drain Leakage

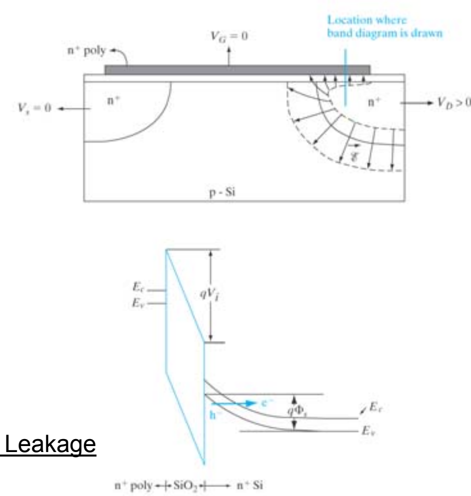



Figure 6.48

Gate-induced drain leakage in MOSFETs. The band diagram for the location shown in color is plotted as a function of depth in the gate–drain overlap region, indicating band-to-band tunneling and creation of electron–hole pairs in the drain region in the Si substrate.

**Ex 11.5 Calculate the theoretical punch -through voltage for an N-channel MOSFET with substrate doping $N_a$=3x10$^{16}$/cm$^3$ , source/drain doping $N_d$=10$^{16}$/cm$^3$, & L=0.8μm. Assume an abrupt junction and that the source and body are grounded.**

$$V_{bi} = V_t \ln\left(\frac{N_a N_d}{n_i^2}\right) = (0.0259)\ln\left[\frac{(3\times10^{16})(10^{19})}{(1.5\times10^{10})^2}\right] = 0.902 \text{ V}$$

$$x_{dO} = \left[\frac{2\epsilon_s V_{bi}}{eN_a}\right]^{1/2} = \left[\frac{2(11.7)(8.85\times10^{-14})(0.902)}{(1.6\times10^{-19})(3\times10^{16})}\right]^{1/2} = 1.973\times10^{-5} \text{ cm} = 0.1973\ \mu\text{m}$$

$$x_d = L - x_{dO} = 0.8 - 0.1973 = 0.6027\ \mu\text{m}$$

Also $x_d = \left[\frac{2\epsilon_s (V_{bi}+V_{DS})}{eN_a}\right]^{1/2}$ or $V_{bi}+V_{DS} = \frac{x_d^2 eN_a}{2\epsilon_s} = \frac{(0.6027\times10^{-4})^2(1.6\times10^{-19})(3\times10^{16})}{2(11.7)(8.85\times10^{-14})}$

$V_{bi}+V_{DS} = 8.419$ V Then $V_{DS} = 8.419 - 0.902 = 7.52$ V



# Lightly doped drain (LDD)

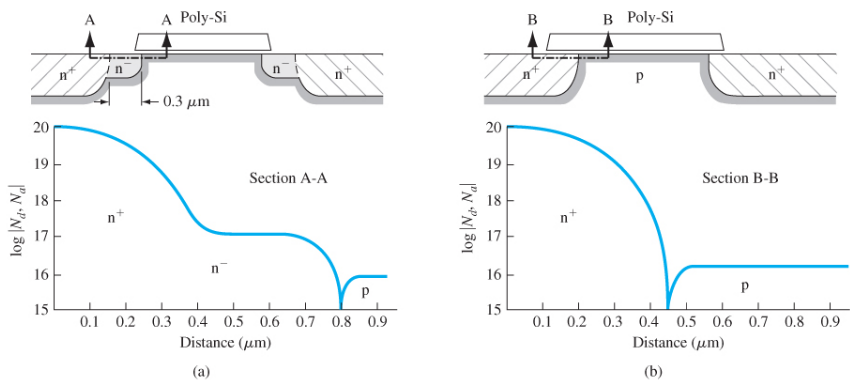



Figure 11.27 | (a) The lightly doped drain (LDD) structure. (b) Conventional structure. (*From Ogura et al. [12].*)

n$^-$ region reduces local fields

# Lightly doped drain (LDD)

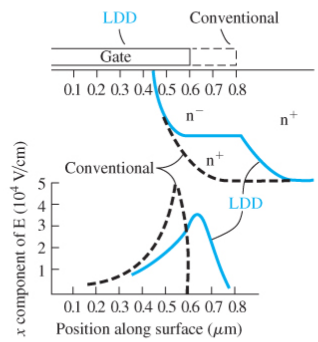



**Figure 11.28** | Magnitude of the electric field at the Si–$SiO_2$ interface as a function of distance; $V_{DS} = 10$ V. $V_{SB} = 2$ V, $V_{GS} = V_T$. *(From Ogura et al. [12].)*



# Threshold Voltage

Obviously, controlling $V_T$ is very important. How is it done?

1. Choice of gate electrode
2. Control of gate oxide $C_i$
3. control of doping (typically using ion implantation)
4. Special case: using substrate bias

   Starting point is

$$V_T = \phi_{ms} - \frac{Q_i}{C_i} - \frac{Q_d}{C_i} + 2\phi_F$$

- S & B Fig. 6.33 illustrates what's going on.

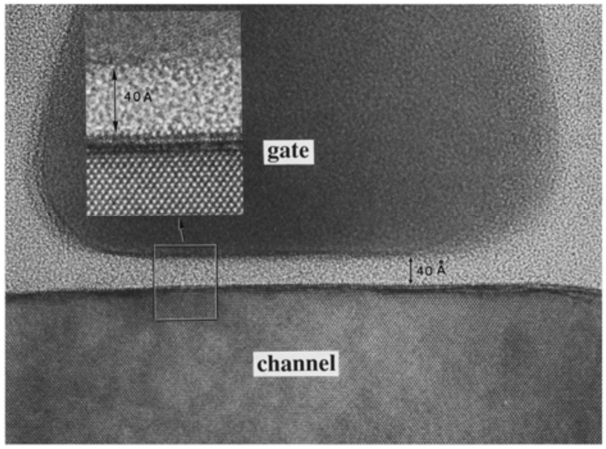



Figure 6.33

Cross section of a MOSFET. This high resolution transmission electron micrograph of a silicon Metal–Oxide Semiconductor Field Effect Transistor shows the silicon channel and metal gate separated by a thin (40 Å, 4 nm) silicon–dioxide insulator. The inset shows a magnified view of the three regions, in which individual rows of atoms in the crystalline silicon can be distinguished. (Photograph courtesy of AT&T Bell Laboratories.)





## $V_T$ Control

- Until recently, choice of gate materials was limited. In recent years, it has become possible to *control* the properties of metals, such as their work function. Critical for recent success of deeply scaled devices.
- More traditionally, *n*+ and *p*+ gates are used. ``Nice'' metal would have so-called mid-gap workfunction.
- 2nd and 3rd terms are reduced by increasing $C_i$ (which is also good for drive current) → reduction in absolute value of $V_T$
- How is $C_i$ increased? Two options ……..
- Changing doping underneath (preferably) or in the channel
- Net effect: increase of, say, $N_a^-$ *locally* so it looks as if the substrate has a larger doping for n-channel devices → $V_T$ ……
- For p-channel, implanting boron will compensate some of the $N_D^+$ which would make the doping look smaller and make $V_T$ less negative.

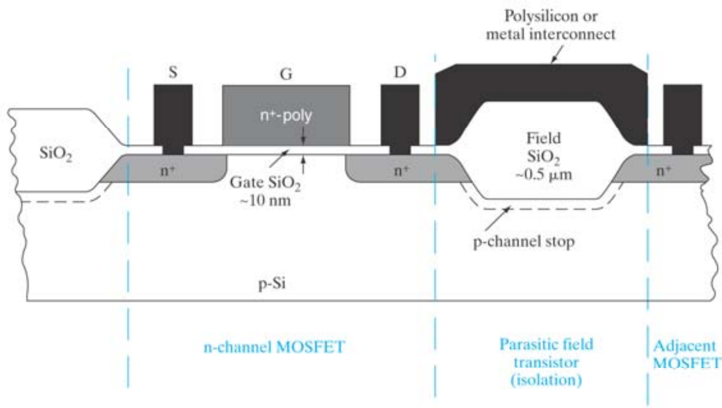



Figure 6.34

Thin oxide in the gate region and thick oxide in the field between transistors for $V_T$ control (not to scale).

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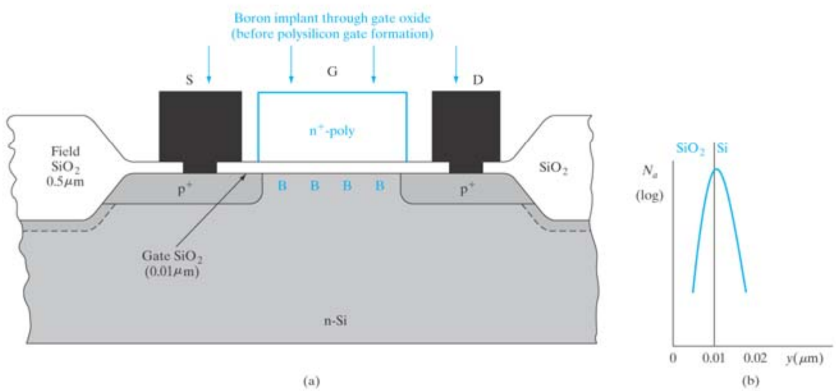


Figure 6.35

Adjustment of $V_T$ in a p-channel transistor by boron implantation: (a) boron ions are implanted through the thin gate oxide but are absorbed within the thick oxide regions; (b) variation of implanted boron concentration in the gate region–here the peak of the boron distribution lies just below the Si surface.

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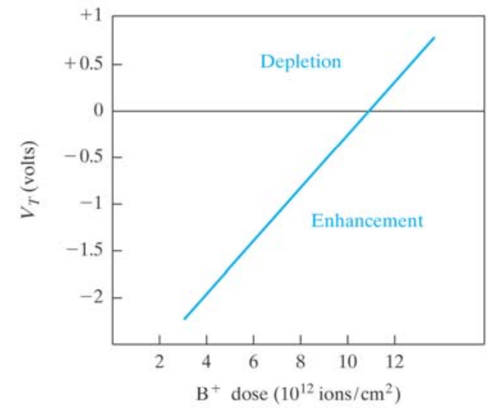


Figure 6.36

Typical variation of $V_T$ for a p-channel device with increased implanted boron dose. The originally enhancement p-channel transistor becomes a depletion-mode device ($V_T > 0$) by sufficient B implantation.





# VT Adjustment by Ion Implantation

(a) $\Delta V_T = +\frac{eD_I}{C_{ox}}$

for $D_1$ acceptors/unit area implanted into P - substrate

Negative $\Delta V_T$ if donors implanted.

(b) For $x_1 < x_{dT} \Rightarrow V_T = V_{T0} + \frac{eD_I}{C_{ox}}$ where $D_1 = (N_s - N_a)x_I$

For $x_1 < x_{dT} \Rightarrow x_{dT} \rightarrow \sqrt{\frac{2\varepsilon_s}{eN_a}}\left[2\phi_{fp} - \frac{ex_j^{\ 2}}{2\varepsilon_s}(N_s - N_a)\right]^{\frac{1}{2}}$

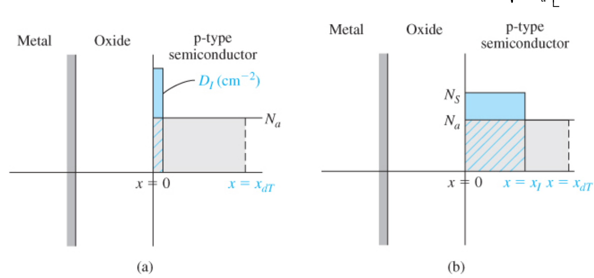


**Figure 11.29** | (a) Ion-implanted profile approximated by a delta function. (b) Ion-implanted profile approximated by a step function in which the depth $x_i$ is less than the space charge width $x_{dT}$.

**Ex 11.6 Si MOSFET: $N_a$=10$^{15}$/cm$^3$, p+ poly-Si gate with an initial FB voltage $V_{FB0}$=+0.95V, $t_{ox}$=12nm. A final threshold voltage $V_T$=+0.40V is required. Assume the idealized delta function of Fig 11.29(a) for the ion implant profile. (a) Which type of ion (donor or acceptor) should be implanted? (b) Calculate the ion dose $D_I$ required.**

We find $\phi_{fpO} = (0.0259)\ln\left(\frac{10^{15}}{1.5\times10^{10}}\right) = 0.2877\,\text{V}$

$$x_{dTO} = \left[\frac{4\in_s V_{bi}}{eN_a}\right]^{1/2} = \left[\frac{4(11.7)(8.85\times10^{-14})(0.2877)}{(1.6\times10^{-19})(10^{15})}\right]^{1/2} = 8.630\times10^{-5}\,\text{cm} = 0.863\,\mu\text{m}$$

$$C_{ox} = \frac{(3.9)(8.85\times10^{-14})}{120\times10^{-8}} = 2.876\times10^{-7}\,\text{F/cm}^2$$

The initial threshold voltage is

$$V_{TO} = V_{FBO} + 2\phi_{fpO} + \frac{eN_a x_{dTO}}{C_{ox}} = +0.95 + 2(0.2877) + \frac{(1.6\times10^{-19})(10^{15})(8.63\times10^{-5})}{2.876\times10^{-7}}$$

$V_{TO} = 1.573\,\text{V}$

Now $V_T = V_{TO} + \Delta V_T$ i.e. $0.40 = 1.573 + \Delta V_T \Rightarrow \Delta V_T = -1.173\,\text{V}$

Negative $\Delta V_T \Rightarrow$ implant donor ions

Now $|\Delta V_T| = \frac{eD_I}{C_{ox}}$ or $D_I = \frac{|\Delta V_T| C_{ox}}{e} = \frac{(1.173)(2.876\times10^{-7})}{1.6\times10^{-19}} = 2.11\times10^{12}\,\text{cm}^{-2}$



# Radiation-induced oxide charge

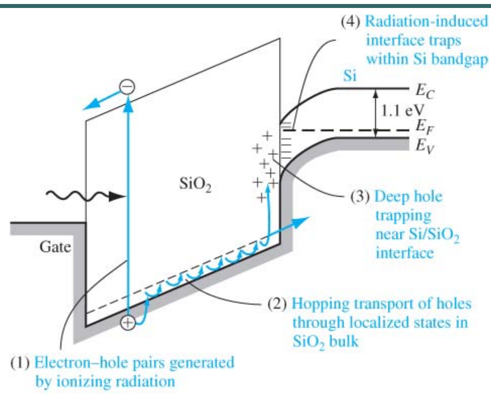


**Figure 11.30** | Schematic of ionizing radiation–induced processes in an MOS capacitor with a positive gate bias. *(From Ma and Dressendorfer [7].)*

# Radiation-induced oxide charge

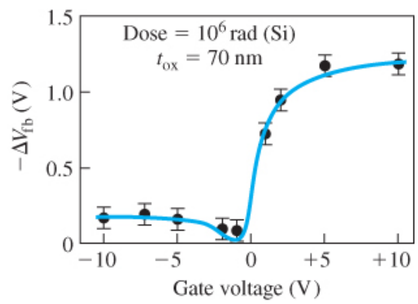


**Figure 11.31** | Radiation-induced flat-band voltage shift in an MOS capacitor as a function of applied gate bias during irradiation.
*(From Ma and Dressendorfer [7].)*

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**Ex 11.7 Calculate the threshold voltage shift due to radiation-induced oxide charge trapping, for a MOS device with oxide thickness $t_{ox}$ of (a) 12nm & (b) 8nm. (c) What can be said about $\Delta V_T$ as $t_{ox}$ decreases?**

**Assume an ionizing pulse creates $10^{18}$ EHPs/cm$^3$ in the oxide, and that the electrons are swept out through the gate terminal with zero recombination, and that 20% of the holes are trapped at the oxide-semiconductor interface.**

(a) $N_h = (10^{18})(120\times10^{-8}) = 1.2\times10^{12}$ cm$^{-2}$

$Q'_{ss} = (1.2\times10^{12})(0.2) = 2.4\times10^{11}$ cm$^{-2}$

$C_{ox} = \dfrac{(3.9)(8.85\times10^{-14})}{120\times10^{-8}} = 2.876\times10^{-7}$ F/cm$^2$

Then $\Delta V_T = -\dfrac{Q'_{ss}}{C_{ox}} = -\dfrac{(2.4\times10^{11})(1.6\times10^{-19})}{2.876\times10^{-7}} = -0.134$ V

(b) $N_h = (10^{18})(80\times10^{-8}) = 8\times10^{11}$ cm$^{-2}$

$Q'_{ss} = (8\times10^{11})(0.2) = 1.6\times10^{11}$ cm$^{-2}$

$C_{ox} = \dfrac{(3.9)(8.85\times10^{-14})}{80\times10^{-8}} = 4.314\times10^{-7}$ F/cm$^2$

Then $\Delta V_T = -\dfrac{Q'_{ss}}{C_{ox}} = -\dfrac{(1.6\times10^{11})(1.6\times10^{-19})}{4.314\times10^{-7}} = -0.0593$ V

(c) Threshold voltage shift decreases when the oxide thickness decreases.

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# Radiation-induced interface states

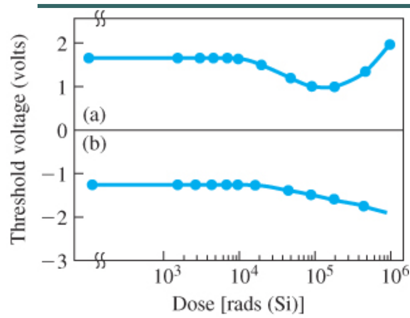


**Figure 11.32** | Threshold voltage versus total ionizing radiation dose of (a) an n-channel MOSFET and (b) a p-channel MOSFET.
*(From Ma and Dressendorfer [7].)*

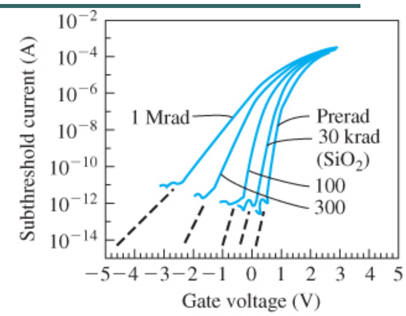


**Figure 11.33** | Subthreshold current versus gate voltage of a MOSFET prior to irradiation and at four total radiation dose levels.
*(From Ma and Dressendorfer [7].)*



# Radiation-induced interface states

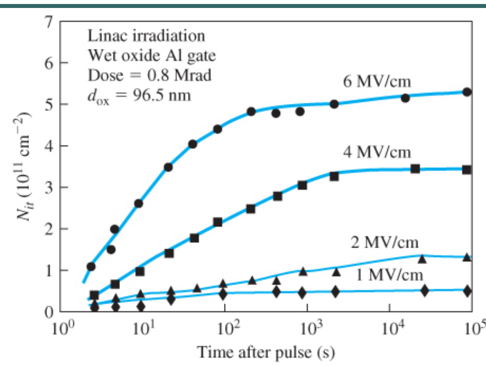


**Figure 11.34** | Radiation-induced interface state density versus time after a pulse of ionizing radiation for several values of oxide electric field.
*(From Ma and Dressendorfer [7].)*

## Hot electron charging

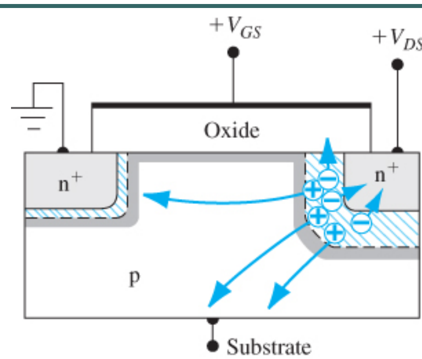


**Figure 11.35** | Hot carrier generation, current components, and electron injection into the oxide.



## Assignment #6

| | |
|---|---|
| 10.36 | 11.2 |
| 10.42 | 11.5 |
| 10.47 | 11.10 |
| 10.52 | 11.17 |