EE415/515 Fundamentals of Semiconductor Devices Fall 2012

Lecture 11: MOSFET (Chapter 10.3, 10.4)

Reminder:
Here is what the MOSFET looks like

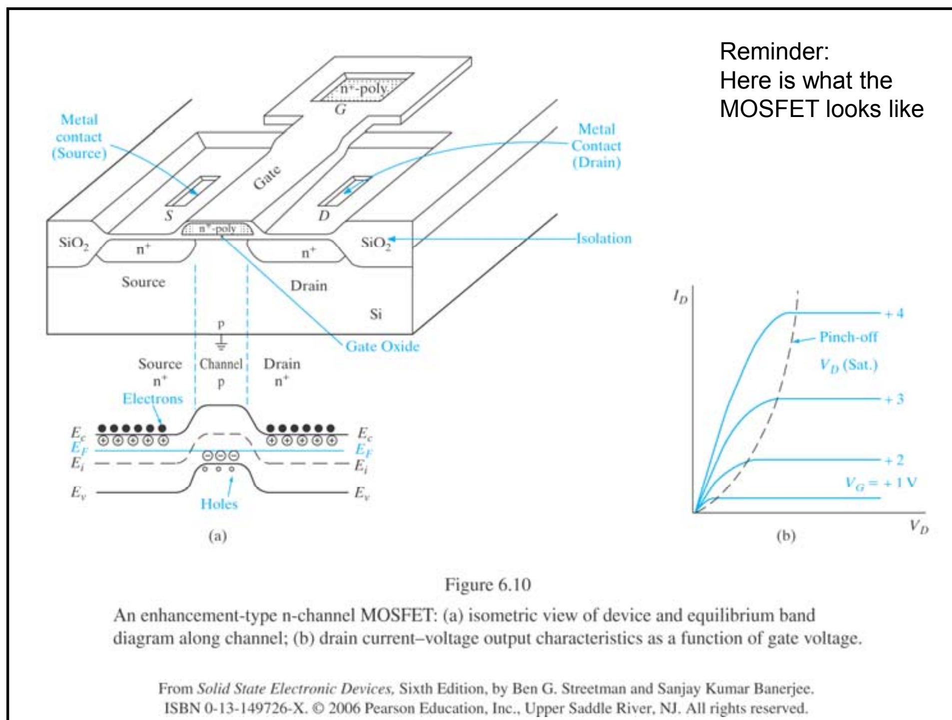

Figure 6.10

An enhancement-type n-channel MOSFET: (a) isometric view of device and equilibrium band diagram along channel; (b) drain current–voltage output characteristics as a function of gate voltage.

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N-channel MOSFETs:
Enhancement & Depletion modes

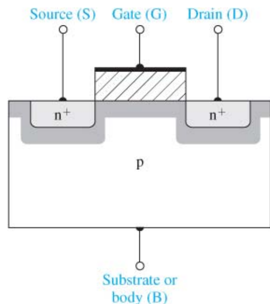


Figure 10.34 | Cross section and circuit symbol for an n-channel enhancement mode MOSFET.

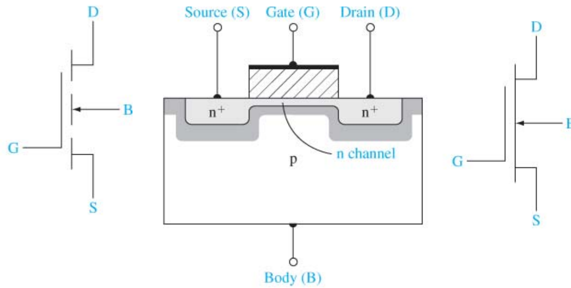
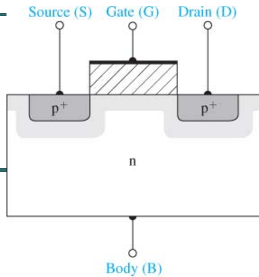


Figure 10.35 | Cross section and circuit symbol for an n-channel depletion mode MOSFET.

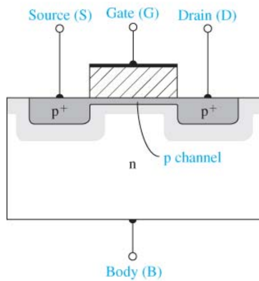
P-channel MOSFETs:

Enhancement & Depletion modes



D
B
G
S

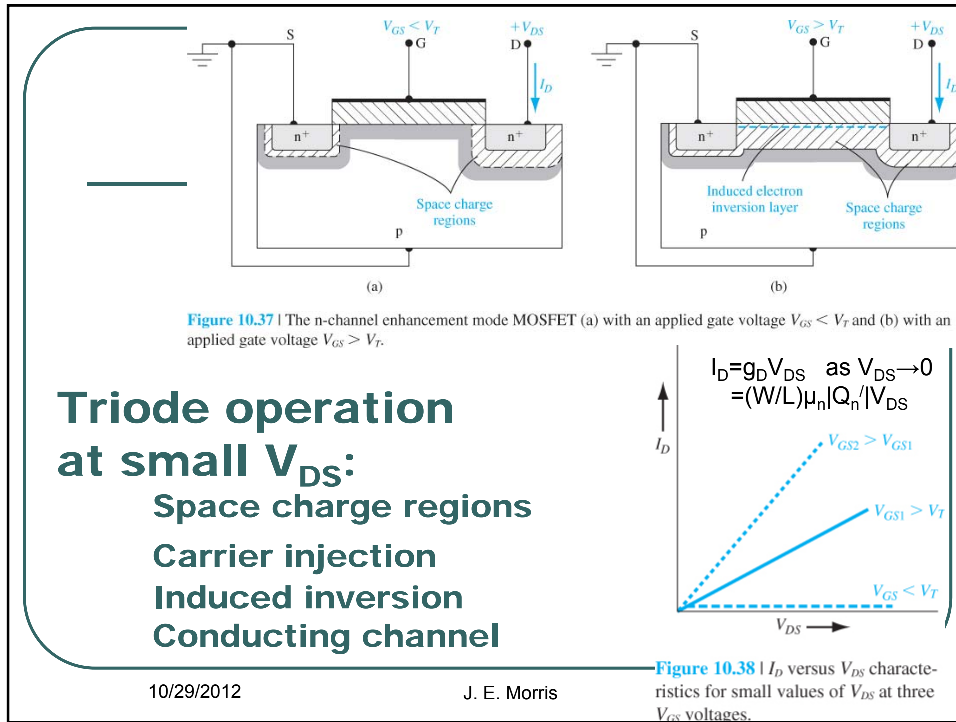
(a)



D
B
G
S

(b)

Figure 10.36 | Cross section and circuit symbol for (a) a p-channel enhancement mode MOSFET and (b) a p-channel depletion mode MOSFET.


S
$V_{GS} < V_T$
G
$+V_{DS}$
D
I_D
n+
n+
Space charge regions
p
(a)
S
$V_{GS} > V_T$
G
$+V_{DS}$
D
I_D
n+
n+
Induced electron inversion layer
Space charge regions
p
(b)
Figure 10.37 | The n-channel enhancement mode MOSFET (a) with an applied gate voltage $V_{GS} < V_T$ and (b) with an applied gate voltage $V_{GS} > V_T$.
Triode operation at small V_{DS}:
Space charge regions
Carrier injection
Induced inversion
Conducting channel
$I_D = g_D V_{DS}$ as $V_{DS} \to 0$
$= (W/L)\mu_n|Q_n'|V_{DS}$
I_D
$V_{GS2} > V_{GS1}$
$V_{GS1} > V_T$
$V_{GS} < V_T$
V_{DS}
Figure 10.38 | I_D versus V_{DS} characteristics for small values of V_{DS} at three V_{GS} voltages.
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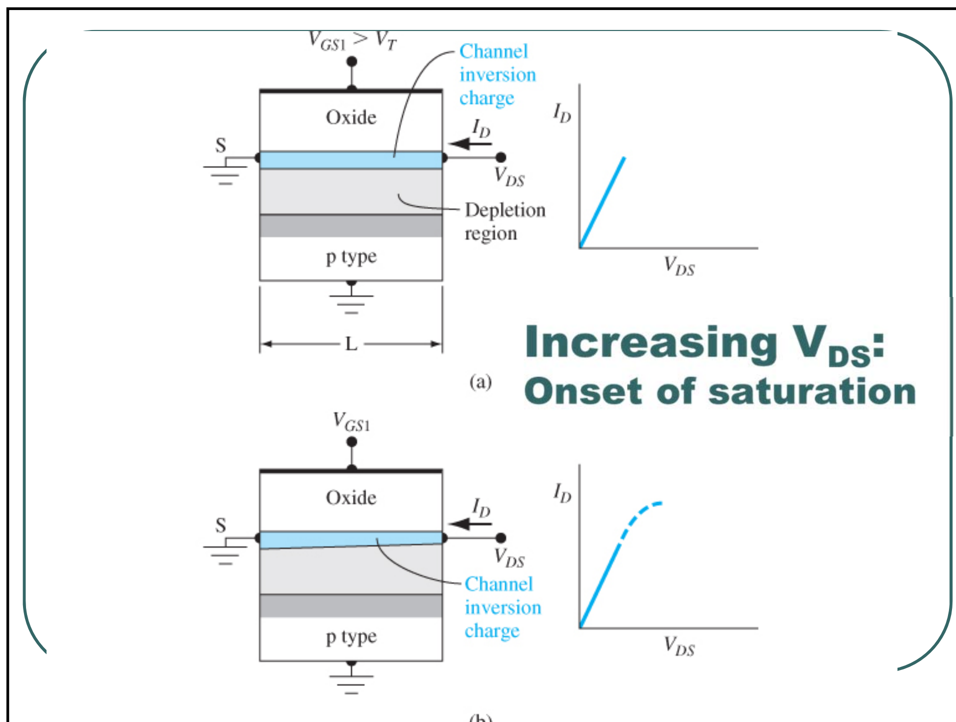

$V_{GS1} > V_T$
Channel inversion charge
Oxide
S
I_D
V_{DS}
Depletion region
p type
L
(a)
I_D
V_{DS}
Increasing V_{DS}:
Onset of saturation
V_{GS1}
Oxide
S
I_D
V_{DS}
Channel inversion charge
p type
I_D
V_{DS}

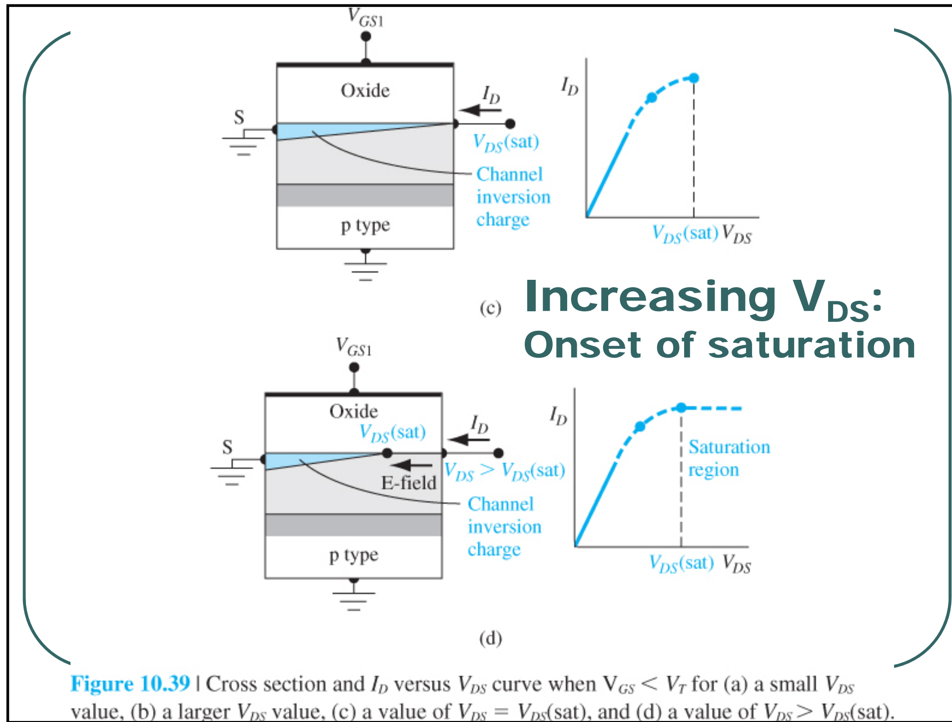
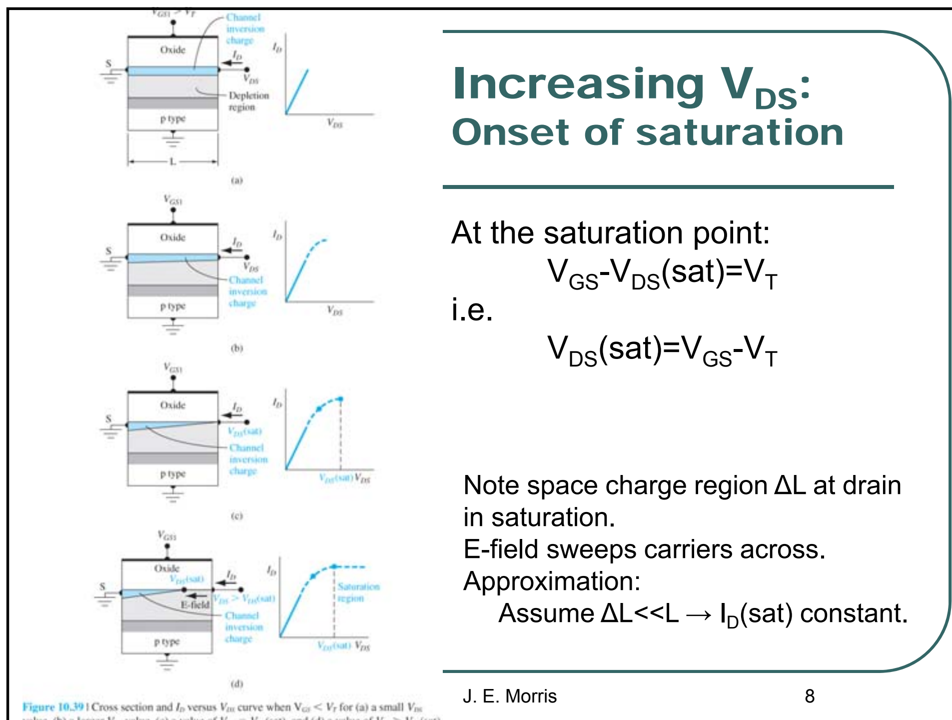


Figure 10.39 | Cross section and I_D versus V_{DS} curve when $V_{GS} < V_T$ for (a) a small V_{DS} value, (b) a larger V_{DS} value, (c) a value of $V_{DS} = V_{DS}$(sat), and (d) a value of $V_{DS} > V_{DS}$(sat).



N-channel MOSFET characteristics:

Note non-linear triode region

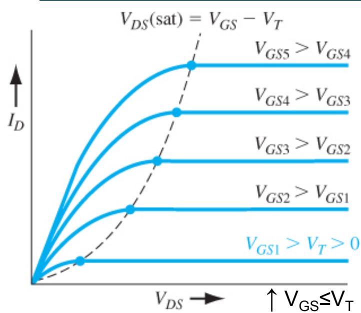


Figure 10.40 | Family of I_D versus V_{DS} curves for an n-channel enhancement mode MOSFET.

See later :

$$I_D = \frac{W\mu_n C_{ox}}{2L}\left[2(V_{GS} - V_T)V_{DS} - V_{DS}^2\right]$$

$$= \frac{k_n'}{2}\frac{W}{L}\left[2(V_{GS} - V_T)V_{DS} - V_{DS}^2\right]$$

$$= K_n\left[2(V_{GS} - V_T)V_{DS} - V_{DS}^2\right]$$

where $k_n' = \mu_n C_{ox}$ is the process conduction parameter

and $K_n = \frac{k_n'}{2}\frac{W}{L} = \frac{W\mu_n C_{ox}}{2L}$ is the conduction parameter

In saturation :

$$I_D = \frac{W\mu_n C_{ox}}{2L}(V_{GS} - V_T)^2$$

N-channel depletion mode

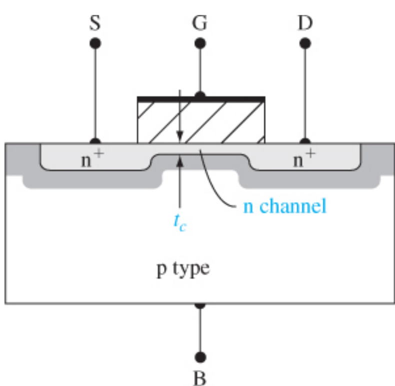


Figure 10.41 | Cross section of an n-channel depletion mode MOSFET.

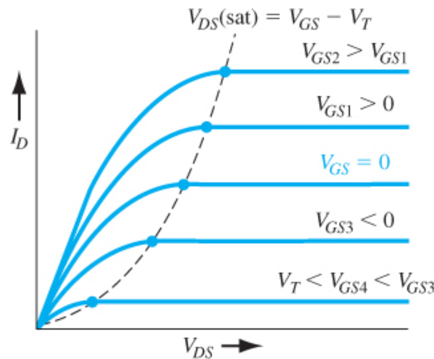


Figure 10.42 | Family of I_D versus V_{DS} curves for an n-channel depletion mode MOSFET.

I-V Characteristics

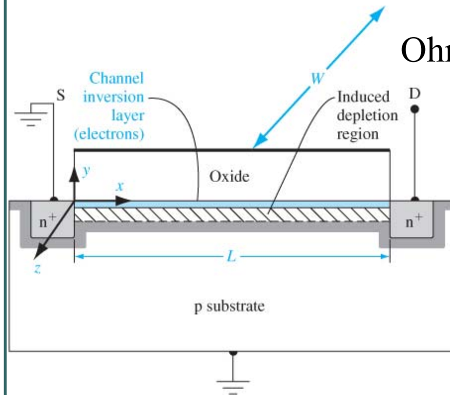


Figure 10.43 | Geometry of a MOSFET for I_D versus V_{DS} derivation.

Ohm's Law :

$$J_x = \sigma E_x = en\mu_n E_x$$

$$I_x = \int_y \int_z J_x dydz$$

$$= W\mu_n E_x e \int_y n(y)dy$$

$$= -W\mu_n Q_n^/ E_x$$

I_x, E_x $\Rightarrow$ constant along channel

I-V Characteristics: Charge neutrality

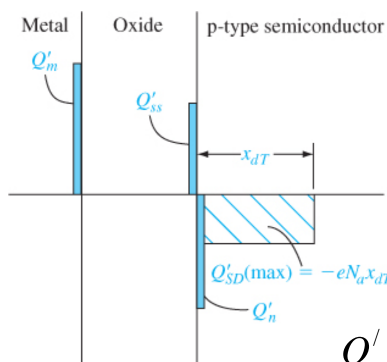


Figure 10.44 | Charge distribution in the n-channel enhancement mode MOSFET for $V_{GS} > V_T$.

$$Q_m^/ + Q_{ss}^/ + Q_n^/ + Q_{SD}^/(\text{max}) = 0$$

I-V Characteristics: Gauss's Law

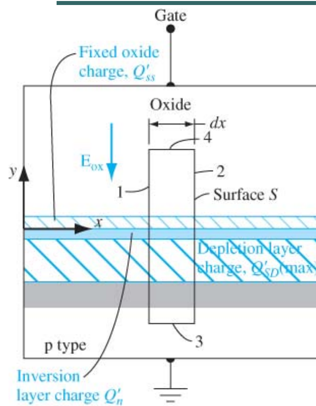


Figure 10.45 | Geometry for applying Gauss's law.

$$\oint_s \varepsilon E_n dS = -\varepsilon_{ox} E_{ox} W dx$$

$$= Q_T = \left[Q'_{ss} + Q'_n + Q'_{SD}(\max)\right] W dx$$

i.e.

$$-\varepsilon_{ox} E_{ox} = Q'_{ss} + Q'_n + Q'_{SD}(\max)$$

I-V Characteristics: Oxide field

V_x is channel potential (wrt S) at x

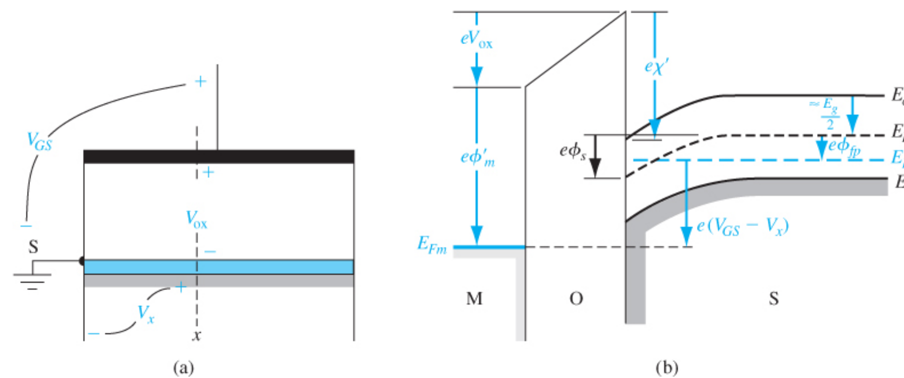


Figure 10.46 | (a) Potentials at a point *x* along the channel. (b) Energy-band diagram through the MOS structure at the point *x*.

I-V Characteristics: Oxide field

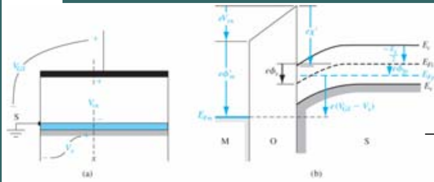


Figure 10.46 | (a) Potentials at a point x along the channel. (b) Energy-band diagram through the MOS structure at the point x.

$$E_{Fp} - E_{Fn} = e(V_{GS} - V_x)$$

$$= e\left[\left(\phi_m' + V_{ox}\right) - \left(\chi' + \frac{E_g}{2e} - \phi_s + \phi_{fp}\right)\right]$$

$$V_{GS} - V_x = V_{ox} + 2\phi_{fp} + \phi_{ms}$$

using $\phi_s = 2\phi_{fp}$ for inversion

Hence:

$$-\varepsilon_{ox}E_{ox} = \frac{-\varepsilon_{ox}}{t_{ox}}V_{ox} = \frac{-\varepsilon_{ox}}{t_{ox}}\left[\left(V_{GS} - V_x\right) - \left(\phi_{ms} + 2\phi_{fp}\right)\right]$$

$$= -C_{ox}\left[\left(V_{GS} - V_x\right) - \left(V_T + \frac{Q_{ss}' + Q_{SD}'(\max)}{C_{ox}}\right)\right]$$

$$= Q_{ss}' + Q_n' + Q_{SD}'(\max)$$

So $I_x = -W\mu_n E_x Q_n'$

$$= -W\mu_n\left(-\frac{dV_x}{dx}\right)\left(-C_{ox}\left[\left(V_{GS} - V_x\right) - V_T\right]\right)$$

$$= -W\mu_n C_{ox}\frac{dV_x}{dx}\left[\left(V_{GS} - V_x\right) - V_T\right]$$

I-V Characteristics: Final equations

$$I_x = -W\mu_n C_{ox}\frac{dV_x}{dx}\left[\left(V_{GS} - V_x\right) - V_T\right]$$

$$\int_0^L I_x dx = -W\mu_n C_{ox}\int_{V_x(0)}^{V_x(L)}\left[\left(V_{GS} - V_x\right) - V_T\right]dV_x$$

$$I_D = -I_x = \frac{W\mu_n C_{ox}}{L}\left[(V_{GS} - V_T)V_{DS} - \frac{1}{2}V_{DS}^2\right]$$

for $V_{GS} \geq V_T$ *and* $0 \leq V_{DS} \leq V_{DS}(sat)$

where $V_x(0) = 0$ & $V_x(L) = V_{DS}$

Max $I_D \Rightarrow \frac{\partial I_D}{\partial V_{DS}} = 0$

when $V_{GS} - V_T = V_{DS} = V_{DS}(sat)$

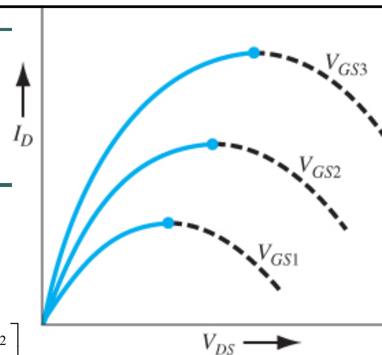


Figure 10.47 | Plots of I_D versus V_{DS} from Equation (10.62).

For $V_{DS} \geq V_{DS}(sat)$, $I_D = I_D(sat)$

$$= \frac{W\mu_n C_{ox}}{L}\left[(V_{GS} - V_T)V_{DS}(sat) - \frac{1}{2}V_{DS}(sat)^2\right]$$

$$= \frac{W\mu_n C_{ox}}{2L}(V_{GS} - V_T)^2$$

Ex 10.7 N-channel Si MOSFET: μ_n=650cm²/V-s, t_{ox}=8nm, W/L=12, V_T=0.40V. Find the drain current for (a) V_{GS}=0.8V, (b) V_{GS}=1.2V, & (c) V_{GS}=1.6V, if the transistor is biased in the saturation region.

We find $C_{ox} = \frac{\epsilon_{ox}}{t_{ox}} = \frac{(3.9)(8.85\times10^{-14})}{80\times10^{-8}} = 4.314\times10^{-7}$ F/cm^2

Then $k_n' = \mu_n C_{ox} = (650)(4.314\times10^{-7}) = 2.804\times10^{-4}$ A/V^2 or $k_n' = 0.2804$ mA/V^2

Now $I_D = \frac{k_n'}{2}\cdot\frac{W}{L}(V_{GS}-V_T)^2 = \frac{0.2804}{2}(12)(V_{GS}-0.4)^2$

(a) $I_D = (1.6826)(0.8-0.4)^2 = 0.269$ mA

(b) $I_D = (1.6826)(1.2-0.4)^2 = 1.077$ mA

(c) $I_D = (1.6826)(1.6-0.4)^2 = 2.423$ mA

$$I_D = \frac{W\mu_n C_{ox}}{L}\left[(V_{GS}-V_T)V_{DS} - \frac{1}{2}V_{DS}^{\ 2}\right] \quad \& \quad \mathrm{I_D} = \frac{W\mu_n C_{ox}}{2L}(V_{GS}-V_T)^2$$

$$I_D \approx \frac{W\mu_n C_{ox}}{L}(V_{GS}-V_T)V_{DS} \qquad \sqrt{\mathrm{I_D}} = \sqrt{\frac{W\mu_n C_{ox}}{2L}}(V_{GS}-V_T)$$

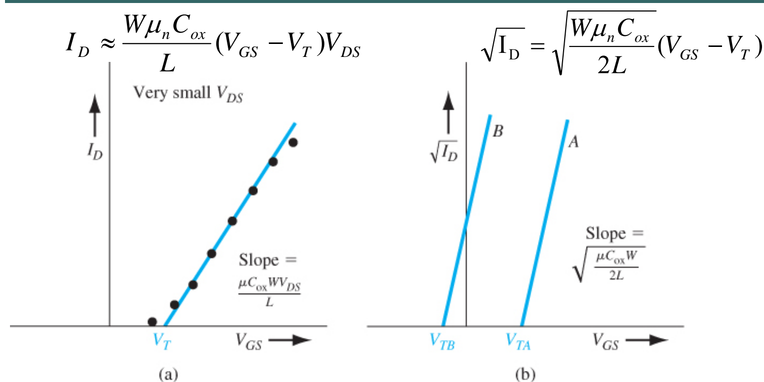


Figure 10.48 | (a) I_D versus V_{GS} (for small V_{DS}) for enhancement mode MOSFET. (b) Ideal $\sqrt{I_D}$ versus V_{GS} in saturation region for enhancement mode (curve A) and depletion mode (curve B) n-channel MOSFETs.

Ex 10.8 N-channel Si MOSFET: W=6μm, L=1.5μm, t_{ox}=8nm. When the transistor is biased in the saturation region, the drain current is I_D(sat)=0.132mA at V_{GS}=1.0V and I_D(sat)=0.295mA at V_{GS}=1.25V. Determine the electron mobility and threshold voltage.

We find $C_{ox} = \frac{\epsilon_{ox}}{t_{ox}} = \frac{(3.9)(8.85\times10^{-14})}{80\times10^{-8}} = 4.314\times10^{-7}$ F/cm^2

$I_D(sat) = \frac{W\mu_n C_{ox}}{2L}(V_{GS} - V_T)^2$ Then

$$\sqrt{I_{D2}(sat)} - \sqrt{I_{D1}(sat)} = \sqrt{\frac{W\mu_n C_{ox}}{2L}}(V_{GS2} - V_{GS1})$$

$\sqrt{0.295\times10^{-3}} - \sqrt{0.132\times10^{-3}} = 1.7176\times10^{-2} - 1.1489\times10^{-2} = 5.687\times10^{-3}$, Then

$5.687\times10^{-3} = \sqrt{\frac{(6)\mu_n(4.314\times10^{-7})}{2(1.5)}}(1.25-1.0)$ Or $\left(\frac{5.687\times10^{-3}}{0.25}\right)^2 = 8.628\times10^{-7}\cdot\mu_n$

$\Rightarrow \mu_n \cong 600$ cm^2/V-s

We now find

$0.132\times10^{-3} = \frac{(6)(600)(4.314\times10^{-7})}{2(1.5)}(1.0 - V_T)^2$ → $\left(\frac{0.132\times10^{-3}}{5.1768\times10^{-4}}\right)^{1/2} = 1.0 - V_T$

$V_T = 0.495$ V

P-channel

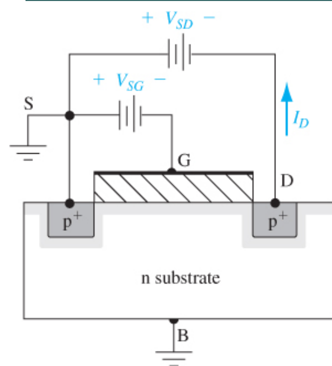


Figure 10.49 | Cross section and bias configuration for a p-channel enhancement mode MOSFET.

$$I_D = \frac{W\mu_p C_{ox}}{L}\left[(V_{SG} + V_T)V_{SD} - \frac{1}{2}V_{SD}^2\right]$$

$for\ \ 0 \le V_{SD} \le V_{SD}(sat)$

$$I_D(sat) = \frac{W\mu_p C_{ox}}{2L}(V_{SG} + V_T)^2$$

$for\ \ V_{SD} \ge V_{SD}(sat)$

Transconductances

$$g_m = \frac{\partial I_D}{\partial V_{GS}}$$

Triode region :

$$I_D = \frac{W\mu_n C_{ox}}{L}\left[(V_{GS} - V_T)V_{DS} - \frac{1}{2}V_{DS}^{\ 2}\right]$$

$$g_m = \frac{W\mu_n C_{ox}}{L} V_{DS}$$

Saturation region :

$$\mathrm{I_D} = \frac{W\mu_n C_{ox}}{2L}(V_{GS} - V_T)^2$$

$$g_m = \frac{W\mu_n C_{ox}}{L}(V_{GS} - V_T)$$

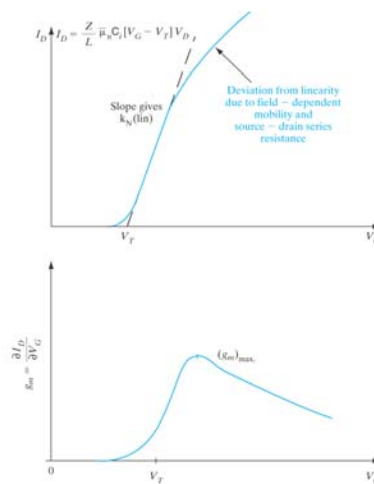


Figure 6.28

Linear region transfer characteristics: (a) plot of drain current versus gate voltage for MOSFETs in the linear region; (b) transconductance as a function of gate bias.

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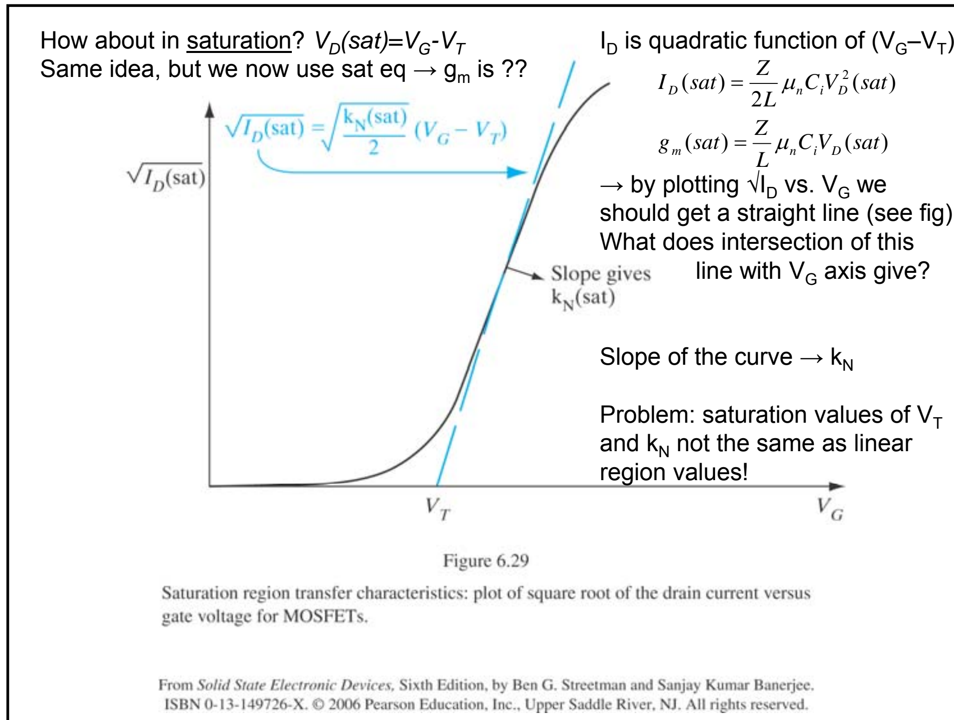
How about in saturation? $V_D(sat)=V_G-V_T$
Same idea, but we now use sat eq → g_m is ??
I_D is quadratic function of $(V_G–V_T)$
$I_D(sat) = \frac{Z}{2L}\mu_n C_i V_D^2(sat)$
$g_m(sat) = \frac{Z}{L}\mu_n C_i V_D(sat)$
→ by plotting $\sqrt{I_D}$ vs. V_G we should get a straight line (see fig)
What does intersection of this line with V_G axis give?
$\sqrt{I_D(sat)} = \sqrt{\frac{k_N(sat)}{2}}(V_G - V_T)$
$\sqrt{I_D(sat)}$
Slope gives $k_N(sat)$
Slope of the curve → k_N
Problem: saturation values of V_T and k_N not the same as linear region values!
V_T
V_G
Figure 6.29
Saturation region transfer characteristics: plot of square root of the drain current versus gate voltage for MOSFETs.
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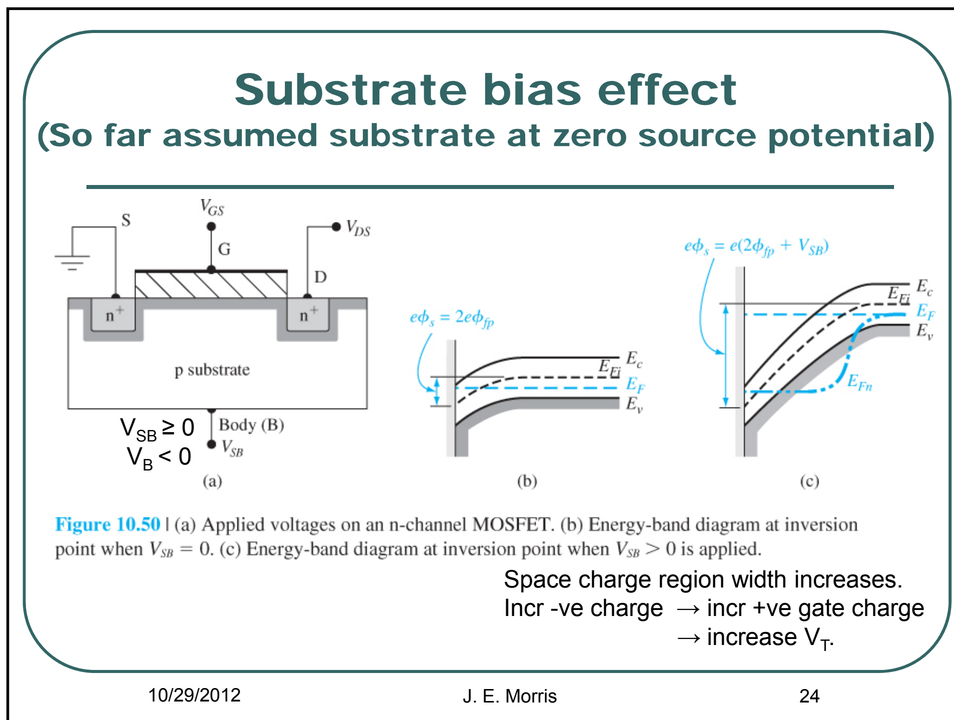
Substrate bias effect
(So far assumed substrate at zero source potential)
V_{GS}
S
G
D
V_{DS}
n^+
n^+
p substrate
Body (B)
V_{SB}
$V_{SB} \geq 0$
$V_B < 0$
$e\phi_s = 2e\phi_{fp}$
$e\phi_s = e(2\phi_{fp} + V_{SB})$
E_c
E_{Fi}
E_F
E_v
E_{Fn}
(a)
(b)
(c)
Figure 10.50 | (a) Applied voltages on an n-channel MOSFET. (b) Energy-band diagram at inversion point when $V_{SB} = 0$. (c) Energy-band diagram at inversion point when $V_{SB} > 0$ is applied.
Space charge region width increases.
Incr -ve charge → incr +ve gate charge
→ increase V_T.
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24

Substrate bias effect:
Body effect coefficient

$$V_{SB} = 0 \Rightarrow Q'_{SD}(\max) = -eN_a x_{dT} = -\sqrt{2e\varepsilon_s N_a (2\phi_{fp})}$$

$$V_{SB} > 0 \Rightarrow Q'_{SD} = -eN_a x_d = -\sqrt{2e\varepsilon_s N_a (2\phi_{fp} + V_{SB})}$$

$$\Delta Q'_{SD} = -\sqrt{2e\varepsilon_s N_a}\left[\sqrt{2\phi_{fp} + V_{SB}} - \sqrt{2\phi_{fp}}\right]$$

$$\Delta V_T = \frac{-\Delta Q'_{SD}}{C_{ox}}$$

$$= \frac{\sqrt{2e\varepsilon_s N_a}}{C_{ox}}\left[\sqrt{2\phi_{fp} + V_{SB}} - \sqrt{2\phi_{fp}}\right]$$

$$= \gamma\left[\sqrt{2\phi_{fp} + V_{SB}} - \sqrt{2\phi_{fp}}\right]$$

where γ is the body effect coefficient

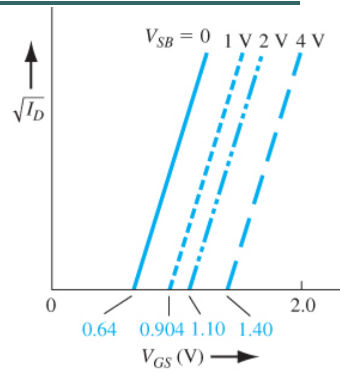

Figure 10.51 | Plots of $\sqrt{I_D}$ versus V_{GS} at several values of V_{SB} for an n-channel MOSFET.

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Ex 10.9 N-channel Si MOSFET: $N_a = 10^{16}/cm^3$, $t_{ox} = 12nm$. Find (a) body effect coefficient, & (b) the change in V_T for (a) $V_{SB} = 1V$ & (b) $V_{SB} = 2V$.

(a) $\phi_{fp} = V_t \ln\left(\frac{N_a}{n_i}\right) = (0.0259)\ln\left(\frac{10^{16}}{1.5\times10^{10}}\right) = 0.3473$ V

$C_{ox} = \frac{\epsilon_{ox}}{t_{ox}} = \frac{(3.9)(8.85\times10^{-14})}{120\times10^{-8}} = 2.876\times10^{-7}$ F/cm^2

$\gamma = \frac{\sqrt{2e\epsilon_s N_a}}{C_{ox}} = \frac{\sqrt{2(1.6\times10^{-19})(11.7)(8.85\times10^{-14})(10^{16})}}{2.876\times10^{-7}}$, $\gamma = 0.200$ V$^{1/2}$

(b) $\Delta V_T = \gamma\left[\sqrt{2\phi_{fp} + V_{SB}} - \sqrt{2\phi_{fp}}\right]$

(i) $\Delta V_T = (0.200)\left[\sqrt{2(0.3473)+1} - \sqrt{2(0.3473)}\right] = (0.200)[1.3018 - 0.8334]$

$\Delta V_T = 0.0937$ V

(ii) $\Delta V_T = (0.200)\left[\sqrt{2(0.3473)+2} - \sqrt{2(0.3473)}\right] = (0.200)[1.6415 - 0.8334]$

$\Delta V_T = 0.162$ V

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High frequency effects

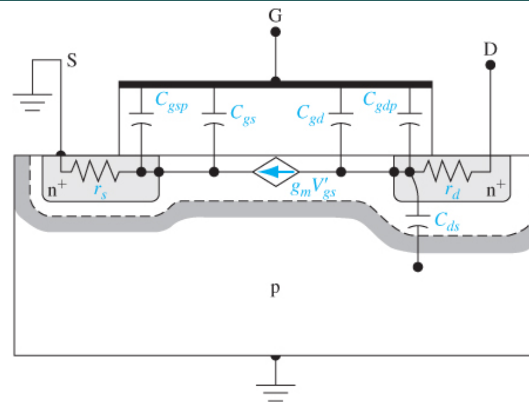

Figure 10.52 | Inherent resistances and capacitances in the n-channel MOSFET structure.

10/29/2012 J. E. Morris 27

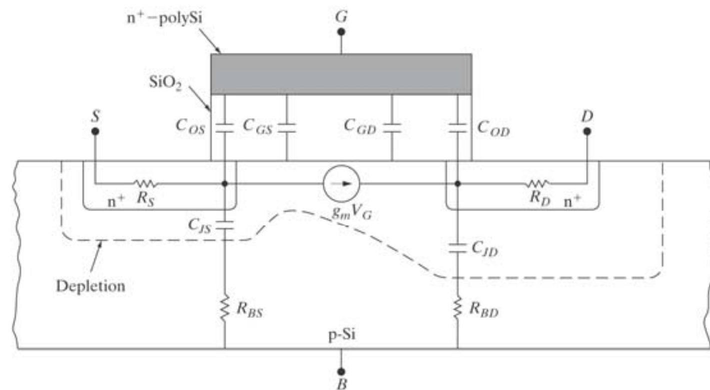

Figure 6.39

Equivalent circuit of a MOSFET, showing the passive capacitive and resistive components. The gate capacitance C_i is the sum of the distributed capacitances from the gate to the source end of the channel (C_{GS}) and the drain end (C_{GD}). In addition, we have an overlap capacitance (where the gate electrode overlaps the source/drain junctions) from the gate-to-source (C_{OS}) and gate-to-drain (C_{OD}). C_{OD} is also known as the Miller overlap capacitance. We also have p-n junction depletion capacitances associated with the source (C_{JS}) and drain (C_{JD}). The parasitic resistances include the source/drain series resistances (R_S and R_D), and the resistances in the substrate between the bulk contact and the source and drain (R_{BS} and R_{BD}). The drain current can be modeled as a (gate) voltage-controlled constant-current source.

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Small signal equivalent circuit

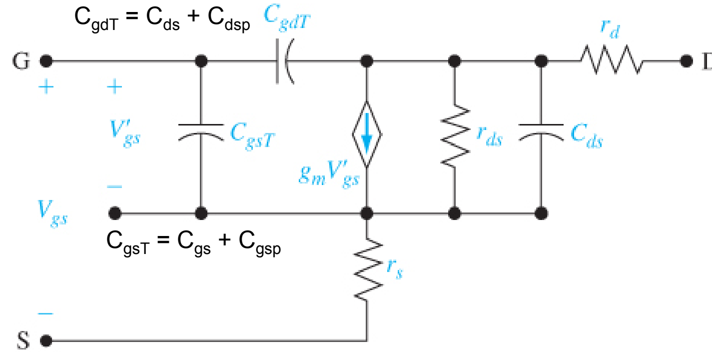


Figure 10.53 | Small-signal equivalent circuit of a common-source n-channel MOSFET.

Simplified small-signal models

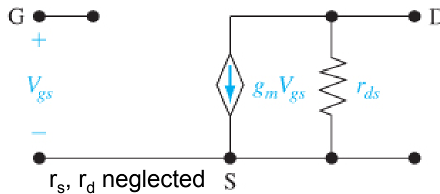
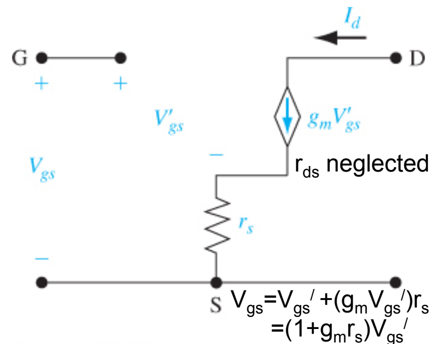


Figure 10.54 | Simplified, low-frequency small-signal equivalent circuit of a common-source n-channel MOSFET.



$V_{gs}=V_{gs}{}^{/}+(g_mV_{gs}{}^{/})r_s$
$=(1+g_mr_s)V_{gs}{}^{/}$

Figure 10.55 | Simplified, low-frequency small-signal equivalent circuit of common-source n-channel MOSFET including source resistance r_s.

Cutoff frequency

Channel transit time (L/v_{sat}) not usual limitation

Input : $I_i = j\omega C_{gsT} V_{gs} + j\omega C_{gdT}(V_{gs} - V_d)$

Output : $\frac{V_d}{R_L} + g_m V_{gs} + j\omega C_{gdT}(V_d - V_{gs}) = 0$

$$\Rightarrow I_i = j\omega\left[C_{gsT} + C_{gdT}\left(\frac{1+g_m R_L}{1+j\omega R_L C_{gdT}}\right)\right]V_{gs}$$

$$\approx j\omega\left[C_{gsT} + C_{gdT}(1+g_m R_L)\right]V_{gs} \quad \text{for } \omega << \frac{1}{R_L C_{gdT}}$$

Figure 10.56 | High-frequency small-signal equivalent circuit of common-source n-channel MOSFET.

Cutoff frequency/Miller capacitance

$$I_i \approx j\omega\left[C_{gsT} + C_{gdT}(1+g_m R_L)\right]V_{gs}$$
$$= j\omega\left[C_{gsT} + C_M\right]V_{gs} \text{ where } C_M = (1+g_m R_L)C_{gdT}$$

Figure 10.57 | Small-signal equivalent circuit including Miller capacitance.

$$\mathrm{I_d} = \mathrm{g_m V_{gs}}$$
$$I_i = j\omega\left[C_{gsT} + C_M\right]V_{gs}$$
$$\left|\frac{\mathrm{I_d}}{I_i}\right| = \frac{g_m}{\omega\left[C_{gsT} + C_M\right]}$$
$$\Rightarrow 1 \text{ at } \omega_T = \frac{g_m}{C_{gsT} + C_M} = \frac{g_m}{C_G}$$

In saturation :

$$\mathrm{C_{gd}} \to 0 \;\&\; C_{gs} \approx (WL)C_{ox}$$

$$\text{So } \mathrm{f_T} = \frac{g_m}{2\pi\, C_G} \approx \frac{\frac{W\mu_n C_{ox}}{L}(V_{GS} - V_T)}{2\pi(WL)C_{ox}} = \frac{\mu_n(V_{GS} - V_T)}{2\pi\, L^2}$$

Ex 10.10 N-channel Si MOSFET: μ_n=420cm²/V-s, t_{ox}=18nm, L=1.µm, W=24µm, V_T=0.40V. Find the cutoff frequency if the transistor is biased in the saturation region at V_{GS}=1.5V.

$$f_T = \frac{\mu_n (V_{GS} - V_T)}{2\pi L^2}$$

$$= \frac{(420)(1.5 - 0.4)}{2\pi (1.2 \times 10^{-4})^2} = 5.11 \times 10^9 \text{ Hz}$$

$$\Rightarrow f_T = 5.11 \text{ GHz}$$

CMOS structures

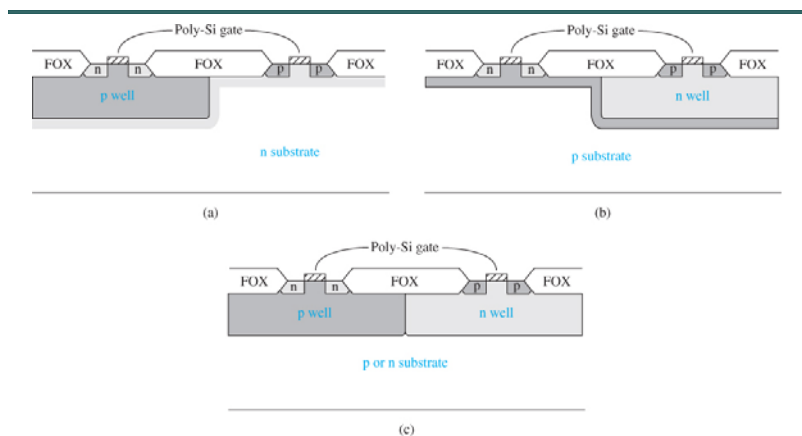


Figure 10.58 | CMOS structures: (a) p well, (b) n well, and (c) twin well.
(From Yang [22].)

CMOS inverter

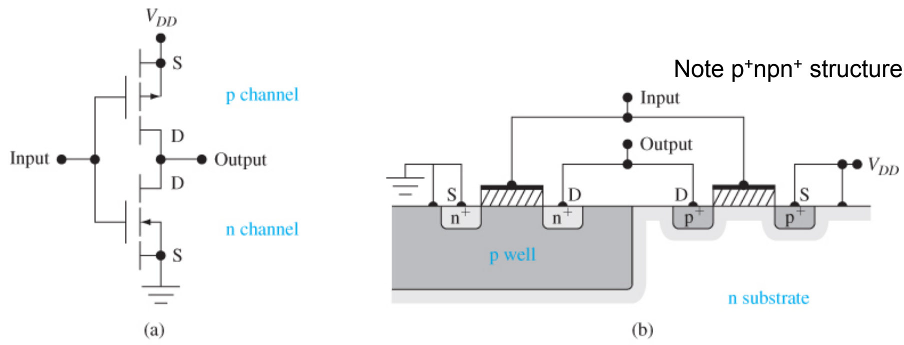


Figure 10.59 | (a) CMOS inverter circuit. (b) Simplified integrated circuit cross section of CMOS inverter.

CMOS p^+npn^+ structure: Latch-up

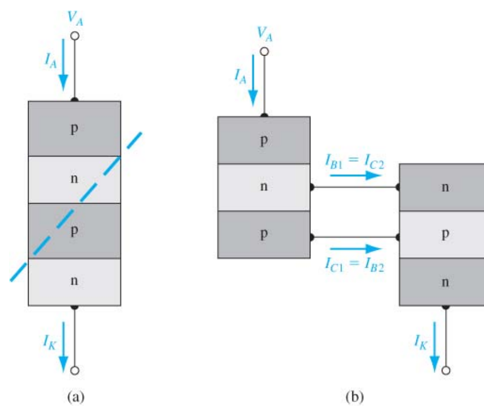


Figure 10.60 | (a) The splitting of the basic pnpn structure. (b) The two-transistor equivalent circuit of the four-layered pnpn device.

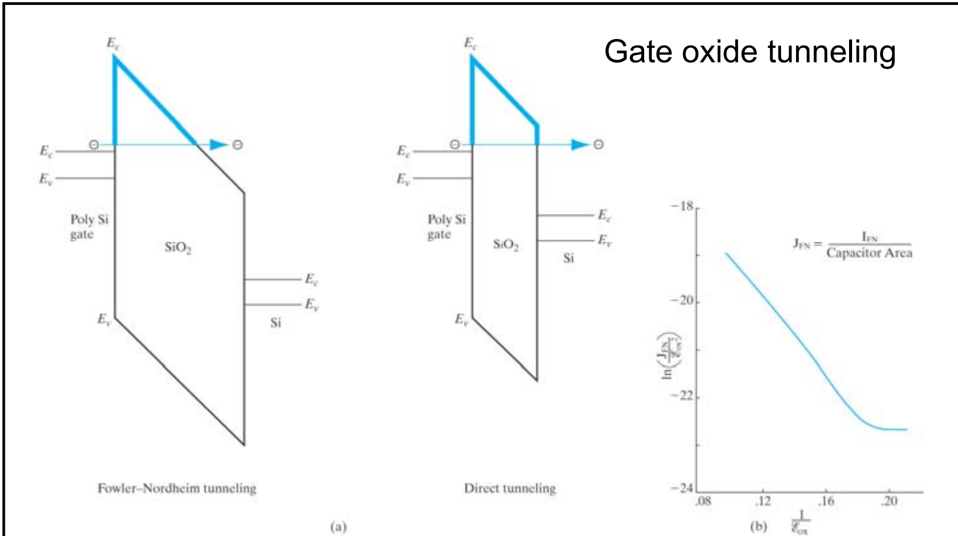


Figure 6.24

Current–voltage characteristics of gate oxides: (a) Fowler–Nordheim and direct tunneling through thin gate oxides; (b) plot of Fowler–Nordheim tunneling leakage current as a function of electric field across the oxide.

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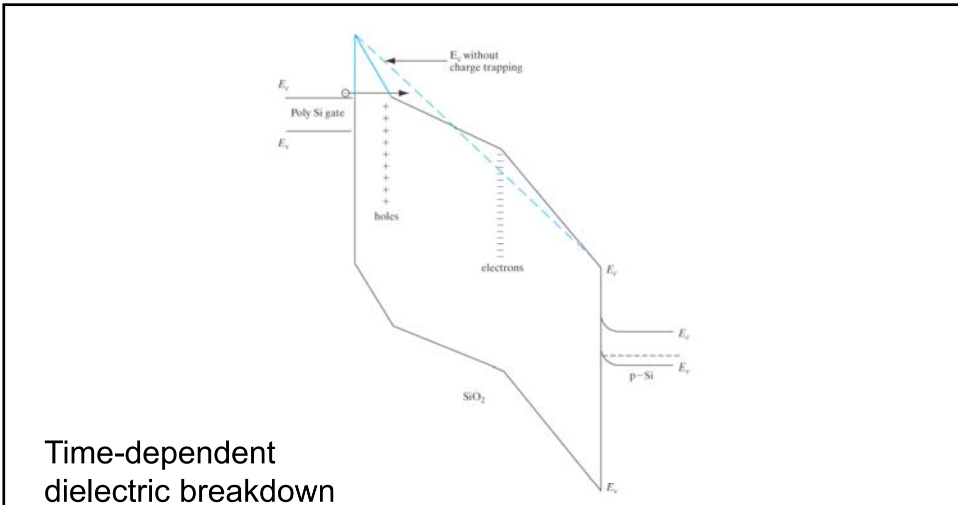

Figure 6.25

Time-dependent dielectric breakdown of oxides: Band diagram of a MOS device showing the band edges in the polysilicon gate, oxide, and Si substrate. Trapped holes and electrons in the oxide distort the band edges, and increase the electric field in the oxide near the gate. The tunneling barrier width is seen to be less than if there were no charge trapping (dashed line).

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