EE415/515 Fundamentals of Semiconductor Devices Fall 2012

Lecture 10: MOS Capacitor (Chapter 10.1, 10.2)

MOS capacitor

Assume p-type substrate, i.e. N-channel device

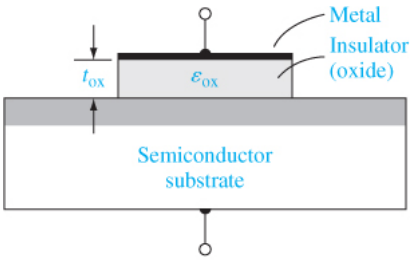


Figure 10.1 | The basic MOS capacitor structure.

Capacitance/unit area $C' = \frac{\varepsilon_{ox}}{t_{ox}}$

Charge/unit area $Q' = C'V$

Metal "gate"

MOS=metal-oxide-semiconductor

Negative gate bias

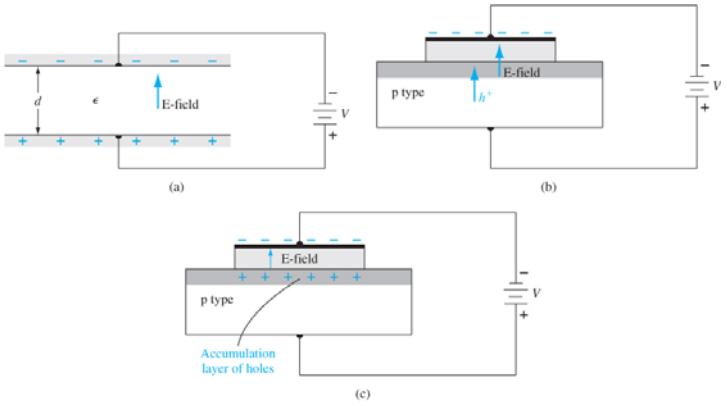


Figure 10.2 | (a) A parallel-plate capacitor showing the electric field and conductor charges. (b) A corresponding MOS capacitor with a negative gate bias showing the electric field and charge flow. (c) The MOS capacitor with an accumulation layer of holes.

Positive gate bias

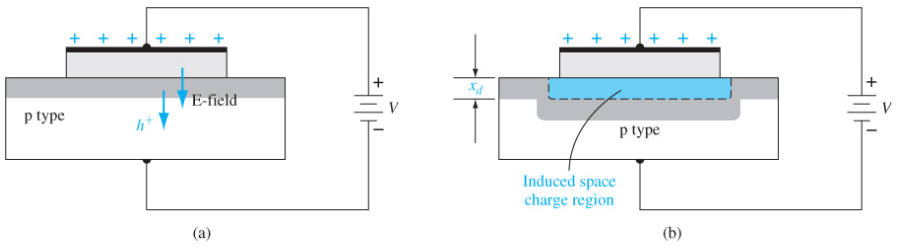
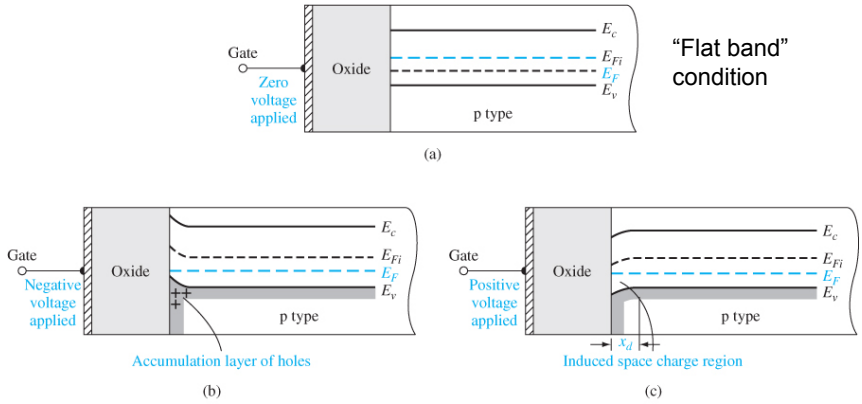


Figure 10.3 | The MOS capacitor with a moderate positive gate bias, showing (a) the electric field and charge flow and (b) the induced space charge region.

Negative space charge region is depleted of holes
→ immobile negative acceptor ions

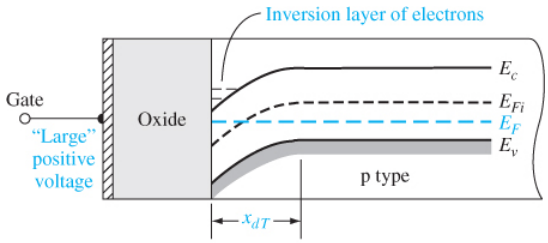
Band-bending with applied bias: accumulation & depletion regions



"Flat band" condition

Figure 10.4 | The energy-band diagram of a MOS capacitor with a p-type substrate for (a) a zero applied gate bias showing the *ideal* case, (b) a negative gate bias, and (c) a moderate positive gate bias.

Increased positive bias: "Inversion"



"Inversion" layer:

$E_F > E_{Fi}$ → n-type
→ electrons

"N-channel"

Figure 10.5 | The energy-band diagram of the MOS capacitor with a p-type substrate for a "large" positive gate bias.

N-type substrate

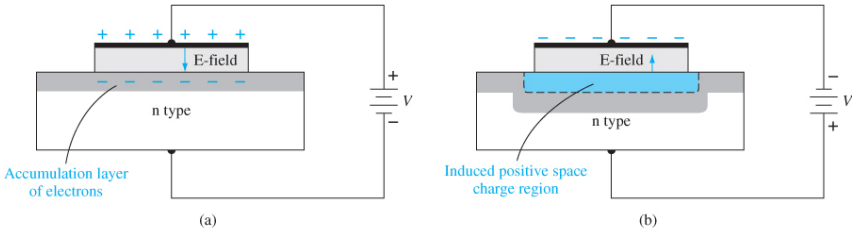


Figure 10.6 | The MOS capacitor with an n-type substrate for (a) a positive gate bias and (b) a moderate negative gate bias.

Accumulation, depletion, & p-channel inversion

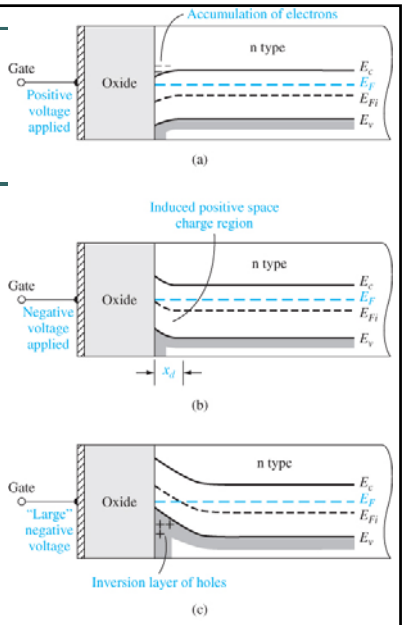
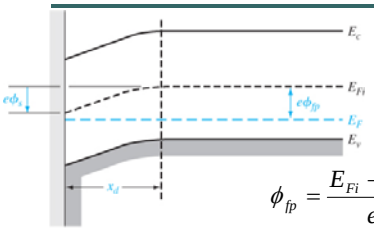


Figure 10.7 | The energy-band diagram of the MOS capacitor with an n-type substrate for (a) a positive gate bias, (b) a moderate negative bias, and (c) a "large" negative gate bias.

Surface potential φ_s, depletion width, & inversion



$$\phi_{fp} = \frac{E_{Fi} - E_F}{e} = \frac{kT}{e}\ln\frac{N_a}{n_i}$$

Figure 10.8 | The energy-band diagram in the p-type semiconductor, indicating surface potential.

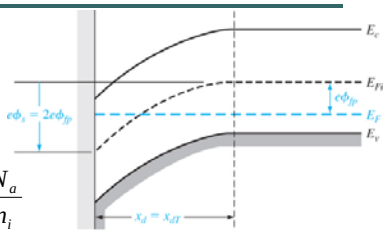


Figure 10.9 | The energy-band diagram in the p-type semiconductor at the threshold inversion point.

ϕ_s = potential across space charge layer

Compare one - sided pn junction : $x_d = \sqrt{\frac{2\varepsilon_s\phi_s}{eN_a}}$

Define the "inversion threshold" when $\phi_s = 2\phi_{fp}$

Inversion threshold $\Rightarrow$ threshold gate voltage

At threshold : inversion region width

$$x_{dT} = \sqrt{\frac{4\varepsilon_s\phi_{fp}}{eN_a}} = \sqrt{\frac{4\varepsilon_s}{eN_a}\frac{kT}{e}\ln\frac{N_a}{n_i}}$$

Increase bias beyond threshold :

x_{dT} changes little

ϕ_s & surface electron density incr

Ex 10.1 Find x_{dT} for an oxide to p-type Si junction at 300K with N_a=2x10^{15}/cm^3. Does x_{dT} increase or decrease as N_a increases?

$$\phi_{fp} = V_t \ln\left(\frac{N_a}{n_i}\right) = (0.0259)\ln\left(\frac{2\times10^{15}}{1.5\times10^{10}}\right)$$

$$= 0.3056\ \text{V}$$

$$x_{dT} = \left\{\frac{4\in_s \phi_{fp}}{eN_a}\right\}^{1/2}$$

$$= \left\{\frac{4(11.7)(8.85\times10^{-14})(0.3056)}{(1.6\times10^{-19})(2\times10^{15})}\right\}^{1/2}$$

$$x_{dT} = 6.29\times10^{-5}\ \text{cm}$$

or $x_{dT} = 0.629\ \mu\text{m}$

P-channel inversion threshold

$$\phi_{fn} = \frac{kT}{e}\ln\frac{N_d}{n_i} \qquad x_{dT} = \sqrt{\frac{4\varepsilon_s\phi_{fn}}{eN_d}}$$

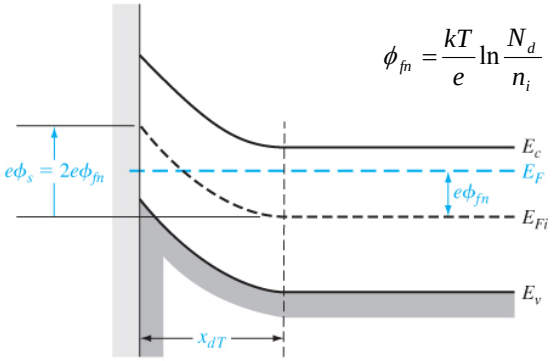


Figure 10.10 | The energy-band diagram in the n-type semiconductor at the threshold inversion point.

x_{dT} variation with N_a, N_d

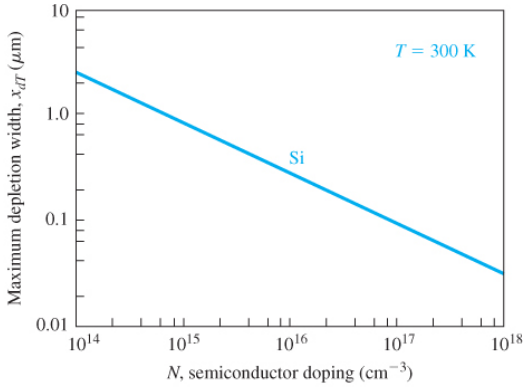


Figure 10.11 | Maximum induced space charge region width versus semiconductor doping.

Surface charge density

Electron concentration $n = n_i \exp\frac{E_F - E_{Fi}}{kT}$

so electron inversion charge density

$$n_s = n_i \exp\frac{e(\phi_{fp} + \Delta\phi_s)}{kt}$$

$$= n_i \exp\frac{e\phi_{fp}}{kt} \exp\frac{e\Delta\phi_s}{kt} = n_{st} \exp\frac{e\Delta\phi_s}{kt}$$

where $n_{st} = n_i \exp\frac{e\phi_{fp}}{kt}$

= electron concentration at threshold,

and $\Delta\phi_s = \phi_s - 2\phi_{fp}$

Note n_s incr rapidly with φ_s (gate voltage), so x_{dT} approx constant

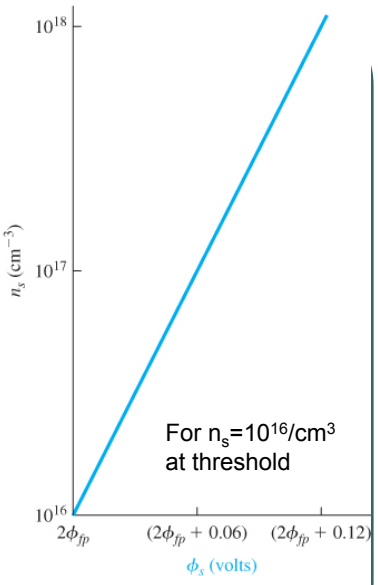


Figure 10.12 | Electron inversion charge density as a function of surface potential.

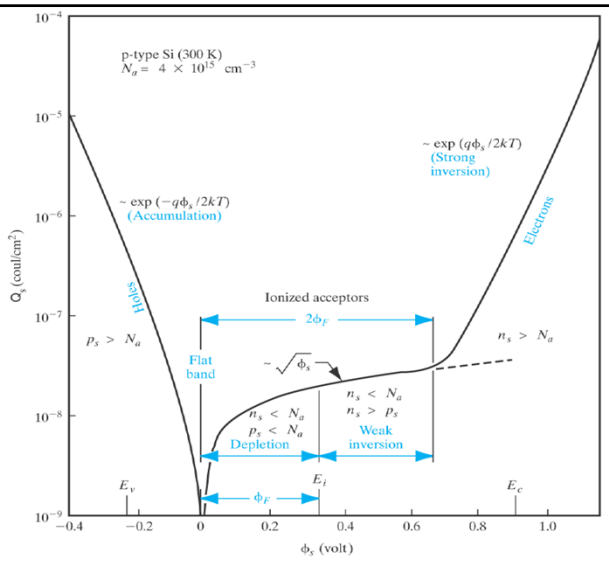


Figure 6.14

Variation of space-charge density in the semiconductor as a function of the surface potential ϕ_S for p-type silicon with $N_a = 4 \times 10^{15}$ cm^{-3} at room temperature. p_S and n_S are the hole and electron concentrations at the surface, ϕ_F is the potential difference between the Fermi level and the intrinsic level of the bulk. (Garrett and Brattain, Phys. Rev., 99, 376 (1955).)

Work function effects

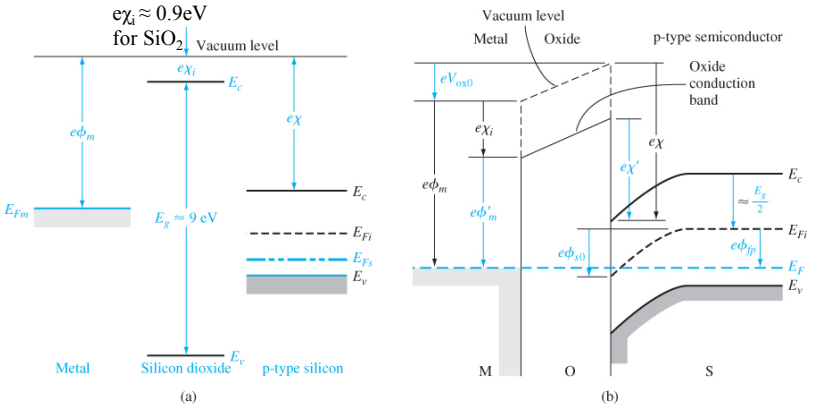


Figure 10.13 | (a) Energy levels in a MOS system prior to contact and (b) energy-band diagram through the MOS structure in thermal equilibrium after contact.

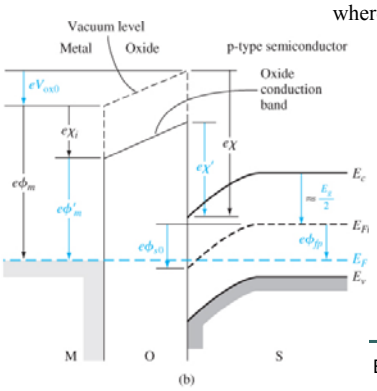
Φ_m' & χ' "modified" for e- injection into oxide conduction band

Work function effects

$$(e\phi_m' + e\chi_i) + eV_{ox0} = (e\chi' + e\chi_i) + \frac{E_g}{2} - (e\phi_{s0} - e\phi_{fp})$$

i.e. $$V_{ox0} + \phi_{s0} = -\left[\phi_m' - \left(\chi' + \frac{E_g}{2e} + \phi_{fp}\right)\right] = -\phi_{ms}$$

where ϕ_{ms} is the metal - semiconductor work function difference



Ex 10.2 Find φ_{ms} for Al-SiO_2 φ_m'=3.20V and Si-SiO_2 χ'=3.25eV. Assume E_g=1.12eV and $N_a=10^{16}/cm^3$.

$$\phi_{fp} = V_t \ln\left(\frac{N_a}{n_i}\right) = (0.0259)\ln\left(\frac{10^{16}}{1.5\times10^{10}}\right)$$
$$= 0.347\ \text{V}$$
$$\phi_{ms} = \left[\phi_m' - \left(\chi' + \frac{E_g}{2e} + \phi_{fp}\right)\right]$$
$$= [3.20 - (3.25 + 0.56 + 0.347)]$$
$$\phi_{ms} = -0.957\ \text{V}$$

(Degenerate) polysilicon gates

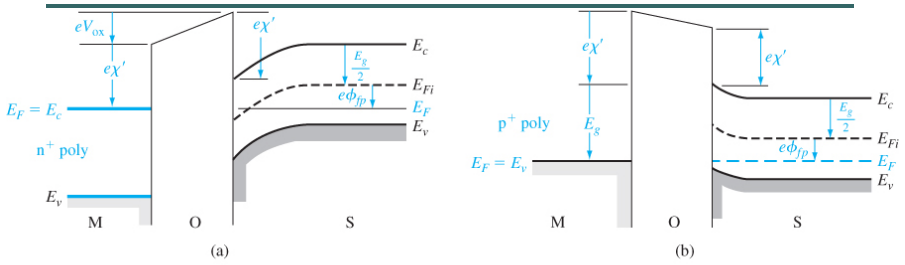


Figure 10.14 | Energy-band diagram through the MOS structure with a p-type substrate at zero gate bias for (a) an n^+ polysilicon gate and (b) a p^+ polysilicon gate.

Degenerate $\rightarrow E_F = E_c$ or E_v In practice, E_F possibly 0.1 - 0.2eV above E_c or below E_v

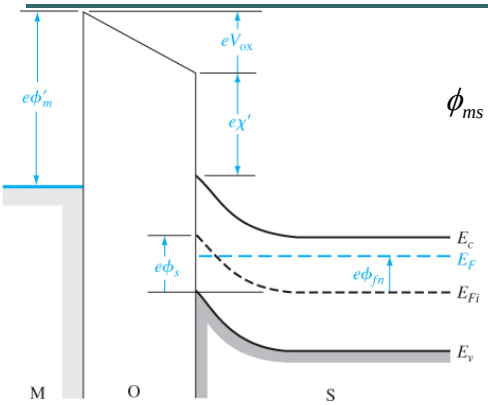
n^+polysilicon :

$$\phi_{ms} = \left[\chi' - \left(\chi' + \frac{E_g}{2e} + \phi_{fp}\right)\right] = -\left(\frac{E_g}{2e} + \phi_{fp}\right)$$

p^+polysilicon :

$$\phi_{ms} = \left[\left(\chi' + \frac{E_g}{e}\right) - \left(\chi' + \frac{E_g}{2e} + \phi_{fp}\right)\right] = \left(\frac{E_g}{2e} - \phi_{fp}\right)$$

N-type substrate (negative bias)



$$\phi_{ms} = \phi'_m - \left(\chi' + \frac{E_g}{2e} + \phi_{fn} \right)$$

Figure 10.15 | Energy-band diagram through the MOS structure with an n-type substrate for a negative applied gate bias.

Φ_{ms} vs substrate doping for various gate materials

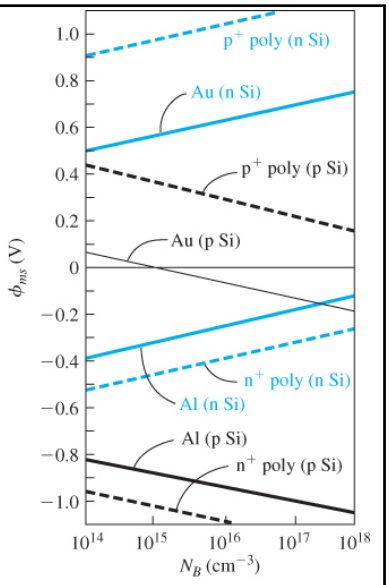


Figure 10.16 | Metal–semiconductor work function difference versus doping for aluminum, gold, and n^- and p^- polysilicon gates.
(From Sze [17] and Werner [20].)

Flat band voltage

(=gate voltage for zero semiconductor band bending i.e. for zero net space charge)

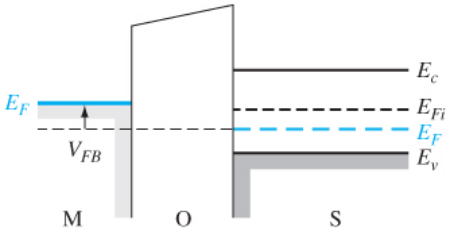


Figure 10.17 | Energy-band diagram of a MOS capacitor at flat band.

For zero gate voltage :

$$V_{ox0} + \phi_{s0} = -\phi_{ms}$$

For gate voltage $V_G = \Delta V_{ox} + \Delta\phi_s$

$$= (V_{ox} - V_{ox0}) + (\phi_s - \phi_{s0})$$

$$= V_{ox} + \phi_s + \phi_{ms}$$

Oxide charge

May have Q'_{ss}/unit area trapped charge

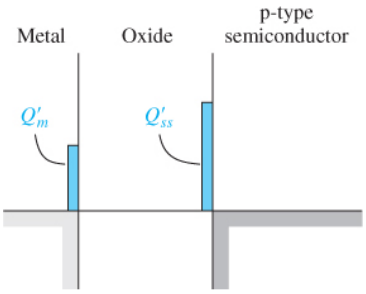


Figure 10.18 | Charge distribution in a MOS capacitor at flat band.

For zero net oxide charge at flat band :

$$Q'_m + Q'_{ss} = 0, \text{ i.e. } C_{ox} V_{ox} + Q'_{ss} = 0$$

$$\text{i.e. } V_{ox} = \frac{-Q'_{ss}}{C_{ox}} \text{ and } V_G \Rightarrow V_{FB} = \phi_{ms} - \frac{Q'_{ss}}{C_{ox}}$$

since $\phi_s = 0$ at the flat band condition

Ex 10.3 Find V_{FB} for a MOS capacitor with a n+ poly-Si gate and N_a=2x10^{15}/cm^3, t_{ox}=4nm, Q'_{ss}=2x10^{10}e/cm^2. What is φ_{ms}?

From Figure 10.16, $\phi_{ms} \cong -1.03$ V

$$C_{ox} = \frac{\epsilon_{ox}}{t_{ox}} = \frac{(3.9)(8.85\times10^{-14})}{40\times10^{-8}}$$

$$= 8.629\times10^{-7}\ \text{F/cm}^2$$

Then

$$V_{FB} = \phi_{ms} - \frac{Q'_{ss}}{C_{ox}}$$

$$= -1.03 - \frac{(2\times10^{10})(1.6\times10^{-19})}{8.629\times10^{-7}}$$

$$V_{FB} = -1.034\ \text{V}$$

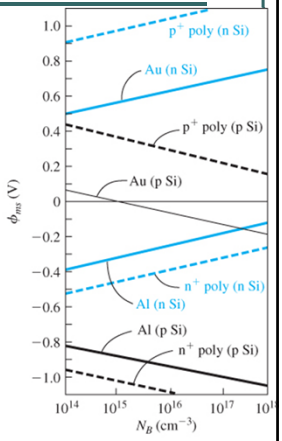
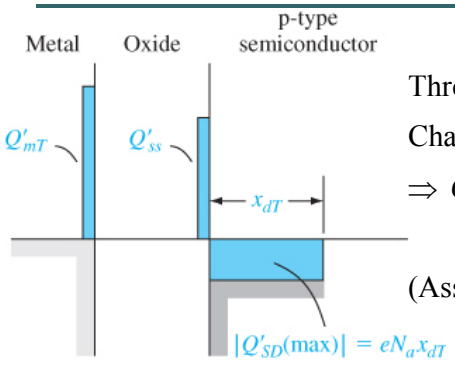


Figure 10.16 | Metal–semiconductor work function difference versus doping for aluminum, gold, and n$^-$ and p$^-$ polysilicon gates.
(From Sze [17] and Werner [20].)

Threshold voltage
=gate voltage for the inversion threshold



Threshold : $\phi_s = 2\phi_{fn}$ or $2\phi_{fp}$

Charge conservation

$$\Rightarrow Q'_{mT} + Q'_{ss} = \left|Q'_{SD}(\text{max})\right| = eN_a x_{dT}$$

(Assumes : inversion electron density = 0 at the threshold)

Figure 10.19 | Charge distribution in a MOS capacitor with a p-type substrate at the threshold inversion point.

Threshold voltage

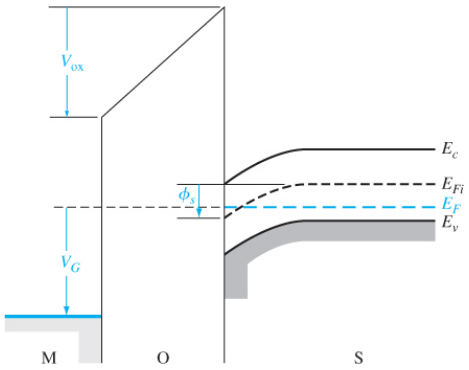


Figure 10.20 | Energy-band diagram through the MOS structure with a positive applied gate bias.

$$V_G = \Delta V_{ox} + \Delta\phi_s = V_{ox} + \phi_s + \phi_{ms}$$

$$V_{TN} = V_{oxT} + 2\phi_{fp} + \phi_{ms}$$

$$= \frac{Q'_{mT}}{C_{ox}} + 2\phi_{fp} + \phi_{ms}$$

$$= \frac{|Q'_{SD}(\max)|}{C_{ox}} - \frac{Q'_{ss}}{C_{ox}} + 2\phi_{fp} + \phi_{ms}$$

$$= \frac{t_{ox}}{\varepsilon_{ox}}\left(|Q'_{SD}(\max)| - Q'_{ss}\right) + 2\phi_{fp} + \phi_{ms}$$

$$= V_{FB} + \frac{|Q'_{SD}(\max)|}{C_{ox}} + 2\phi_{fp}$$

Ex 10.4 Find φ_{ms} & V_{TN} for Si MOS device at 300K with a p^+ polysilicon gate, N_a=2x10^{16}/cm^3, t_{ox}=8nm, Q'_{ss}=2x10^{10}/cm^2.

From Figure 10.16, $\phi_{ms} \cong +0.28$ V

We find

$$\phi_{fp} = V_t \ln\left(\frac{N_a}{n_i}\right) = (0.0259)\ln\left(\frac{2\times10^{16}}{1.5\times10^{10}}\right)$$

$$= 0.3653\,\text{V}$$

$$x_{dT} = \left\{\frac{4\in_s \phi_{fp}}{eN_a}\right\}^{1/2}$$

$$= \left\{\frac{4(11.7)(8.85\times10^{-14})(0.3653)}{(1.6\times10^{-19})(2\times10^{16})}\right\}^{1/2}$$

$$= 2.174\times10^{-5}\,\text{cm}$$

$$|Q'_{SD}(\max)| = eN_a x_{dT}$$

$$= (1.6\times10^{-19})(2\times10^{16})(2.1744\times10^{-5})$$

$$= 6.958\times10^{-8}\,\text{C/cm}^2$$

Then

$$V_{TN} = \left(|Q'_{SD}(\max)| - Q'_{ss}\right)\left(\frac{t_{ox}}{\in_{ox}}\right) + \phi_{ms} + 2\phi_{fp}$$

$$= \frac{\left[(6.958\times10^{-8}) - (1.6\times10^{-19})(2\times10^{10})\right](80\times10^{-8})}{(3.9)(8.85\times10^{-14})} + 0.28 + 2(0.3653)$$

$$V_{TN} = 0.1539 + 0.28 + 2(0.3653)$$

$$= 1.16\,\text{V}$$

Depletion/enhancement modes

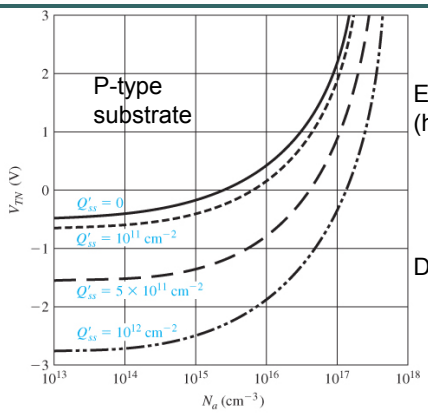
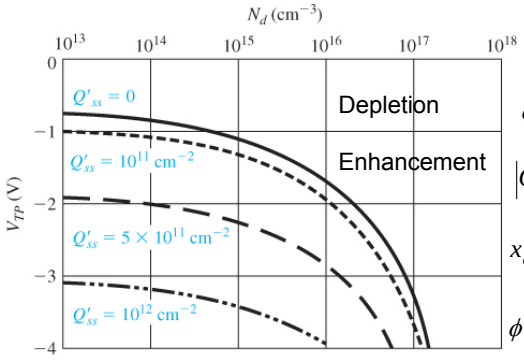


Figure 10.21 | Threshold voltage of an n-channel MOSFET versus the p-type substrate doping concentration for various values of oxide trapped charge (t_{ox} = 500 Å, aluminum gate).

N-type substrate

$$V_{TP} = \frac{t_{ox}}{\varepsilon_{ox}}\left(-\left|Q'_{SD}(\max)\right| - Q'_{ss}\right) - 2\phi_{fn} + \phi_{ms}$$



$$\phi_{ms} = \phi'_m - \left(\chi' + \frac{E_g}{2} - \phi_{fn}\right)$$

$$\left|Q'_{SD}(\max)\right| = eN_d x_{dT}$$

$$x_{dT} = \sqrt{\frac{4\varepsilon_s \phi_{fn}}{eN_d}}$$

$$\phi_{fn} = \frac{kT}{e}\ln\frac{N_d}{n_i}$$

Figure 10.22 | Threshold voltage of a p-channel MOSFET versus the n-type substrate doping concentration for various values of oxide trapped charge (t_{ox} = 500 Å, aluminum gate).

Ex 10.5 Find V_{TN} for n-type Si/SiO_2 MOS capacitor at 300K for: p^+ poly-Si gate, N_d=2x10^{16}/cm^3, t_{ox}=20nm, Q'_{ss}=5x10^{10}/cm^2. Determine the threshold voltage. Is it a depletion or enhancement mode device?

From Figure 10.16, $\phi_{ms} \cong 1.06$ V

We find

$$\phi_{fn} = V_t \ln\left(\frac{N_d}{n_i}\right) = (0.0259)\ln\left(\frac{2\times10^{16}}{1.5\times10^{10}}\right)$$

$$= 0.3653\,\text{V}$$

$$x_{dT} = \left\{\frac{4 \in_s \phi_{fn}}{eN_d}\right\}^{1/2}$$

$$= \left\{\frac{4(11.7)(8.85\times10^{-14})(0.3653)}{(1.6\times10^{-19})(2\times10^{16})}\right\}^{1/2}$$

$$= 2.174\times10^{-5}\,\text{cm}$$

$$|Q'_{SD}(\max)| = eN_d\phi_{fn}$$

$$= (1.6\times10^{-19})(2\times10^{16})(2.1744\times10^{-5})$$

$$= 6.958\times10^{-8}\,\text{C/cm}^2$$

Now

$$V_{TP} = \left[-|Q'_{SD}(\max)| - Q'_{ss}\right]\cdot\left(\frac{t_{ox}}{\in_{ox}}\right) + \phi_{ms} - 2\phi_{fn}$$

$$= \frac{\left[-(6.958\times10^{-8}) - (5\times10^{10})(1.6\times10^{-19})\right](200\times10^{-8})}{(3.9)(8.85\times10^{-14})} + 1.06 - 2(0.3653)$$

$$V_{TP} = -0.4495 + 1.06 - 2(0.3653)$$

or $V_{TP} = -0.12$ V

Capacitance-Voltage Characteristics:

Accumulation, depletion, & inversion modes

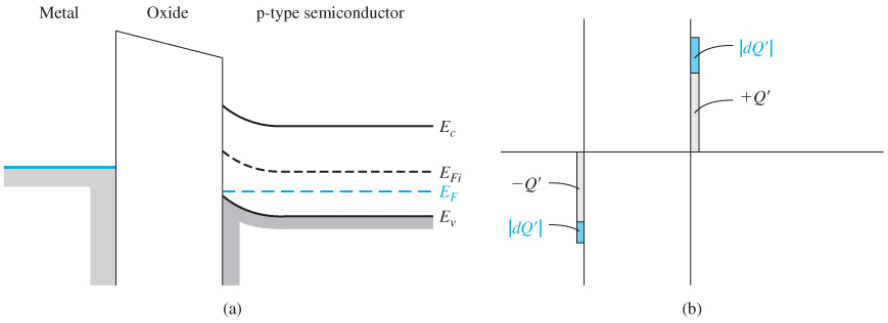


Figure 10.23 | (a) Energy-band diagram through a MOS capacitor for the accumulation mode. (b) Differential charge distribution at accumulation for a differential change in gate voltage.

$$C'(accumul) = C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}}$$

C-V Depletion mode

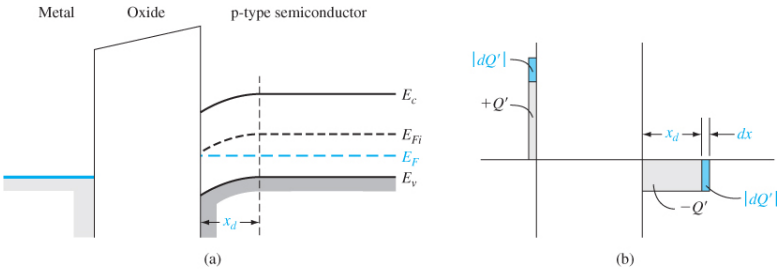


Figure 10.24 | (a) Energy-band diagram through a MOS capacitor for the depletion mode. (b) Differential charge distribution at depletion for a differential change in gate voltage.

$$\frac{1}{C'(depl)} = \frac{1}{C_{ox}} + \frac{1}{C'_{SD}}$$

$$\Rightarrow C'(depl) = \frac{C_{ox}C'_{SD}}{C_{ox}+C'_{SD}} = \frac{C_{ox}}{1+\frac{C_{ox}}{C'_{SD}}} = \frac{\varepsilon_{ox}}{t_{ox}+\frac{\varepsilon_{ox}}{\varepsilon_s}x_d} \quad \text{since } C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}} \ \& \ C'_{SD} = \frac{\varepsilon_s}{x_d}$$

C-V Inversion mode

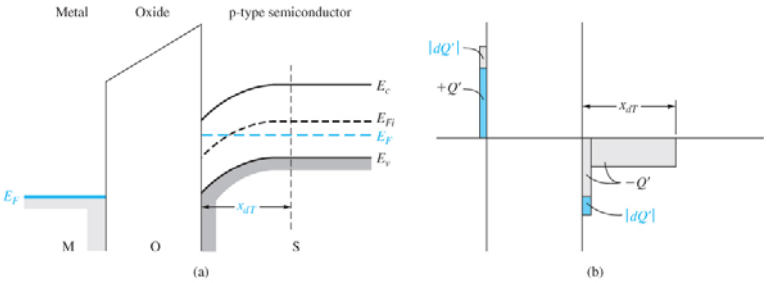
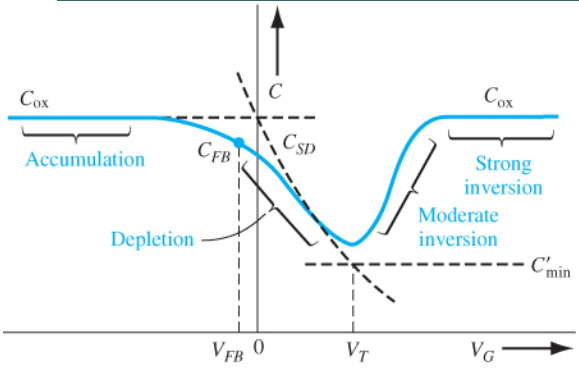


Figure 10.25 | (a) Energy-band diagram through a MOS capacitor for the inversion mode. (b) Differential charge distribution at inversion for a low-frequency differential change in gate voltage.

At inversion, x reaches its maximum, and C(depl) reaches a minimum $\Rightarrow C'_{\min} = \dfrac{\varepsilon_{ox}}{t_{ox}+\frac{\varepsilon_{ox}}{\varepsilon_s}x_{dT}}$

and at strong inversion $x_d = x_{dT}$ does not change and $C'(inv) = \dfrac{\varepsilon_{ox}}{t_{ox}}$

C-V characteristics



$$C'_{FB} = \frac{\varepsilon_{ox}}{t_{ox} + \frac{\varepsilon_{ox}}{\varepsilon_s}\sqrt{\frac{kT}{e}\cdot\frac{\varepsilon_s}{eN_a}}}$$

Figure 10.26 | Ideal low-frequency capacitance versus gate voltage of a MOS capacitor with a p-type substrate. Individual capacitance components are also shown.

Ex 10.6 MOS capacitor: n^+ poly-Si gate, N_a=3x10^{16}/cm^3, t_{ox}=8nm, Q'_{ss}=2x10^{10}/cm^2. Find C'_{min}/C_{ox} & C'_{FB}/C_{ox}.

$$C_{ox} = \frac{\epsilon_{ox}}{t_{ox}} = \frac{(3.9)(8.85\times10^{-14})}{80\times10^{-8}}$$
$$= 4.314\times10^{-7}\ \text{F/cm}^2$$
$$\phi_{fp} = (0.0259)\ln\left(\frac{3\times10^{16}}{1.5\times10^{10}}\right) = 0.3758\ \text{V}$$
$$x_{dT} = \left\{\frac{4(11.7)(8.85\times10^{14})(0.3758)}{(1.6\times10^{-19})(3\times10^{16})}\right\}^{1/2}$$
$$= 1.80\times10^{-5}\ \text{cm}$$

Now

$$C'_{min} = \frac{\epsilon_{ox}}{t_{ox} + \left(\frac{\epsilon_{ox}}{\epsilon_s}\right)\cdot x_{dT}}$$
$$= \frac{(3.9)(8.85\times10^{-14})}{80\times10^{-8} + \left(\frac{3.9}{11.7}\right)(1.80\times10^{-5})}$$
$$= 5.076\times10^{-8}\ \text{F/cm}^2$$

We find

$$\frac{C'_{min}}{C_{ox}} = \frac{5.076\times10^{-8}}{4.314\times10^{-7}} = 0.1177$$

Now

$$C'_{FB} = \frac{\epsilon_{ox}}{t_{ox} + \left(\frac{\epsilon_{ox}}{\epsilon_s}\right)\sqrt{\frac{V_t\,\epsilon_s}{eN_a}}}$$
$$= \frac{(3.9)(8.85\times10^{-14})}{80\times10^{-8} + \left(\frac{3.9}{11.7}\right)\sqrt{\frac{(0.0259)(11.7)(8.85\times10^{-14})}{(1.6\times10^{-19})(3\times10^{16})}}}$$
$$C'_{FB} = 2.174\times10^{-7}\ \text{F/cm}^2$$

We find

$$\frac{C'_{FB}}{C_{ox}} = \frac{2.174\times10^{-7}}{4.314\times10^{-7}} = 0.504$$

C-V for n-type substrate (p-channel)

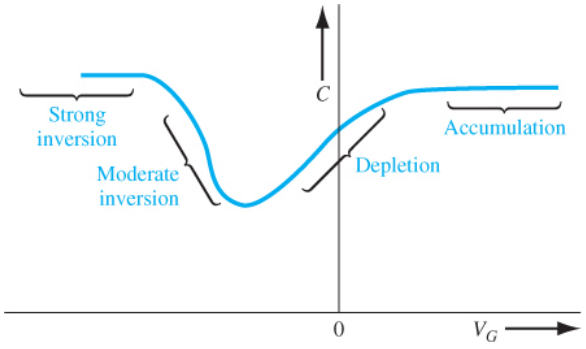


Figure 10.27 | Ideal low-frequency capacitance versus gate voltage of a MOS capacitor with an n-type substrate.

Low/high frequency

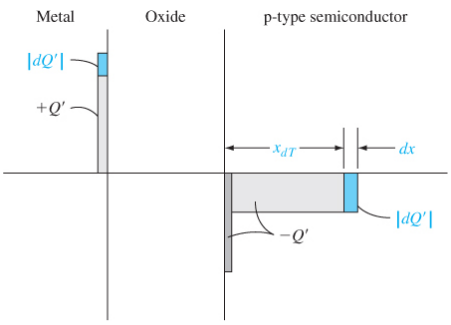


Figure 10.28 | Differential charge distribution at inversion for a high-frequency differential change in gate voltage.

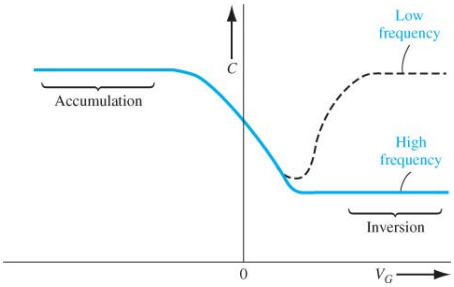
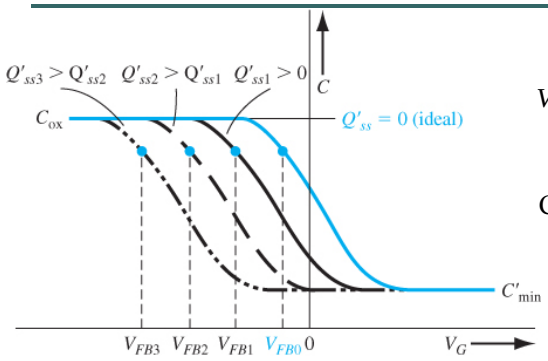


Figure 10.29 | Low-frequency and high-frequency capacitance versus gate voltage of a MOS capacitor with a p-type substrate.

At high frequencies, inversion electrons cannot respond, so $C \rightarrow C_{min}$
(Inversion electrons come from minority carrier diffusion from p-type or EHP generation)

Effect of fixed oxide charges Q'_{ss}



$$V_{FB} = \phi_{ms} - \frac{Q'_{ss}}{C_{ox}}$$

Curves (V_{FBB}) move with Q'_{ss}

Figure 10.30 | High-frequency capacitance versus gate voltage of a MOS capacitor with a p-type substrate for several values of effective trapped oxide charge.

Interface charge effects

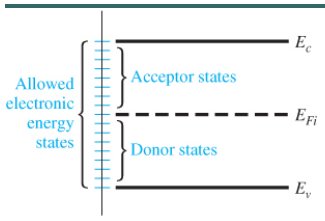


Figure 10.31 | Schematic diagram showing interface states at the oxide–semiconductor interface.

Interface states:

- Negative charge on acceptor states if $E<E_F$
- Positive charge on donor states if $E>E_F$

Charge can flow between substrate and states

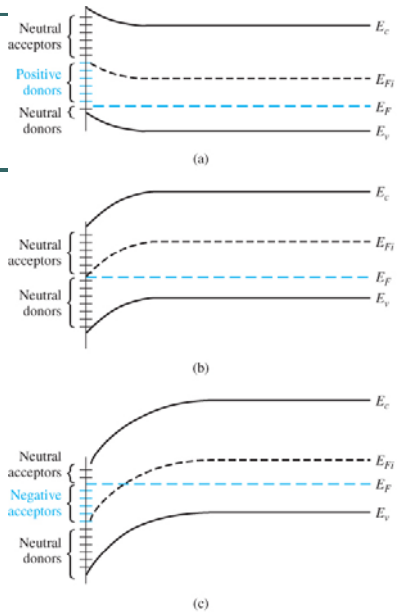


Figure 10.32 | Energy-band diagram in a p-type semiconductor showing the charge trapped in the interface states when the MOS capacitor is biased (a) in accumulation, (b) at midgap, and (c) at inversion.

Effect of interface states on C-V

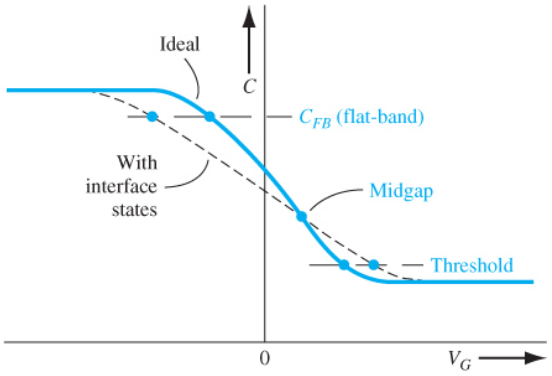


Figure 10.33 | High-frequency C–V characteristics of a MOS capacitor showing effects of interface states.

Assignment #5

9.4	10.7
9.15	10.17
9.27	10.24
9.29	10.30