ECE414/514 Electronics Packaging

Spring 2012 Lecture 5

Electrical C: Transmission lines (Transmission line reflections)

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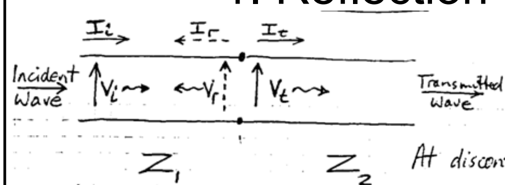
Lecture topics

- Reflection concepts
- Reflection coefficients
- Basic cases:
  - Matched and open circuit
- Generalized mismatches
  - Source and load
- Bounce chart/lattice diagram
- Reflections from discontinuities
- EMI and EMC

Objectives

- Understand origins of reflections
- Determine reflection waveforms by bounce chart
- Calculate effects of discontinuities
- Calculate EM radiation and susceptibility in basic case

1. Reflection Coefficient



At discontinuity $Z_1 \rightarrow Z_2$
and the relationships of the incident wave $V_i = I_i Z_1$ cannot be maintained in the transmitted wave $V_t = I_t Z_2$ without changes in V, I. Solution requires reflected wave $V_r = I_r Z_1$

Boundary conditions $V_i + V_r = V_t$

$I_i - I_r = I_t$

Gives $V_r = \frac{Z_2 - Z_1}{Z_2 + Z_1} V_i = \Gamma_V V_i$

(Voltage) Reflection Coefficient

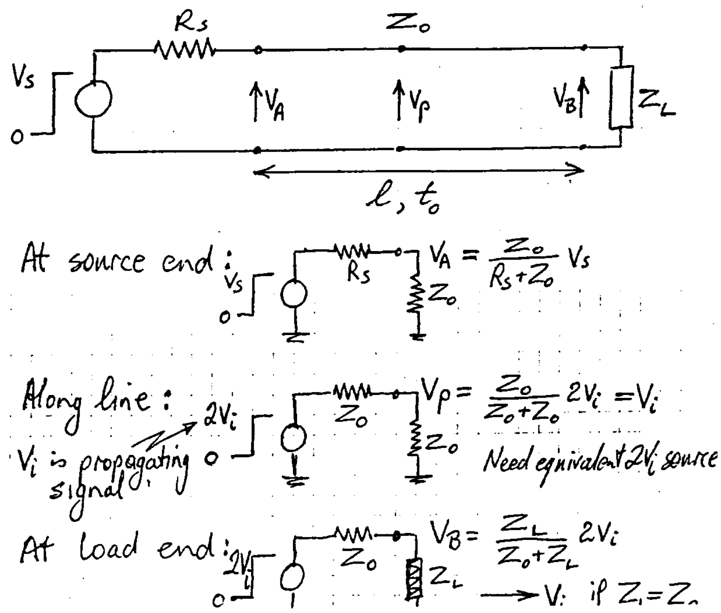
& $I_r = \Gamma_I I_i = -\Gamma_V I_i$

(Current) Reflection Coefficient

Voltage transmission coefficient $V_t / V_i = 1 + \Gamma_V$

Voltage reflection at Load $\Gamma_{VL} = \frac{Z_L - Z_o}{Z_L + Z_o} \rightarrow 0$ for $Z_L = Z_o = R_o$

" " " source $\Gamma_{VS} = \frac{R_S - Z_o}{R_S + Z_o} \rightarrow 0$ for $R_S = Z_o$



2. Basic examples

- 3 significant cases: Γ_{VL}= (R_L-Z_0)/ (R_L+Z_0)
  - Matched load $R_L = Z_0 \rightarrow \Gamma_{VL} = 0$
  - Open circuit load $R_L = \infty \rightarrow \Gamma_{VL} = +1$
  - Short circuit load $R_L = 0 \rightarrow \Gamma_{VL} = -1$
- Similarly at the source end:
  - Γ_{VS}= (R_S-Z_0)/ (R_S+Z_0) $R_S = Z_0 \rightarrow \Gamma_{VS} = 0$
  - $R_S = \infty \rightarrow \Gamma_{VS} = +1$ $R_S = 0 \rightarrow \Gamma_{VS} = -1$

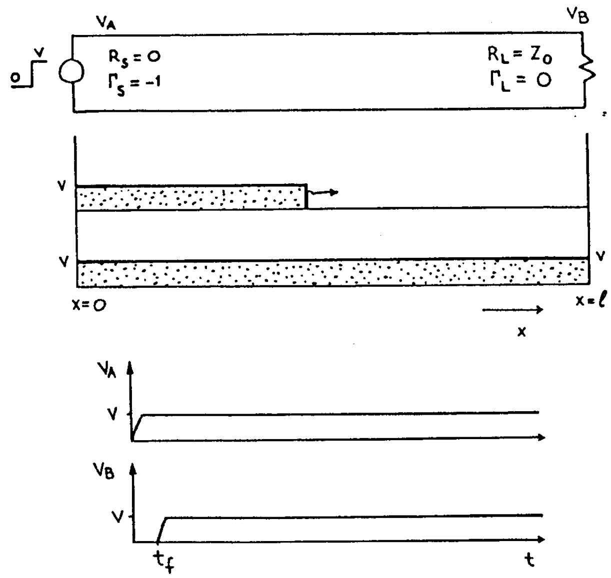


FIGURE 6.17 Termination at the receiving end: $R_S = 0$, $R_L = Z_0$

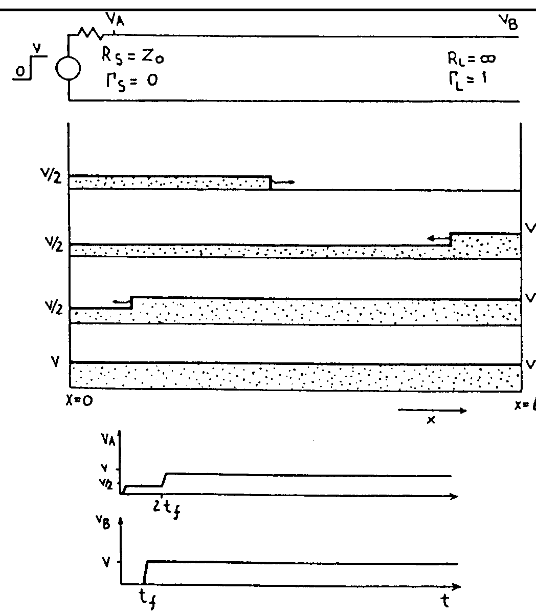
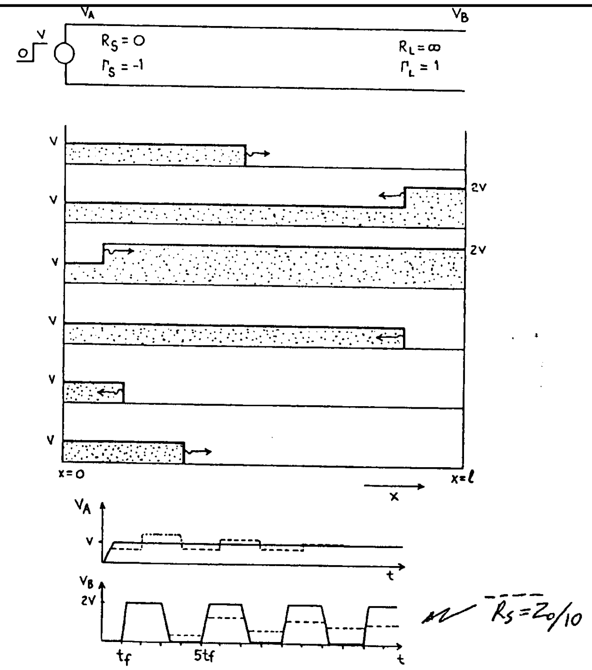


FIGURE 6.18 Termination at the source end: $R_S = Z_0$, $R_L = \infty$



4/15/2012 **FIGURE 6.16** No termination: $R_S = 0$, $R_L = \infty$

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6. WHEN TO USE TRANSMISSION LINE ANALYSIS 243

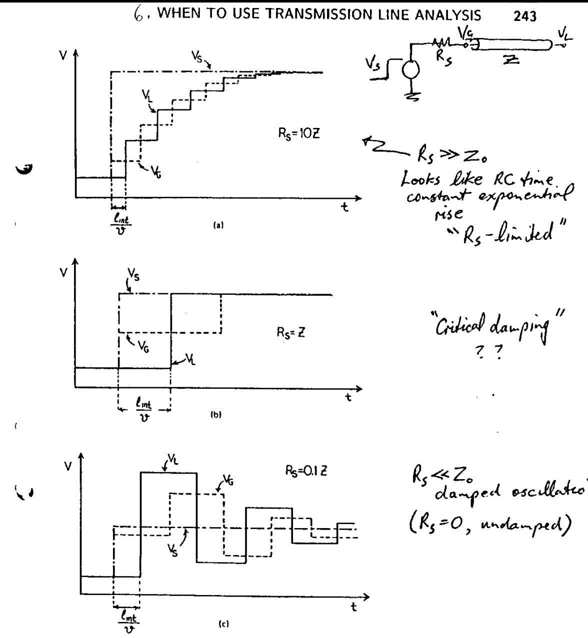

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FIGURE 6.8 Waveforms for various R_S and Z_0 combinations in the circuit in Fig. 6.7. As can be seen by the l_{int}/v markers, the time axes of the plots are not drawn at the same scale for clarity. The top plot $R_s = 10Z_0$ has the longest delay.

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3. Mismatched load &/or source

- 1 volt pulse, $Z_0 = 78\Omega$
  - Consider $R_L = 78\Omega$ cases first, then vary R_L

- (a) $R_S = Z_0$
- (b) $R_S << Z_0$
- (c) $R_S >> Z_0$

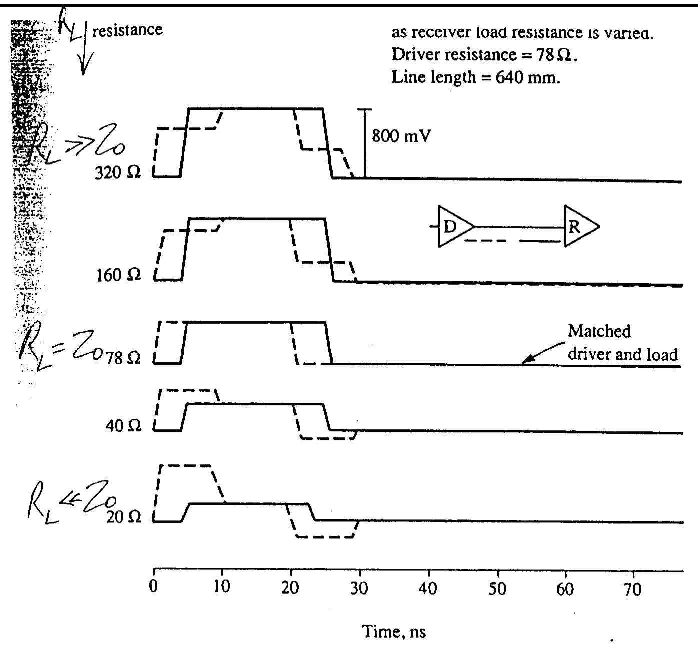

FIGURE 3-10
Same as Figure 3-9, but driver resistance is 78 Ω. $R_S = Z_0$

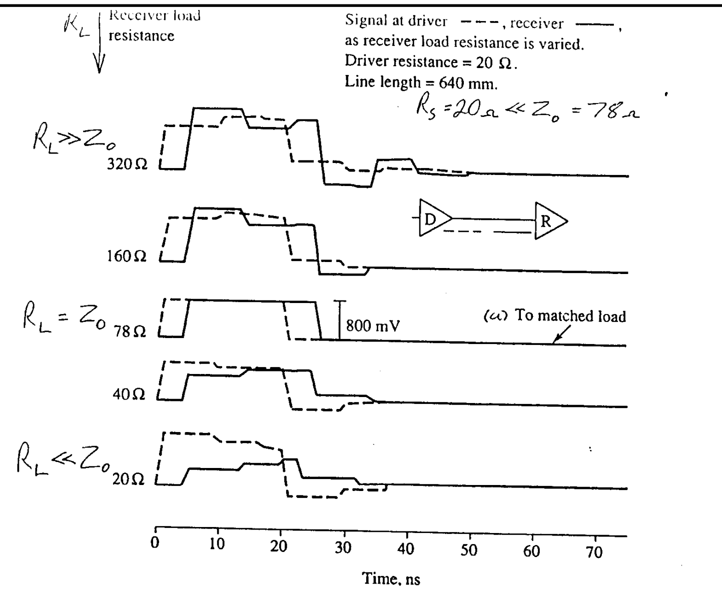

FIGURE 3-9
Multiple reflections on a transmission line. Signal at driver and receiver, driver resis 20 Ω. R_T is varied from low to high values. Characteristic impedance Z_0 of line is 7 waveform is a 20-ns wide trapezoidal pulse with 1 ns rise and fall times and 1 V p(into an open circuit.

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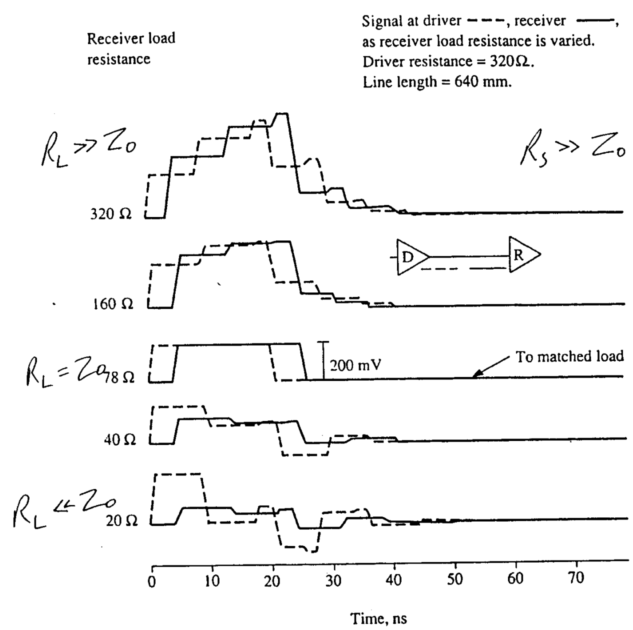

FIGURE 3-11
Same as Figure 3-9, but driver resistance is 320 Ω.

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4. Bounce chart/lattice diagram

- Calculate reflection coefficients
- Distance / time diagram
- Transfer data to waveform plots
- Examples:
  - (1) Open circuit line
  - (2) Two segment line

(1)

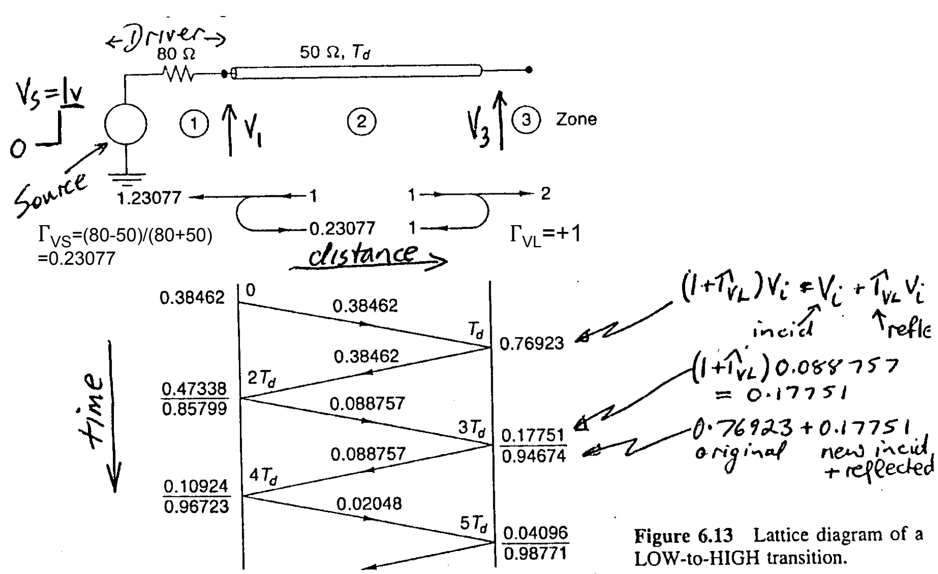


Figure 6.13 Lattice diagram of a LOW-to-HIGH transition.

"BOUNCE" CHART / LATTICE DIAGRAM

(1) $R_S = 80\,\Omega$ $Z_0 = 50\,\Omega$ $R_L = \infty$

$\therefore \Gamma_{VS} = \frac{80-50}{80+50} = \frac{3}{13} = 0.23077$ $\Gamma_{VL} = \frac{\infty - 50}{\infty + 50} = 1$

At $t=0$: $V_1 = \frac{50}{50+80} V_S = \frac{5}{13} v = 0.38462v$

$t = T_d$: Load $V_i = 0.38462v$ $V_r = \Gamma_{VL} V_i = 0.38462v$

& load voltage $V_3 = V_i + V_r = 0.76924v$

$t = 2T_d$: Driver Reflected wave $V_r = \Gamma_{VS} \times 0.38462v = 0.088757v$

$V_1 = 0.38462v + 0.38462v + 0.088757v$

original pulse; reflection from load; reflection back to load

$= 0.85799v$

$t = 3T_d$: Load Reflected wave $= \Gamma_{VL} \times 0.088757v = 0.088757v$

$V_3 = 0.76924 + .088757 + 0.088757$

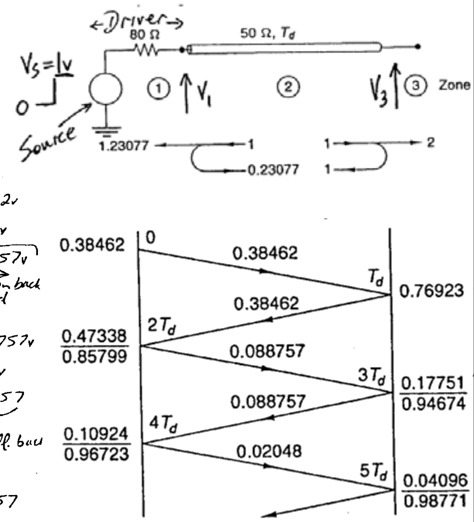
Previous value; $(1+\Gamma_{VL})V_i = 0.17751$ Incid reflection + next refl. back

$= 0.94674v$

$t = 4T_d$: Driver Reflected wave $= \Gamma_{VS} \times 0.088757 = 0.02048v$

$V_1 = 0.85799v + (0.088757 + 0.02048)v$

$= 0.96723v$



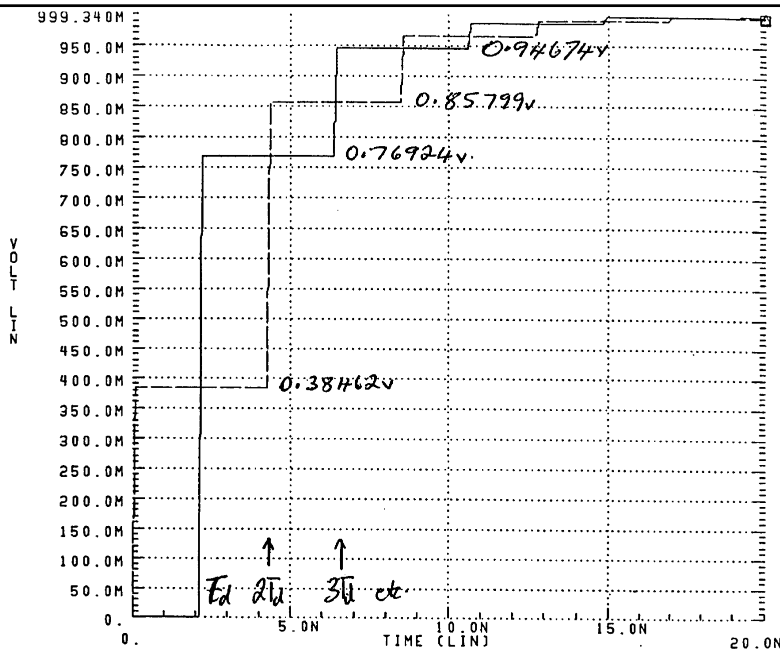
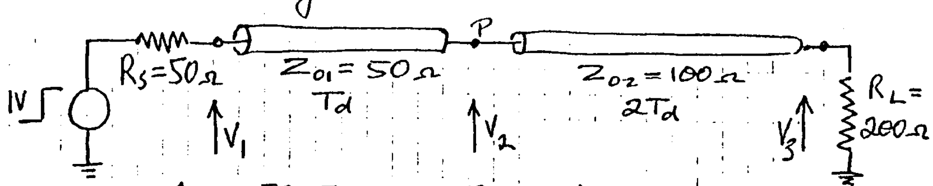


Figure 6.14 Voltage waveforms at source (dotted line) and receiver (solid line), L-to-H transition, $R_s > Z_o$. See Fig. 6.13.

(2)

(2) Two-segment line



$$\Gamma_{VS} = \frac{50-50}{50+50} = 0$$

wave →

$$\Gamma_{VP} = \frac{100-50}{100+50} = 1/3$$

$$\Gamma_{VL} = \frac{200-100}{200+100} = \frac{1}{3}$$

← wave

$$\Gamma'_{VP} = \frac{50-100}{50+100} = -1/3$$

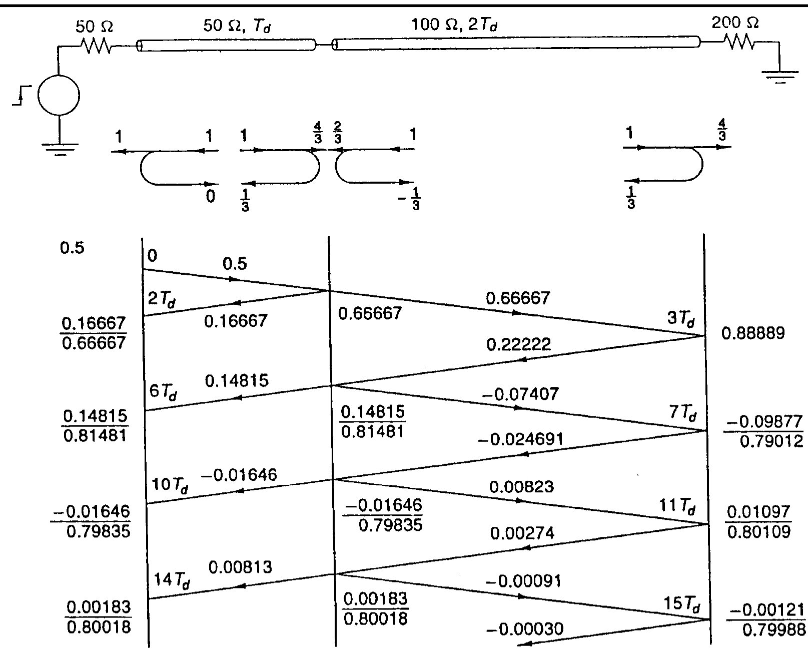


Figure 6.15 Lattice diagram for a two-segment transmission line, L-to-H transition.

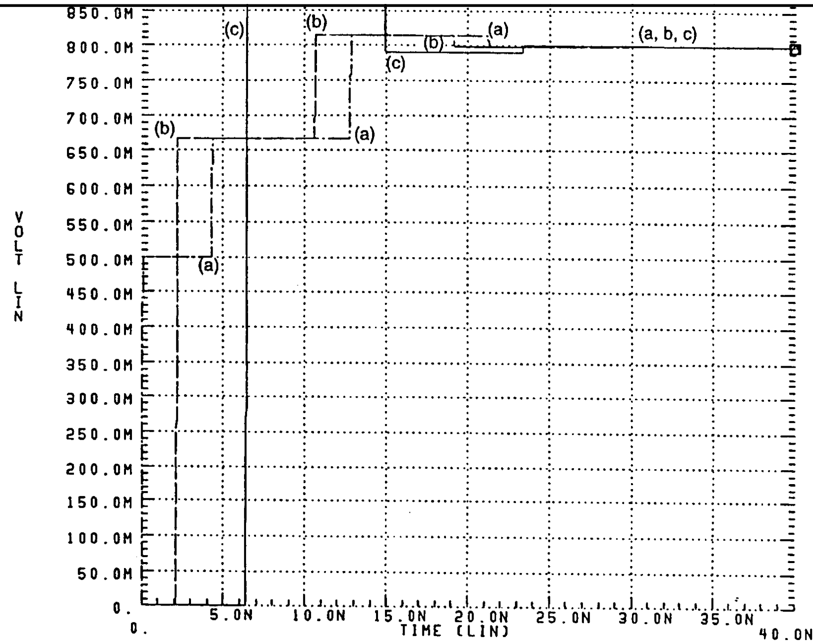


Figure 6.16 Voltage waveforms at (a) source, (b) junction of the two transmission line segments and (c) far end. See Fig. 6.15.

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5. Discontinuities

- Capacitive loads (MOSFETs)
- Stubs
- Multiple loads
- Line geometry changes
  - – bends
  - – vias
- Non-linear loads

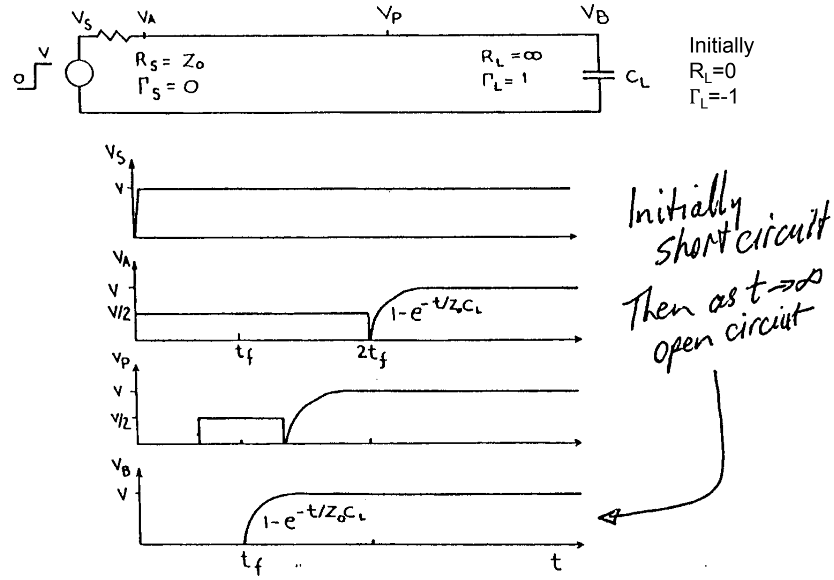


FIGURE 6.22 Capacitively terminated transmission line

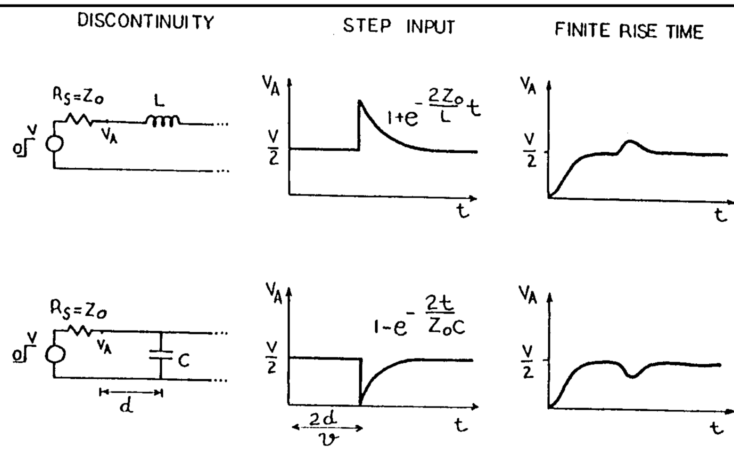


FIGURE 6.6 Inductive and capacitive discontinuities. The transmission line is driven by a signal generator with $R_S = Z_0$, and the reflected waveforms are observed at the source end. The line is either infinitely long or is terminated with $R_L = Z_0$ at the far end. Two types of reflected waveforms are plotted for each discontinuity: one assuming a step input (left) and another assuming a finite-rise-time input (right).

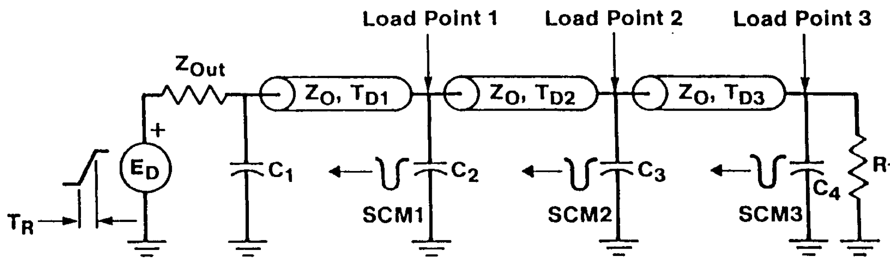


Figure 3-9. Discrete or Distributed Net Configurations. Note reflections fro discontinuities.

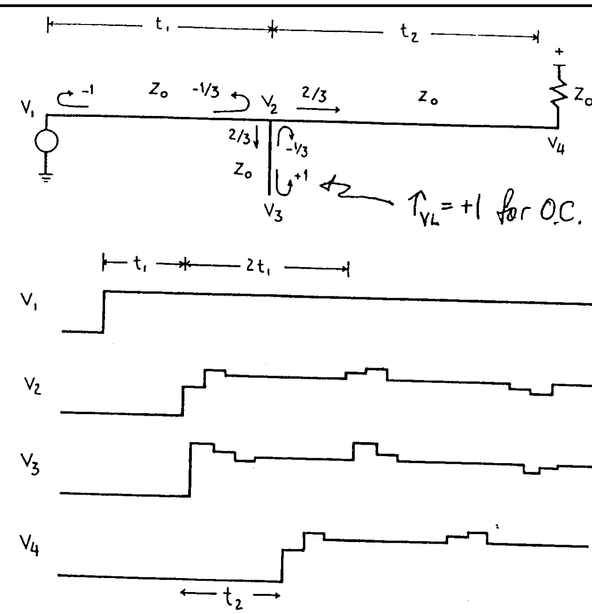


FIGURE 6.32 Data bus with a long stub

Stub is o.c. via, low current load, etc.

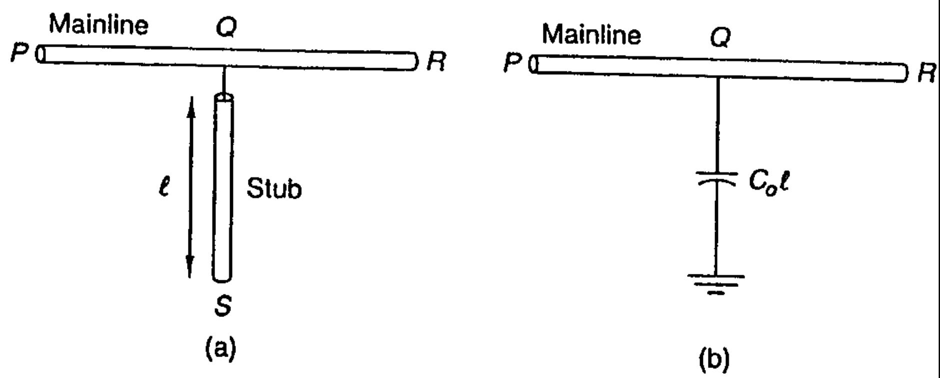
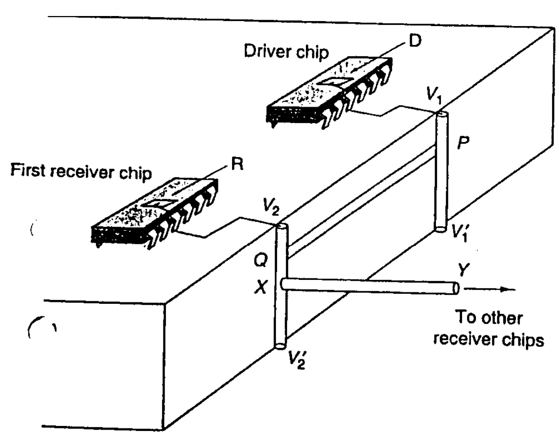


Figure 6.3 A short stub (a) reflects as a capacitor (b).



Best to drive multiple loads from branch at matched source — avoids multiple reflection times from stubs.

Figure 6.4 DV_1, RV_2 are metallizations on the board surface. PQ, XY are board internal traces. V_1V_1', V_2V_2' are through vias. The path DV_1PQXY is the mainline, while RV_2Q, PV_1' and XV_2' are stubs.

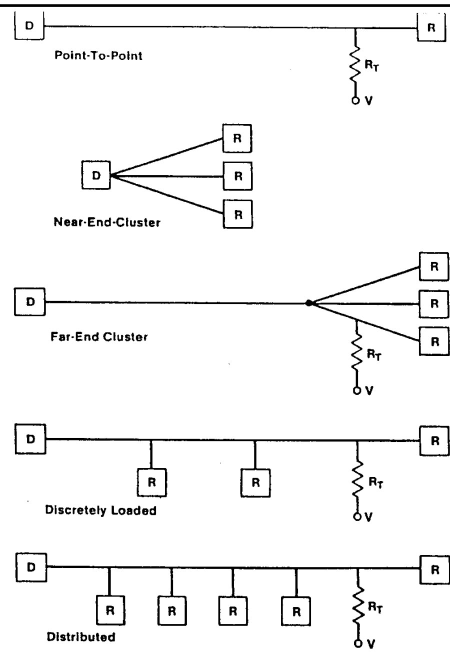


Figure 3-8. Chip Interconnection Networks.

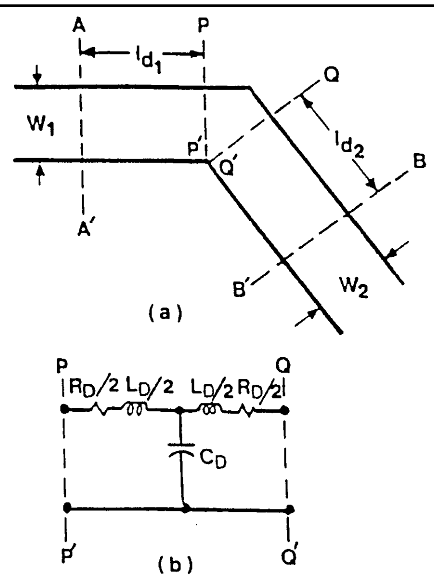


Figure 4-8 (a) A planar bend - top view; (b) Equivalent circuit representation.

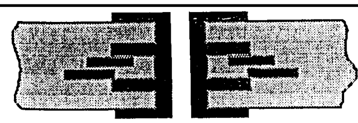


Figure 3.12 Through holes.

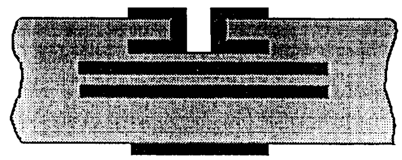


Figure 3.13 Blind vias.

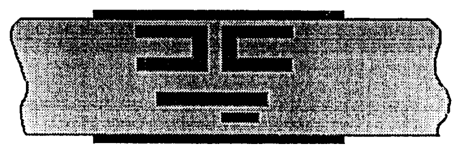


Figure 3.14 Buried vias.

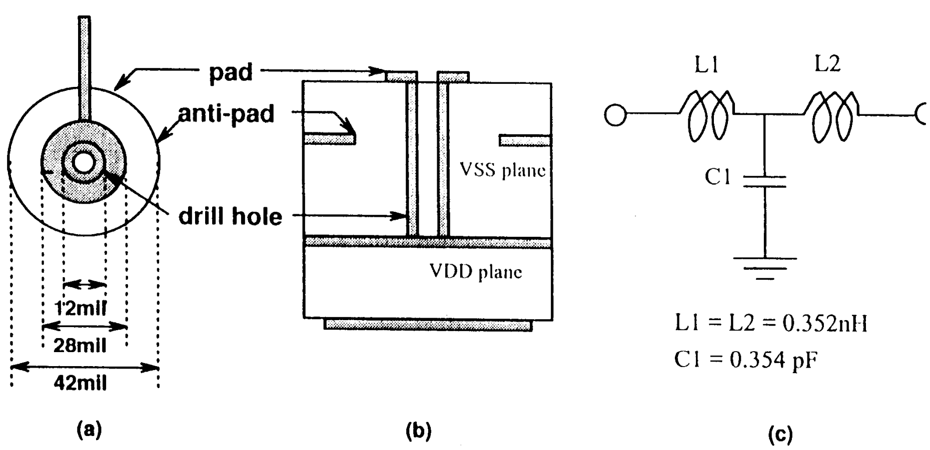


Fig. 10. A via hole (a) top view (b) cross-sectional view (c) equivalent circuit model

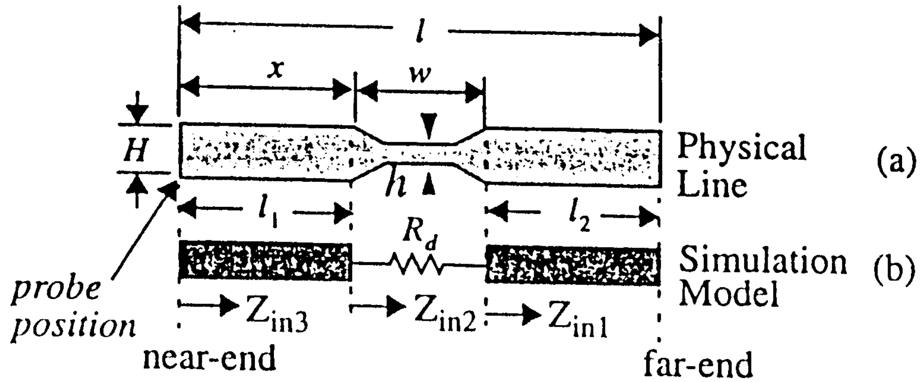


Figure 6. Simulation Model for an Interconnect with Near-Open Defect.

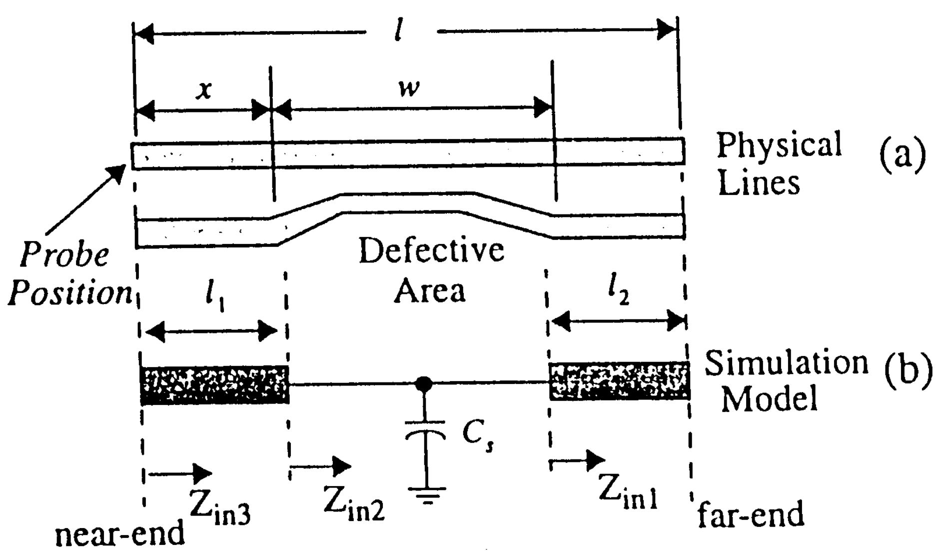
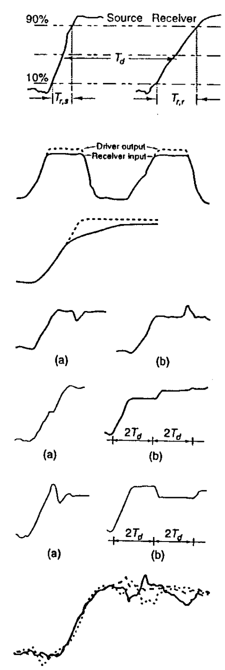


Figure 7. Simulation Model for an Interconnect with Near-Short Defect.

Summary



TRANSMISSION LINE EFFECTS

	Waveform	Transmission line effect	Description/environment	Section
(1)		Propagation delay T_d Risetime degradation ($T_{r,r} > T_{r,s}$)	Line is distributed if $2T_d \geq T_r$	9.1.4
(2)		Ohmic drop (frequency-independent)	Steady-state attenuation	5.2
(3)		Skin effect (frequency dependent)	Slow dribble-up at transition	10.4
(4)	(a) (b)	Reflection from lumped loads: (a) capacitor (b) inductor	Glitch accompanies every transition	6.2.2
(5)	(a) (b)	Undershoot on (a) short line (b) long line	Parallel-terminated line: (at receiver): $R_t < Z_o$ Series-terminated line (at source): $R_s > Z_o$	6.4
(6)	(a) (b)	Overshoot on (a) short line (b) long line	Parallel-terminated line (at receiver): $R_t > Z_o$ Series-terminated line (at source): $R_s > Z_o$	6.4
(7)		Spurious noises: • crosstalk • switching • oscillations • others	Non-deterministic association with every transition	Chap. 7, 8

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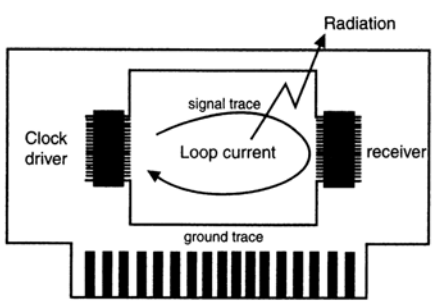
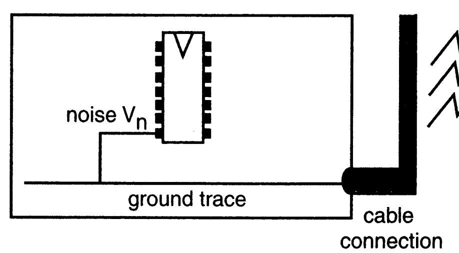
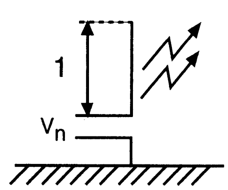
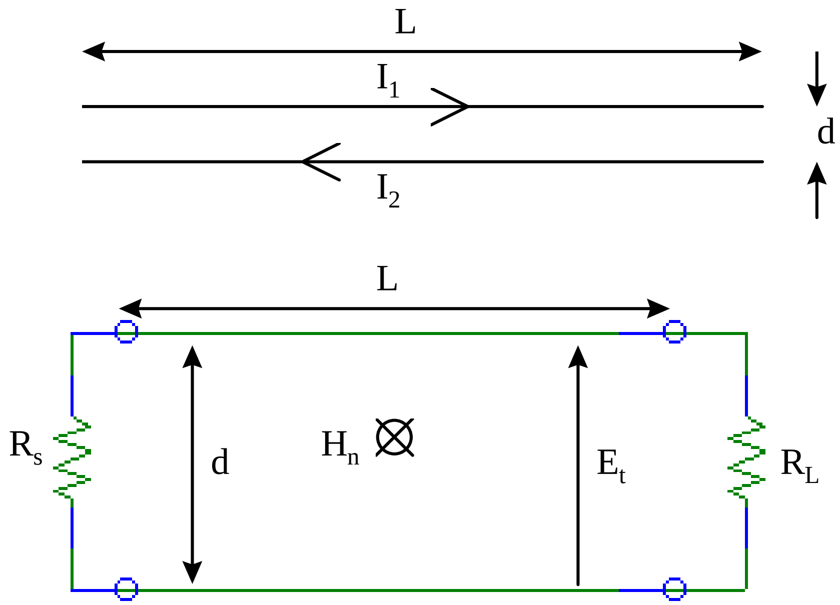
EMI/EMC Models: Loop/Dipole Antennas







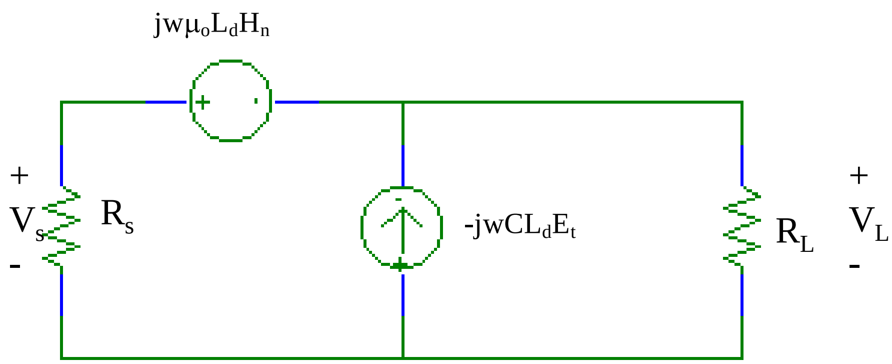


Electromagnetic compatibility/interference models

EMI/EMC Models: Emissions

- At "far field" distance r ($\geq\lambda$=c/f) from the line of length L and area A = L.d, the radiated electric field strength is
  - $E = E_D + E_{CM}$
- where E_D due to the differential current I_D is
  - $E_D = 131.6 \times 10^{-16} f^2 A I_D / r$ V/m
- and E_{CM} due to the common mode current I_{CM} is (for $L \leq \lambda$)
  - $E_{CM} = 4\pi \times 10^{-7} f^2 L I_{CM} / r$ V/m
- where $I_D = (I_1 + I_2)/2$ and $I_{CM} = (I_1 - I_2)/2$. Common mode currents are ideally zero, but small values can lead to CM dominance over differential. For the differential current, the maximum value can be taken to be the supply current, but the user must specify a non-ideal common mode estimate. For digital systems, use $f = 2\pi/t_r$. For other geometries, other expressions for A are valid.
- There are many different standards for EM radiation limits, but for guidance the EU limit is $E \leq 100\mu$V/m at r = 10m (class A) or 3m (class B).

EMI/EMC Models: Susceptibility



Susceptibility

- For the line shown, with capacitance C per unit length, e.g.
  - $C = \pi\ \varepsilon_r\varepsilon_0/\ln(d/r_w)$
- for parallel wires, the induced voltages are
- $V_S = -j\omega\ [R_LR_S/\ (R_L\ +\ R_S)]\ [Ld]\ [C\ -\ (\mu_0/\eta_0)/R_L]$
- $V_L = -j\omega\ [R_LR_S/\ (R_L\ +\ R_S)]\ [Ld]\ [C\ +\ (\mu_0/\eta_0)/R_S]$
- where $E = E_t = \eta_0\ H_n$, and $\eta_0 = 120\pi = 377\Omega$.
- As an example of an EU standard, the device must function in a field of E = 3V/m.