ECE414/514
Electronics Packaging

Spring 2012 Lecture 3
Electrical A:
CMOS; R, L, & C;
ground planes; delta-I noise

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Lecture topics

1. Interconnect modeling
2. Resistance, inductance, & capacitance
   - R, L, & C
3. Skin effect
4. Ground planes
5. MOS devices and CMOS
6. Delta-I (ΔI) switching noise

Objectives

- Explain origins & effects of inductance
  - Review impedance concepts (inductance)
  - Introduce skin effect
  - Understand role of ground planes
- Relate CMOS requirements to package
  - Review MOS device physics
  - Understand CMOS current switching
  - Understand origins of delta-I noise

1. Interconnect modeling

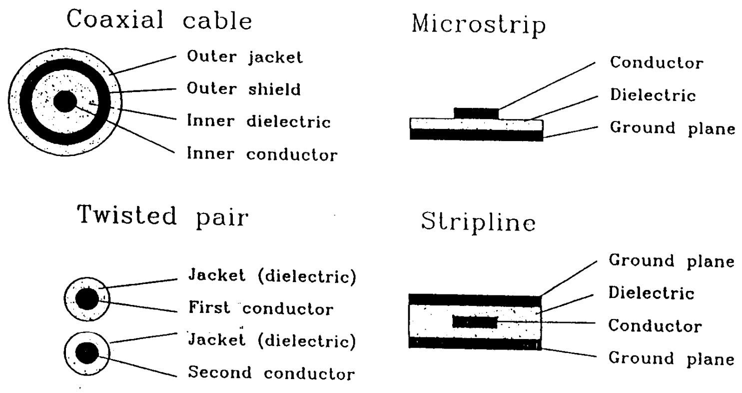
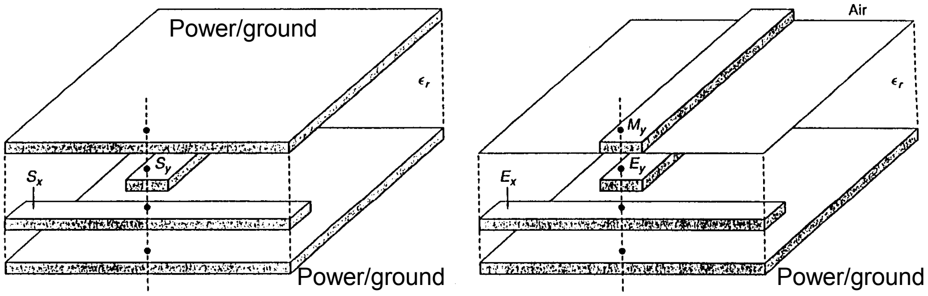


Figure 4.4 Cross sections of popular transmission line geometries.

4.2.1 Ideal Distortionless, Lossless Transmission Line

Orthogonal line systems:
stripline ↓ & microstrip ↓



(a) (b)

Figure 4.18 Common strip types are (a) for internal layers: offset striplines S_x and S_y, and (b) for surface layers: microstrip M_y and embedded microstrips E_x and E_y. The same design may not use all of them. Metal edges are shaded.

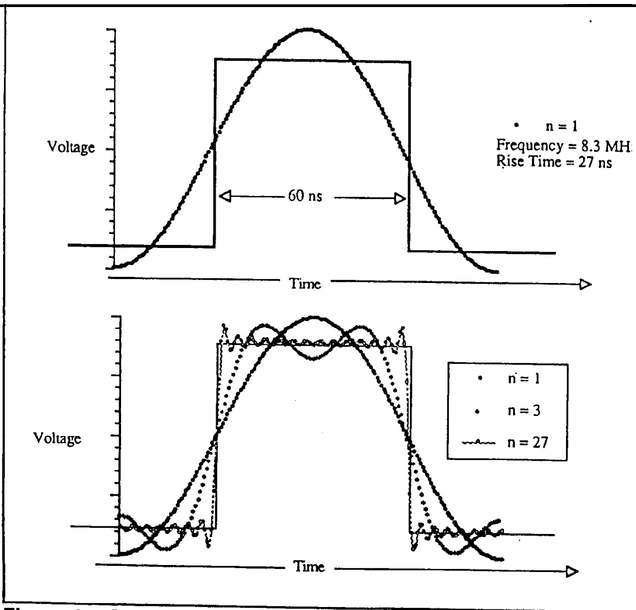
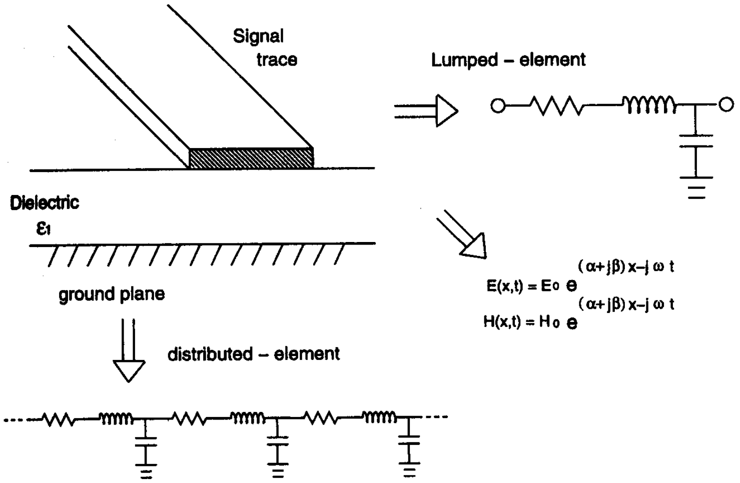


Figure 8.5 Sinusoidal components of a square wave pulse.

Three modeling approaches:



(a) $\omega L >> R$, (b) $R >> \omega L$, (c) $R \approx 0$

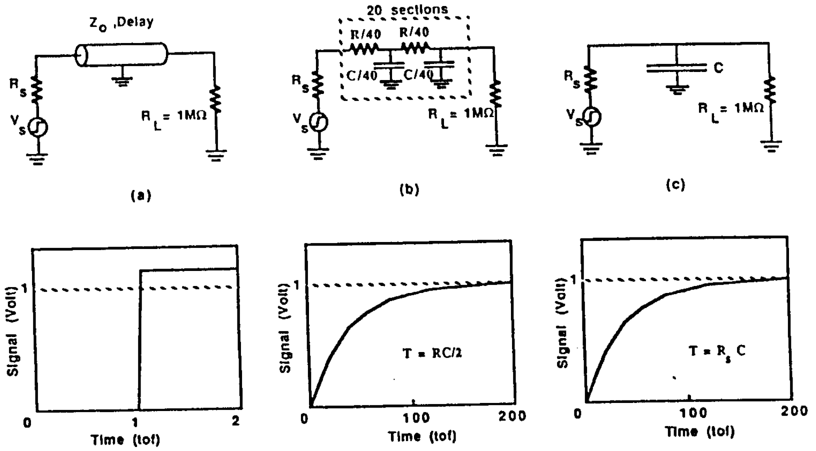


Figure 5-7 Simplified SPICE circuits & signal load responses for limiting propagation regimes. (a)Time-of-flight ($R_S<Z_0$) (b)lossy-line diffusion (c)R_S-limited; time scales are in units of time-of-flights

Typical packaging line lengths & widths

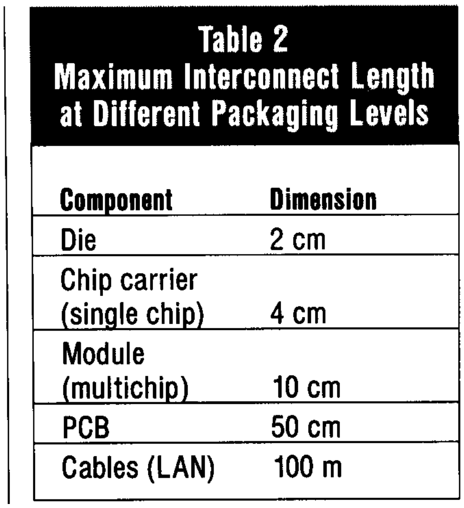


Table 2
Maximum Interconnect Length at Different Packaging Levels

Component	Dimension
Die	2 cm
Chip carrier (single chip)	4 cm
Module (multichip)	10 cm
PCB	50 cm
Cables (LAN)	100 m

Widths

VLSI “wires” in Si:
0.1 to 1 μm

MCM trace widths:
1 to 10 μm

Packages:
10 μm to 0.1 mm

PCBs:
0.1 to 1 mm

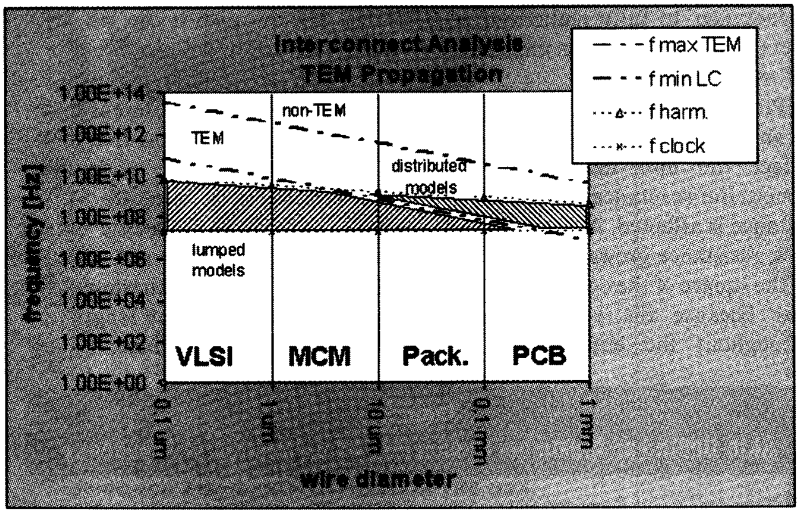
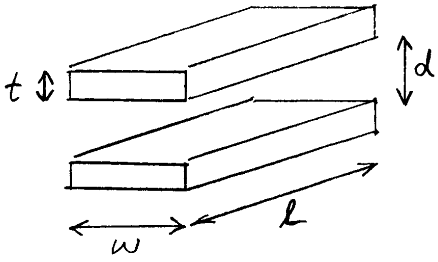


Figure 2
Currently used clock rates (f clock) and their harmonics (f harm).

PRINTED CIRCUIT DESIGN / JULY 1995

2. R, G, ℓ, and C

- Conductor:
- $R = \rho\, \ell/A_R = \rho\, \ell/wt = (\ell/w)\,(\rho/t)$
  - $R/\ell = \rho/wt$
- Dielectric:
- $G = \sigma A_C/d = \sigma\, \ell\, w/d$
  - $G/\ell = \sigma\, w/d$
- $C = \varepsilon A_C/d = \varepsilon\, \ell\, w/d$
  - $C/\ell = \varepsilon\, w/d$



Capacitance/unit length

"Visual" approximations

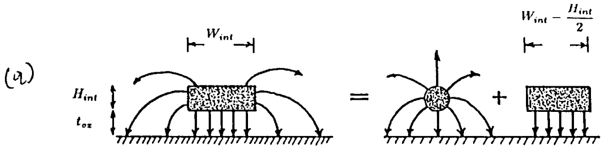


FIGURE 4.2 Modeling of the contribution of fringing fields to interconnection capacitance. Total wire capacitance can be thought of having two components: a parallel plate capacitance determined by the perpendicular field lines between the wire and the ground plane and a fringing field component, which can be approximated by the capacitance of a cylindrical wire with a diameter equal to interconnection thickness [4.3]. Reprinted by permission of Addison-Wesley Publishing Co.

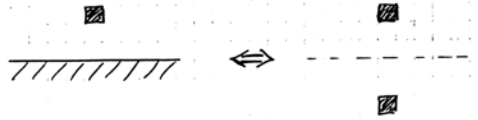
reduced by $H_{int}/2$ to account for some second-order effects [4.4]. This yields the interconnection capacitance per unit length C_{int} as

$$C_{int} = \epsilon_{ox}\left\{\frac{W_{int}}{t_{ox}} - \frac{H_{int}}{2t_{ox}} + \frac{2\pi}{\ln\left[1+\frac{2t_{ox}}{H_{int}}\left(1+\sqrt{1+\frac{H_{int}}{t_{ox}}}\right)\right]}\right\}. \qquad (4.5)$$

Other Capacitor Geometries

(a) "VISUAL" APPROXIMATIONS

(b) METHOD OF IMAGES



$$C_1 = 2\,C_2$$

& since $Z_0 = \sqrt{\frac{L}{C}} \Longrightarrow \frac{v^{-1}}{\sqrt{C}}\frac{1}{\sqrt{C}}$

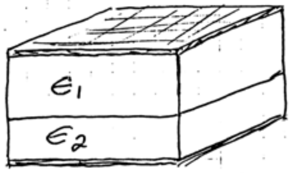
& $v^{-1} = \sqrt{LC}$ $\quad \therefore Z_0 = \frac{v^{-1}}{C}$

$Z_0 C$ independent of geometry.

so $2Z_{01} \Leftrightarrow Z_{02}$

Can find one if know other.

(C) MIXED DIELECTRICS



$$\frac{1}{C} = \frac{1}{C_1} + \frac{1}{C_2}$$

(d) Analytical field calculations (usually idealized structures)

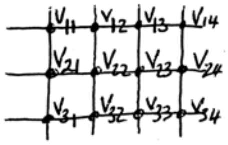
$V = \Sigma v_i$ for charges ρ_i

(e) Graphical approximations — curvilinear squares

(f) Experimental field plotting

(g) Numerical techniques
- mesh
- iteration

For 2D



$$V_{22} = \frac{1}{4}\left(V_{12} + V_{23} + V_{32} + V_{21}\right)$$

(h) Method of Moments

Potential from known charge distribution simple by superposition $V = \frac{1}{4\pi\epsilon} \sum \frac{q_i}{R_i}$

Converse to find charge distribution to produce known potential.

Method of Moments Example

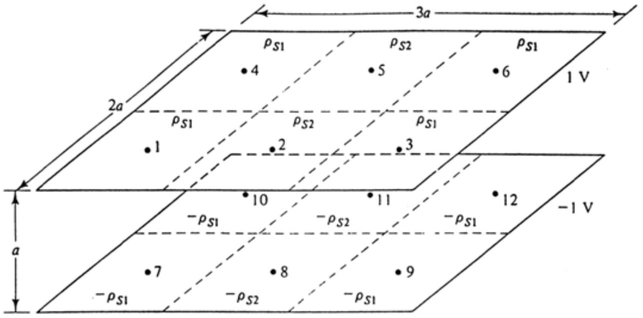


Figure 5.10. For finding the capacitance of a parallel-plate capacitor by the method of moments.

$C=\varepsilon(6a^2/a)=6\varepsilon a$?

Method of Moments Example

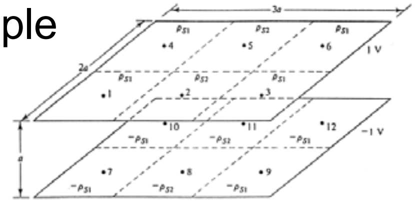


Figure 5.10. For finding the capacitance of a parallel-plate capacitor by the method of moments.

PARALLEL PLATE CAPACITOR

$C = \epsilon \frac{A}{d}$

neglects fringing fields

Field curvature $\rightarrow$ non-uniform surface charge distribution ρ_s

eg. 3a × 2a × a capacitor. Charges $\rho_{S1} a^2, \rho_{S2} a^2$ by symmetry. Assume charges at center of □'s.

Potential at point 1 due to ρ_{S1} at point 4

$$\rightarrow \frac{(\rho_{S1} \times a^2) \leftarrow q}{4\pi\epsilon\, a \leftarrow \text{distance}}$$

Potential at point 1 due to distributed charge $\rho_{S1} a^2$ on square #1 $= \frac{(\rho_{S1} \times a^2)}{\pi \epsilon a} \ln(1+\sqrt{2})$

Method of Moments Example

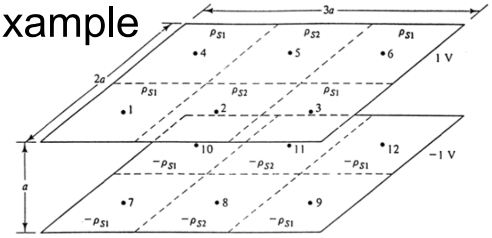


Figure 5.10. For finding the capacitance of a parallel-plate capacitor by the method of moments.

∴ For fixed plate potentials 1v, −1v

Square #1 : $$V_1 = \frac{\rho_{S1} a}{\pi \epsilon} \ln(1+\sqrt{2}) + \frac{\rho_{S1} a^{*}}{4\pi\epsilon}\left(\frac{1}{2} + 1 + \frac{1}{\sqrt{5}} - 1 - \frac{1}{\sqrt{5}} - \frac{1}{\sqrt{2}} - \frac{1}{\sqrt{6}}\right)$$
$$+ \frac{\rho_{S2} a}{4\pi\epsilon}\left(\cancel{2}1 + \frac{1}{\sqrt{2}} - \frac{1}{\sqrt{2}} - \frac{1}{\sqrt{3}}\right) = 1\text{v}$$

Square #2: $$V_2 = \frac{\rho_{S2} a}{\pi \epsilon} \ln(1+\sqrt{2}) + \frac{\rho_{S1} a}{4\pi\epsilon}\left(2 + \frac{2}{\sqrt{2}} - \frac{2}{\sqrt{2}} - \frac{2}{\sqrt{3}}\right)$$
$$+ \frac{\rho_{S2} a}{4\pi\epsilon}\left(1 - 1 - \frac{1}{\sqrt{2}}\right) = 1\text{v}$$

Method of Moments Example

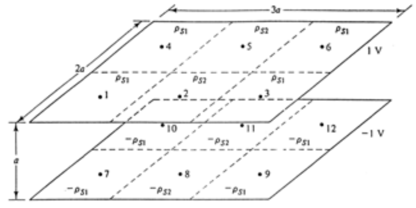


Figure 5.10. For finding the capacitance of a parallel-plate capacitor by the method of moments.

$$\frac{\rho_{S2}a}{\pi\varepsilon_0}\ln(1+\sqrt{2})+\frac{\rho_{S1}a^2}{4\pi\varepsilon_0}\left(\frac{2}{a}+\frac{2}{\sqrt{2}a}-\frac{2}{\sqrt{2}a}-\frac{2}{\sqrt{3}a}\right)$$
$$+\frac{\rho_{S2}a^2}{4\pi\varepsilon_0}\left(\frac{1}{a}-\frac{1}{a}-\frac{1}{\sqrt{2}a}\right)=1 \qquad (5.31b)$$

(Square #2 last slide)

or

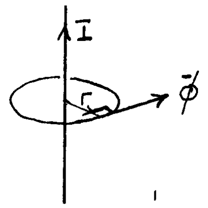
$$2.9101\rho_{S1}+0.4226\rho_{S2}=\frac{4\pi\varepsilon_0}{a} \qquad (5.32a)$$

$$0.8453\rho_{S1}+2.8184\rho_{S2}=\frac{4\pi\varepsilon_0}{a} \qquad (5.32b)$$

Solve: $\rho_{S1}=3.8378\epsilon/a$ $\rho_{S2}=3.3075\epsilon/a$

$\therefore$ Total $Q=21.9662\varepsilon a$ and $C=Q/V=Q/2\text{v}=10.983\varepsilon a$ (c.f. 6εa)

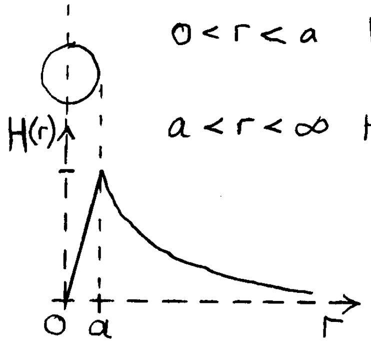
Inductance of a Straight Wire: Magnetic Field



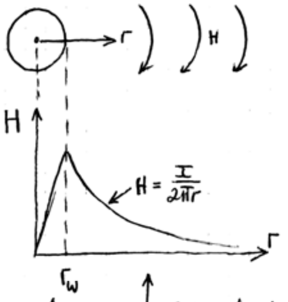
$\vec{H}(r)=\frac{I}{2\pi r}\hat{\phi}$

$0<r<a$ $\quad H(r)=\frac{\pi r^2}{\pi a^2}\cdot I\frac{1}{2\pi r}\hat{\phi}=\frac{Ir}{2\pi a^2}\hat{\phi}$

$a<r<\infty$ $\quad H(r)=\frac{I}{2\pi r}\hat{\phi}$



Internal & External Inductances



↑ External inductance $l_e >> l_i$ usually

↑ Internal inductance l_i

$l = l_i + l_e \approx l_e$

Also $l_e g = \mu\sigma$

$l_e c = \mu\epsilon$

g, c leakage conduct/capac

σ, ε, μ for external medium

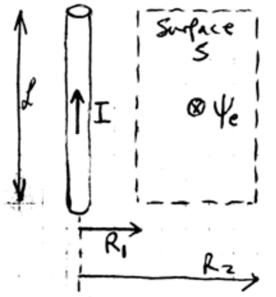
$$\oint_c \underset{\sim}{H}\cdot d\underset{\sim}{l} = I_{enclosed} \xrightarrow{\text{Circular contour at } r} H(r).\,2\pi r = I$$

$$H(r) = \frac{I}{2\pi r}$$

External Inductance: Basic formula

Need to find total external flux

$$\Psi_e = \int_S \underset{\sim}{B}(r).d\underset{\sim}{s} = \int_{R_1}^{R_2} \mu_0 \frac{I}{2\pi r}\, dr = \frac{\mu_0 I}{2\pi} \ln\left(\frac{R_2}{R_1}\right)$$



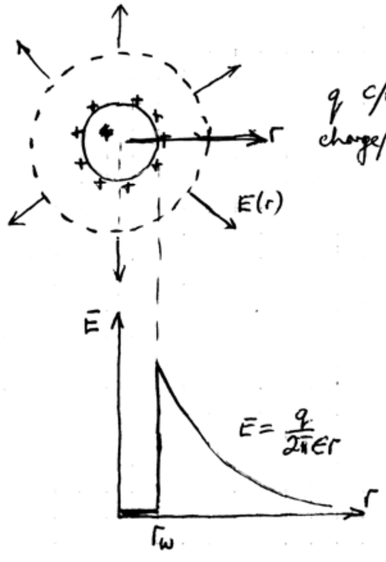
Note: To find $l_e = \frac{\Psi_e}{I} = \frac{\mu_0}{2\pi} \ln\left(\frac{R_2}{R_1}\right)$

over all space $\begin{pmatrix} R_2 \to \infty \\ R_1 = r_w \end{pmatrix}$

requires assumption of specific geometries

(Can't have isolated current, must be a return path)

Straight Wire: Radial Electric Field



q c/m
charge/unit length

$$\oint_S \epsilon \underset{\sim}{E}\cdot d\underset{\sim}{s} = Q_{encl.}$$

$$\epsilon E\,(2\pi r\times\mathcal{L}) = q\times\mathcal{L}$$

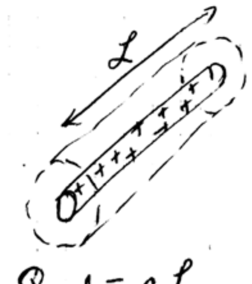
$$\therefore\ E(r) = \frac{q}{2\pi\epsilon r}$$

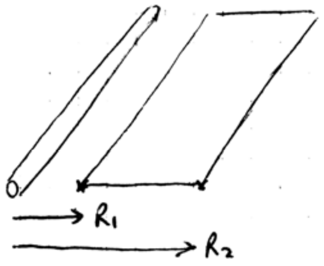
$$\&\ V = -\int_C \underset{\sim}{E}\cdot d\underset{\sim}{\ell}$$

$$= -\int_{R_2}^{R_1}\frac{q}{2\pi\epsilon r}\,dr$$

$$= \frac{q}{2\pi\epsilon}\ln\left(\frac{R_2}{R_1}\right)$$

Ψ_e and V: equate $(2\pi)^{-1}\ln(R_2/R_1)$





$Q_{encl} = q\mathcal{L}$
$\text{Area} = 2\pi r\times\mathcal{L}$

$$\&\ \text{note}\ \frac{V\epsilon}{q} = \frac{\psi_e}{\mu_0 I}$$

$$\ell_e = \frac{\psi_e}{I} = \mu_0\epsilon\frac{V}{q} = \mu_0\epsilon\, c^{-1}$$

↑ Capac/unit length

Internal Inductance

low freq — uniform current.

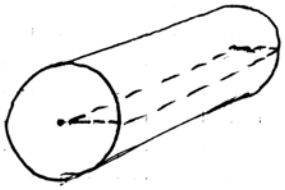
$$I_{encl,i} = \pi r^2 \left(\frac{I}{\pi r_w^2}\right) = I\left(\frac{r}{r_w}\right)^2$$

$$\therefore\ H(r) \cdot 2\pi r = I\left(\frac{r}{r_w}\right)^2 \Rightarrow H(r) = \frac{I}{2\pi r_w^2}\cdot r$$

&

$$\psi_i = \int_s \underset{\sim}{B(r)} \cdot \underset{\sim}{ds} \Rightarrow \psi_i \times \mathcal{L} = \mu_0\int_0^{r_w} \frac{I}{2\pi r_w^2}\, r \cdot \mathcal{L}\, dr$$

↑per unit length

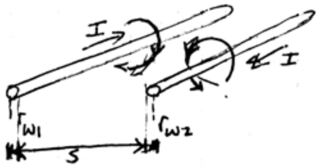


$$\psi_i = \frac{\mu_0 I}{4\pi}$$

$$\therefore\ l_i = \frac{\mu_0}{4\pi}\ \text{H/m}$$

External Inductance: 2-wire line

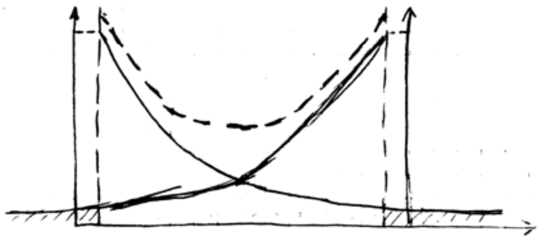
(a) 2-wire line



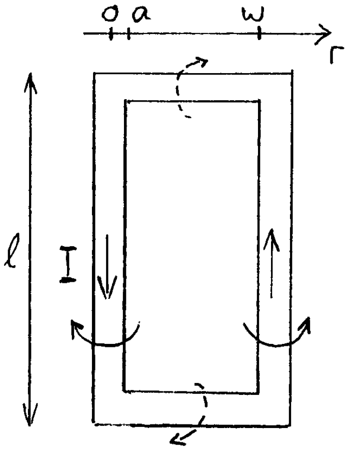
Total flux between wires

$$l_e = \frac{\psi_e}{I} = \frac{\mu_0 I}{2\pi}\left[\ln\left(\frac{s+r_{w1}}{r_{w1}}\right) + \ln\left(\frac{s+r_{w2}}{r_{w2}}\right)\right]$$

$$\underset{s \gg r_{w1} = r_{w2} = r_w}{\Rightarrow} \quad \frac{\mu_0 \cancel{I}}{2\pi}\ln\frac{s^2}{r_w^2} = \frac{\mu_0 \cancel{I}}{\pi}\ln\frac{s}{r_w}$$



Compare:-



$$L = \frac{\phi}{I} = \frac{1}{I}\int_S \vec{B}\cdot d\vec{S}$$

$$L = \frac{\mu}{I}\int \vec{H}\cdot d\vec{S}$$

$$\approx \frac{2\mu l}{I}\left[\int_0^a \frac{Ir}{2\pi a^2}dr + \int_a^w \frac{I}{2\pi r}dr\right]$$

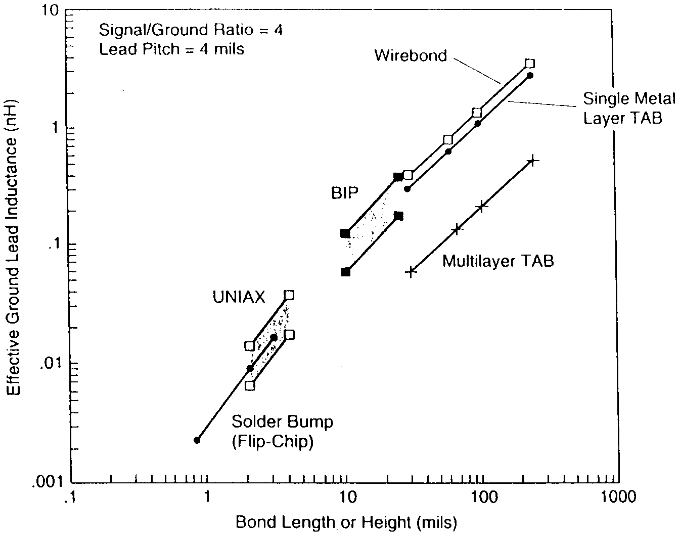
$$L/l = 2\left[\frac{\mu}{4\pi}\left(1 + 2\ln\frac{w}{a}\right)\right]$$

Hence "partial" inductance

$$L = \frac{\mu_0}{4\pi} + \frac{\mu_0}{2\pi}\ln\frac{W}{a}$$

$$= L_i + L_e \approx L_e$$

Lead inductances



3. Skin Effect

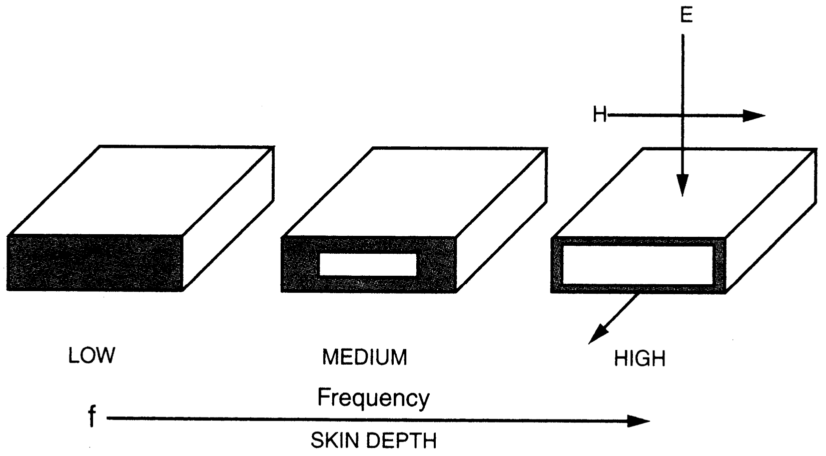


FIGURE 13.19 Effect of frequency on conductor cross section.

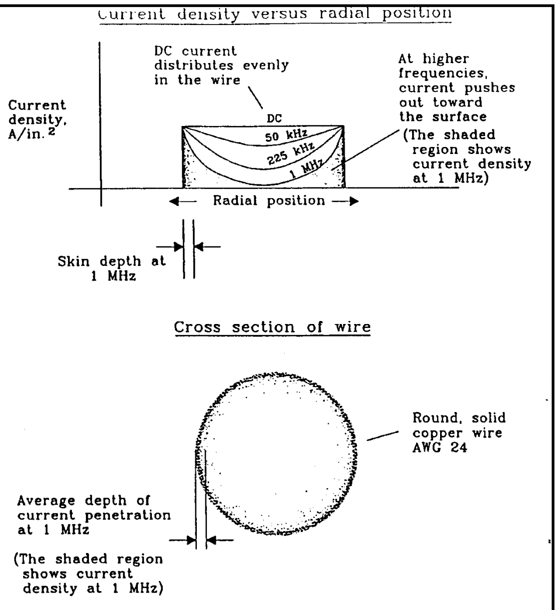
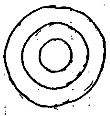


Figure 4.12 Distribution of current in a round wire.

8. SKIN EFFECT



Consider wire to consist of concentric cylinders

Inductance of outer rings $<$ Inductance of center rings

At high frequency, current path seeks lower inductance $\longrightarrow$ outer "skin"

SKIN DEPTH $\delta = \left(\frac{2\rho}{\omega\mu}\right)^{1/2}$

As current area decreases, resistance increases ($R = \rho \ell / A$)

$R \propto 1/\delta \propto freq^{1/2}$

and $L_{SKIN} \propto freq^{-1/2}$

Skin Reactance $\omega L_{SKIN} \propto freq^{1/2}$

($L_{internal} \ll L_{external}$)

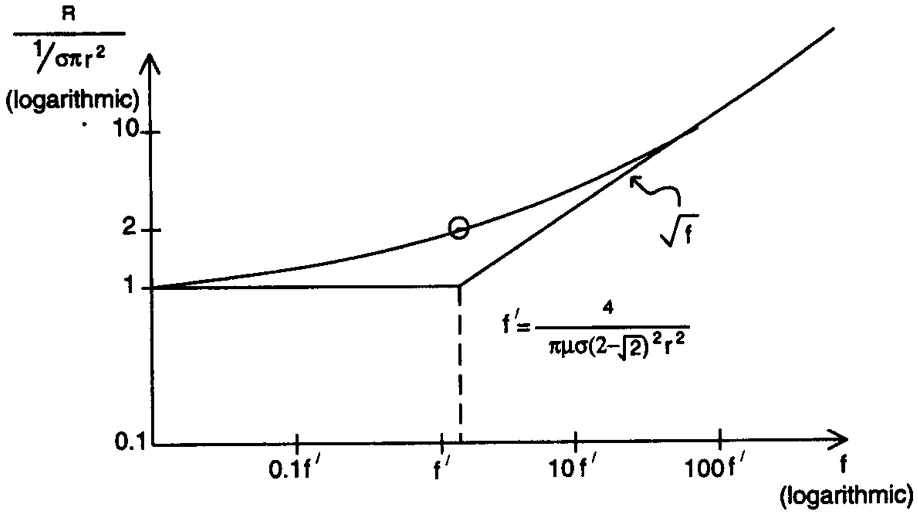
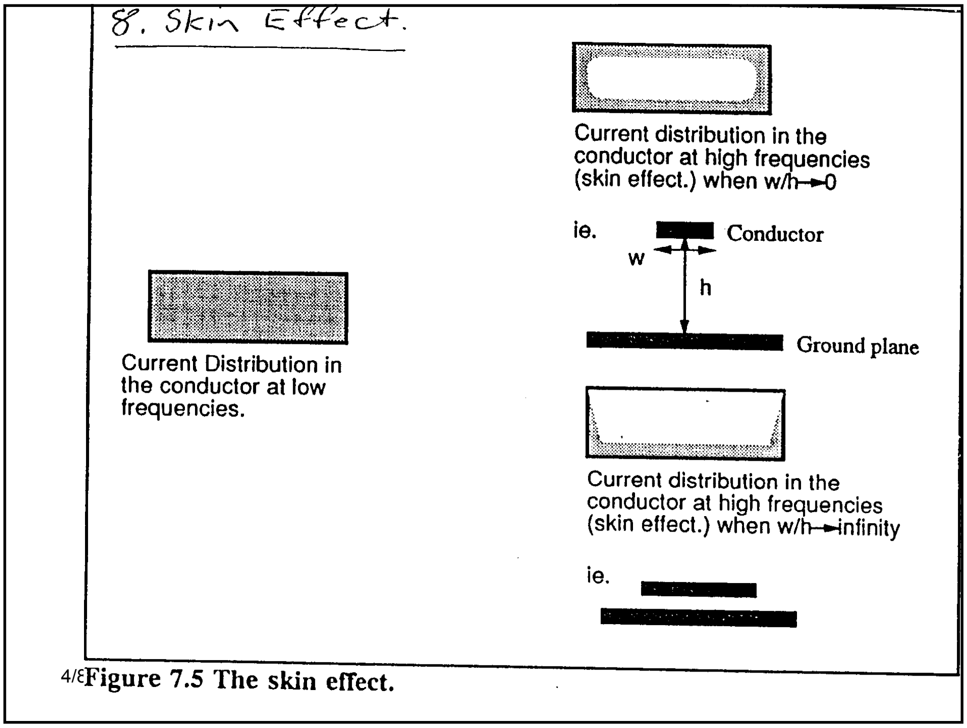
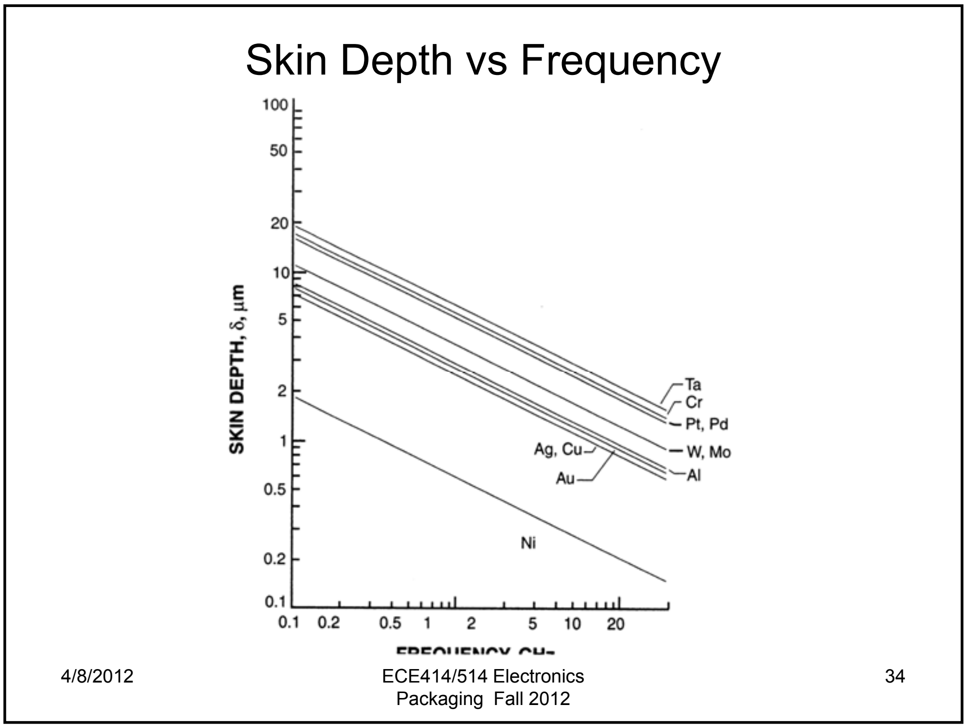


Figure 2.25 $R(f)$ for a wire of circular cross section, radius r.



8. Skin Effect.

4/ **Figure 7.5 The skin effect.**



Skin Depth vs Frequency

4. Ground planes

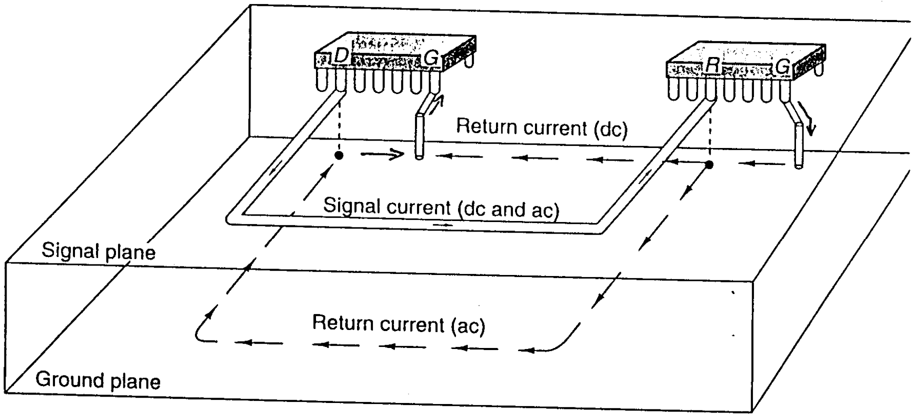


Figure 8.16 Paths for dc and ac ground returns on a multilayer board.

Loss of coupled return → inductance

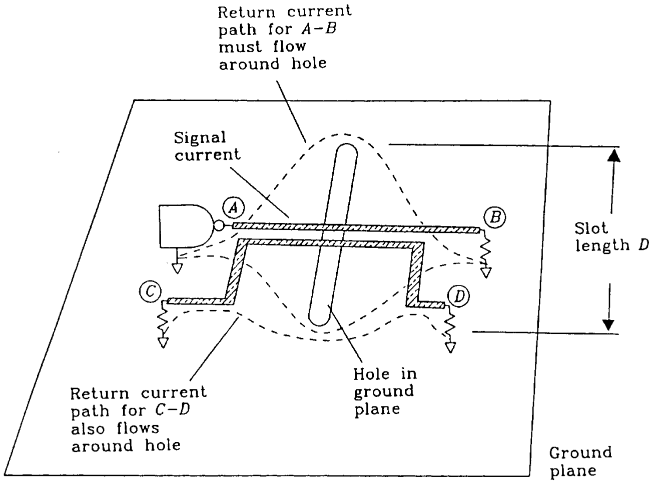


Figure 5.8 Crosstalk in a slotted ground plane.

2. DISCRETE IMPEDANCES

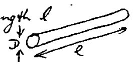
If a signal wire is separated from its return-current path (ground plane), it (& the return path) is modeled as a discrete component $R + j\omega L$ rather than by a transmission line.
(eg. common in high current systems)

[Note skin effect:

Skin depth $\delta = \left(\frac{\rho}{\pi \mu f}\right)^{1/2}$ m

& current distribution $I(x) = I(0) \exp -x/\delta$

1. Round wire : diameter D , length ℓ



(a) Straight

(i) Low frequency $f \ll 16\rho/\pi\mu D^2$, ie. $\delta \gg D/4$

$$R = \rho\ell / \pi (D/2)^2$$

$$L \approx \frac{\mu_0 \ell}{2\pi}\left[\ln\left(\frac{4\ell}{D}\right) + \left(\frac{\mu_r}{4}\right) - 1 + 0.389\left(\frac{D}{\ell}\right)\right] \text{ H}$$

(ii) High frequency

$R \approx \rho\ell / (\pi D . \delta)$ Skin effect

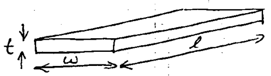
$$L \approx \frac{\mu_0 \ell}{2\pi}\left[\ln\left(\frac{4\ell}{D}\right) + \left(\mu_r \frac{\delta}{D}\right) - 1 + 0.5\left(\frac{D}{\ell}\right)\right] \text{ H}$$

(b) Circular wire, circumference ℓ.

Low freq $L \approx \frac{\mu_0 I}{2\pi}\left[\ln\left(\frac{2}{\pi}\frac{4\ell}{D}\right) + \left(\frac{\mu_r}{4}\right) - 2\right]$

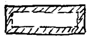
2. PCB land

$t \ll w$



(i) Low frequency $f \ll 4\rho(w+t)^2/\pi\mu w^2 t^2$

ie. $\delta \gg \frac{wt}{2(w+t)}$



$R = \rho\ell / wt$

$2(w+t)\delta > wt$
"Skin area" c/s area

$$L \approx \frac{\mu_0 \ell}{2\pi}\left[\ln\left(\frac{2\ell}{w+t}\right) + 0.5 + 0.2235\left(\frac{w+t}{\ell}\right)\right]$$

(ii) High frequency

$R = \rho\ell / 2(w+t)\delta$ Skin effect

$L \approx \frac{\mu_0 \ell}{2\pi}\left[\ln(X) - 1 + \left(\frac{X}{\ell}\right)\right]$ $X = (w+t)\Big[0.2929 - 0.0698\Big(\frac{w-t}{w+t}$

3. Groundplane : infinite groundplane, thickness t

$$R = \frac{\rho}{\delta}\left[\frac{1 - \exp(-t/\delta).[\cos(t/\delta) - \sin(t/\delta)]}{1 - 2\exp(-t/\delta).\cos(t/\delta) + \exp -2(t/\delta)}\right] \Omega$$

$$L = \frac{\rho}{2\pi f \delta}\left[\frac{1 - \exp(-t/\delta)[\cos(t/\delta) - \sin(t/\delta)]}{1 - 2\exp(-t/\delta).\cos(t/\delta) + \exp -2(t/\delta)}\right] \text{ H}$$

(i) Low freq $f < \rho/\pi\mu t^2$, ie. $\delta \gg t$ $R \approx \rho/t$ Ω
$L \approx \rho/2\pi f t$ H

(ii) High freq , $R \approx \rho/\delta$, $L \approx \rho/2\pi f \delta$ (Skin effect)

Notes: $\frac{\mu_0}{2\pi} = 2\text{nH/cm} = 5.08\text{nH/in}$

Self-inductance $L_s = L_{si} + L_{se}$

internal $\rightarrow 0$ at $f \rightarrow \infty$

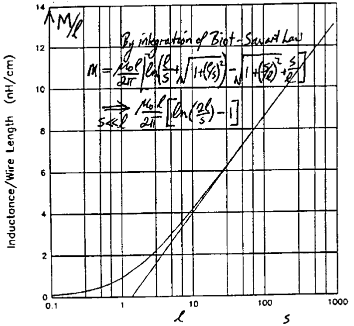
external

$L_{si} = \frac{\mu_0}{2\pi} \cdot \frac{\ell}{4}$

L_{se} = Mutual inductance at $s = r$ from center ie. at surface

for round wire radius r length ℓ

$\approx \frac{\mu_0 \ell}{2\pi}\left[\ln\left(\frac{2\ell}{r}\right) - 1\right]$ for $r \ll \ell$



By integration of Biot-Savart Law

$M = \frac{\mu_0 \ell}{2\pi}\left[\ln\left(\frac{\ell}{s} + \sqrt{1 + (\ell/s)^2}\right) - \sqrt{1 + (s/\ell)^2} + \frac{s}{\ell}\right]$

$\xrightarrow[s \ll \ell]{} \frac{\mu_0 \ell}{2\pi}\left[\ln\left(\frac{2\ell}{s}\right) - 1\right]$

Figure A8.1 Mutual inductance *M* per unit wire length. The lower line is the long-wire approximation. See text to adapt for total self-inductance per unit wire length

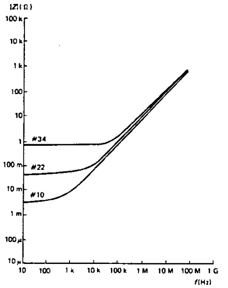


Figure D-2 Impedance of 1 m-long round copper wires

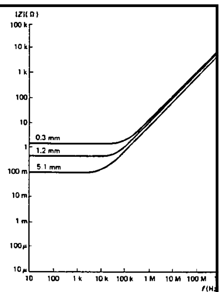


Figure D-4 Impedance of 1-m-long 36-μm-thick PCB lands

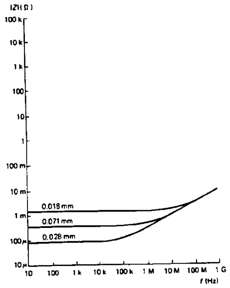


Figure D-6 Impedance of copper groundplanes

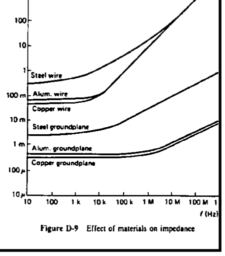
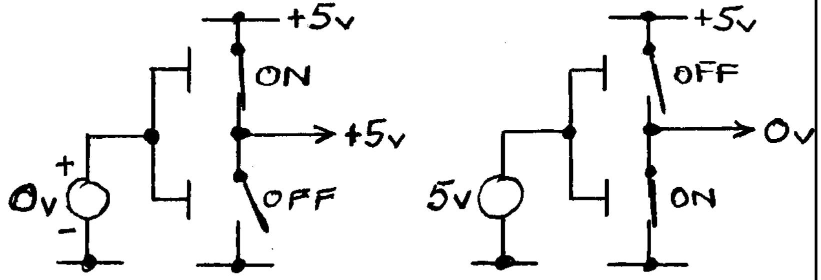


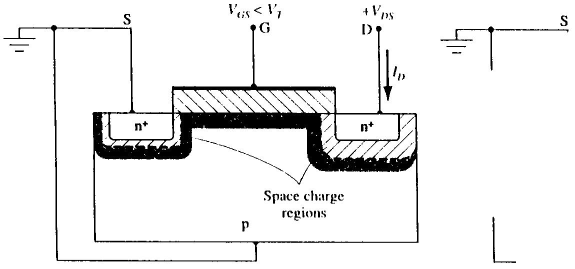
Figure D-9 Effect of materials on impedance

E
F

5. MOS devices and CMOS



N-channel enhancement MOSFET: $V_{DS} \approx 0$



(a)

Figure 10.36 The n-channel enhancement mode MOSFET (a) with an applied and (b) with an applied gate voltage $V_{GS} > V_T$

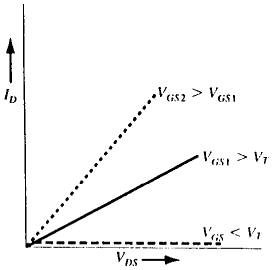


Figure 10.37 I_D versus V_{DS} characteristics for small values of V_{DS} at three V_{GS} voltages

MOSFET operation

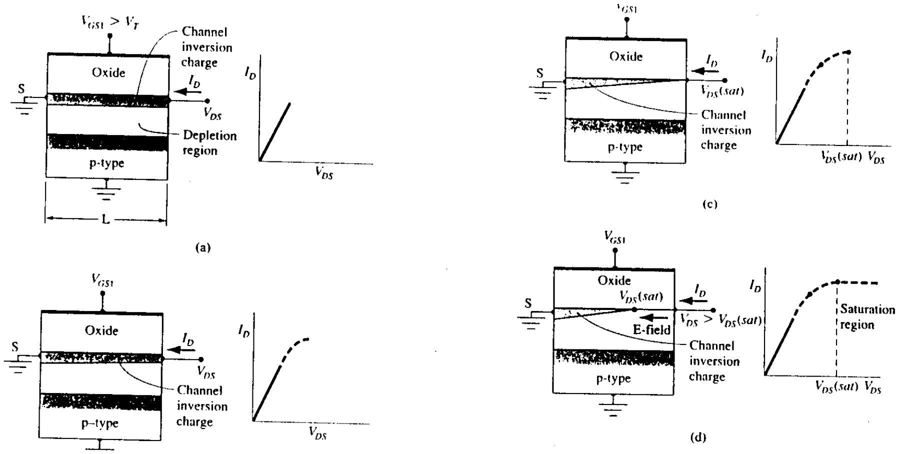


Figure 10.38 Cross section and I_D versus V_{DS} curve when $V_{GS} > V_T$ for (a) a small V_{DS} valu (b) a larger V_{DS} value, (c) a value of $V_{DS} = V_{DS}(sat)$, and (d) a value of $V_{DS} > V_{DS}(sat)$

Enhancement MOSFET characteristics

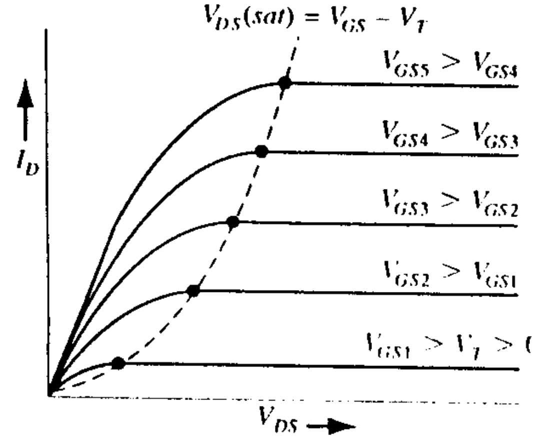


Figure 10.39 Family of I_D versus V_{DS} curves for an n-channel enhancement mode MOSFET

Derivation of MOSFET characteristic equations

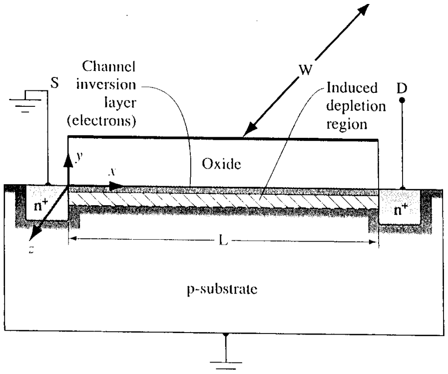


Figure 10.42 Geometry of a MOSFET for I_D versus V_{DS} derivation

$$I(x) = \int_y \int_z J(x)\, dy\, dz$$

$$= W . \mu \int_y \sigma(x) \frac{dV(x)}{dx} . dy$$

$$I(x)\, dx = \mu\, W\, q(x)\, dV(x)$$

$$\text{and} \quad q(x) = \frac{\epsilon_{ox}}{t_{ox}} [V_g - V(x)]$$

$$= C_{ox} [(V_g - V_T) - V(x)]$$

$$I_{DS} \int_0^L dx = \mu W C_{ox} \int_0^{V_{DS}} [(V_g - V_T) - V(x)] dV_x$$

$$I_{DS} . L = \mu W C_{ox} [(V_g - V_T) V_{DS} - V_{DS}^2/2]$$

$$I_{DS} = \frac{\mu}{2} \frac{W}{L} C_{ox} [2(V_g - V_T) - V_{DS}] V_{DS}$$

$$\frac{\partial I_{DS}}{\partial V_{DS}} = \mu \frac{W}{L} C_{ox} [(V_g - V_T) - V_{DS}]$$

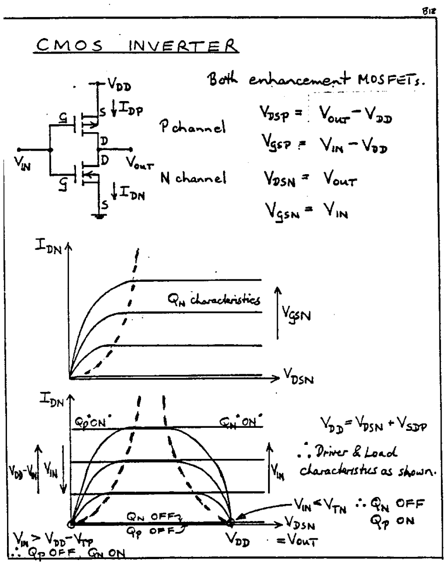
$$\longrightarrow 0 \text{ when } V_{DS} = V_g - V_T$$

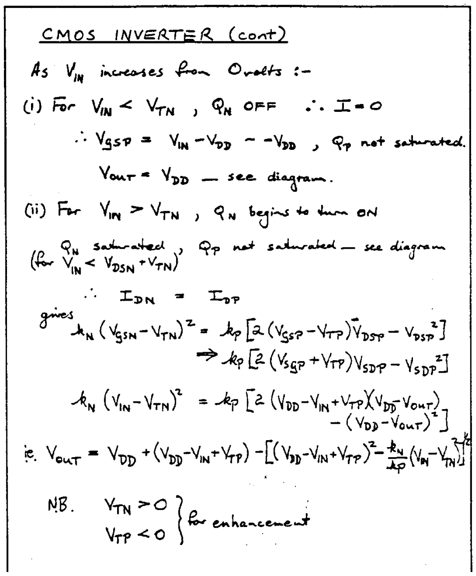
$$\text{Substitute: } I_{DS}]_{SAT} = \frac{\mu}{2} \frac{W}{L} C_{ox} (V_g - V_T)^2$$

$$= \frac{\mu}{2} \frac{W}{L} C_{ox} V_{DS}^2$$

Now set $(\mu W/2L)C_{ox} = k$ →

CMOS dynamic characteristics (part 1)





CMOS INVERTER (cont)

As V_{IN} increases from 0 volts :-

(i) For $V_{IN} < V_{TN}$, Q_N OFF ∴ $I = 0$

∴ $V_{GSP} = V_{IN} - V_{DD} \sim -V_{DD}$, Q_P not saturated.

$V_{OUT} = V_{DD}$ — see diagram.

(ii) For $V_{IN} > V_{TN}$, Q_N begins to turn ON

Q_N saturated (for $V_{IN} < V_{DSN} + V_{TN}$), Q_P not saturated — see diagram

∴ $I_{DN} = I_{DP}$

gives $k_N (V_{GSN} - V_{TN})^2 = k_P [2(V_{GSP} - V_{TP}) V_{DSP} - V_{DSP}^2]$

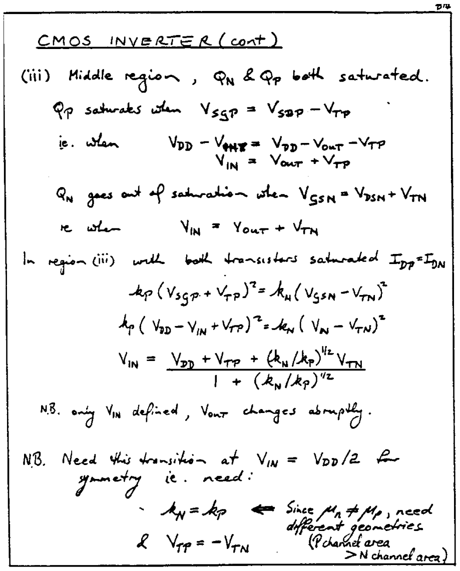
$\Rightarrow k_P [2(V_{SGP} + V_{TP}) V_{SDP} - V_{SDP}^2]$

$$k_N (V_{IN} - V_{TN})^2 = k_P [2(V_{DD} - V_{IN} + V_{TP})(V_{DD} - V_{OUT}) - (V_{DD} - V_{OUT})^2]$$

$$\text{ie. } V_{OUT} = V_{DD} + (V_{DD} - V_{IN} + V_{TP}) - [(V_{DD} - V_{IN} + V_{TP})^2 - \frac{k_N}{k_P}(V_{IN} - V_{TN})^2]^{1/2}$$

N.B. $\left.\begin{matrix} V_{TN} > 0 \\ V_{TP} < 0 \end{matrix}\right\}$ for enhancement

CMOS dynamic characteristics (part 2)



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CMOS INVERTER (cont)

(iii) Middle region, Q_N & Q_P both saturated.

Q_P saturates when $V_{SGP} = V_{SDP} - V_{TP}$

i.e. when $V_{DD} - V_{IN} = V_{DD} - V_{OUT} - V_{TP}$

$V_{IN} = V_{OUT} + V_{TP}$

Q_N goes out of saturation when $V_{GSN} = V_{DSN} + V_{TN}$

ie when $V_{IN} = V_{OUT} + V_{TN}$

In region (iii) with both transistors saturated $I_{DP} = I_{DN}$

$$k_P (V_{SGP} + V_{TP})^2 = k_N (V_{GSN} - V_{TN})^2$$

$$k_P (V_{DD} - V_{IN} + V_{TP})^2 = k_N (V_{IN} - V_{TN})^2$$

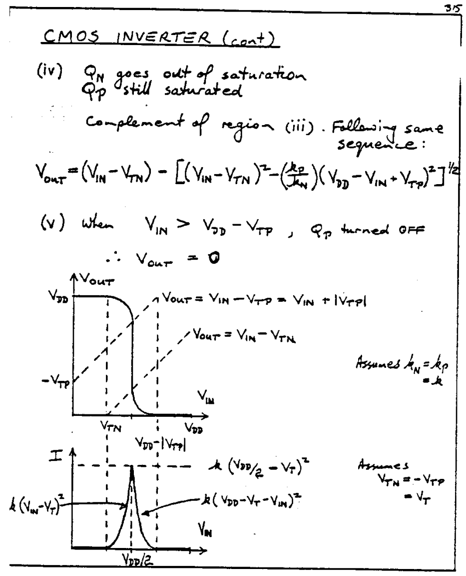
$$V_{IN} = \frac{V_{DD} + V_{TP} + (k_N/k_P)^{1/2} V_{TN}}{1 + (k_N/k_P)^{1/2}}$$

N.B. only V_{IN} defined, V_{OUT} changes abruptly.

N.B. Need this transition at $V_{IN} = V_{DD}/2$ for symmetry ie. need:

$k_N = k_P$ ⟸ Since $\mu_n \neq \mu_p$, need different geometries (P channel area > N channel area)

& $V_{TP} = -V_{TN}$



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CMOS INVERTER (cont)

(iv) Q_N goes out of saturation
Q_P still saturated

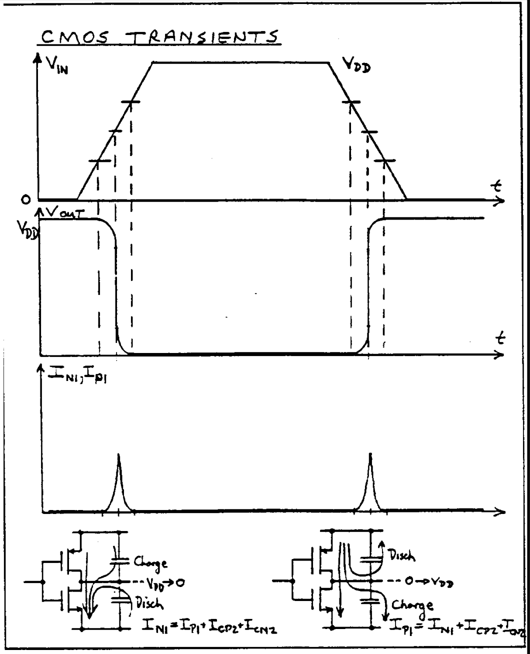
Complement of region (iii). Following same sequence:

$$V_{OUT} = (V_{IN} - V_{TN}) - \left[(V_{IN} - V_{TN})^2 - \left(\frac{k_P}{k_N}\right)(V_{DD} - V_{IN} + V_{TP})^2\right]^{1/2}$$

(v) When $V_{IN} > V_{DD} - V_{TP}$, Q_P turned OFF

$\therefore V_{OUT} = 0$

Switching current (1)



Switching current (2)

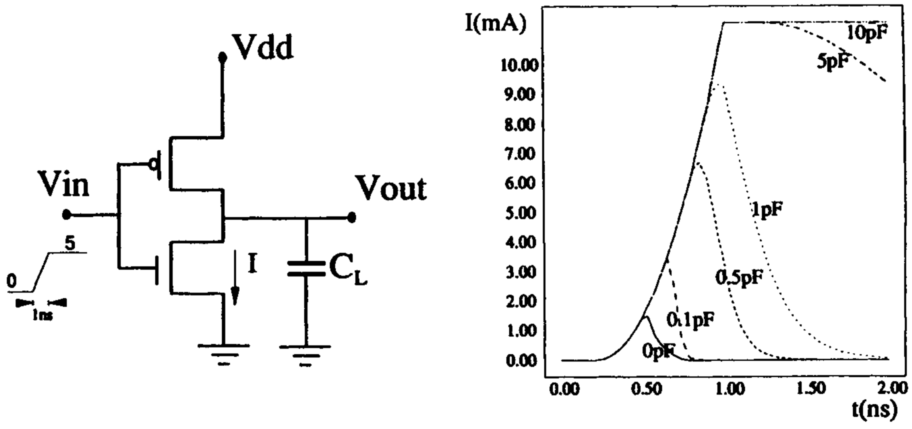


Figure 2.75 N-channel MOSFET current for various sizes of C_L.

CMOS inverter:

VLSI layout & structure

N-WELL CMOS TECHNOLOGY 191

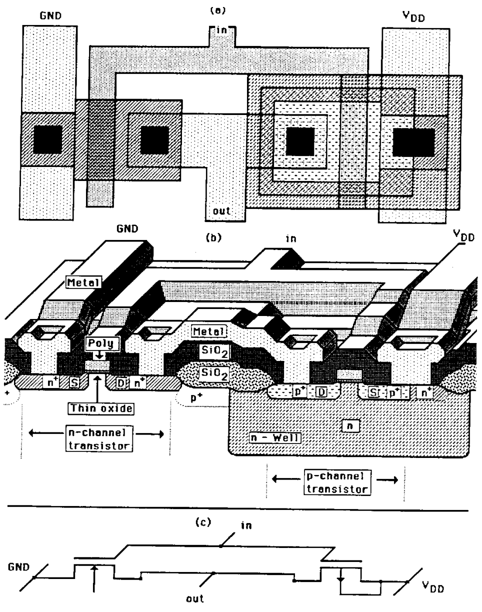
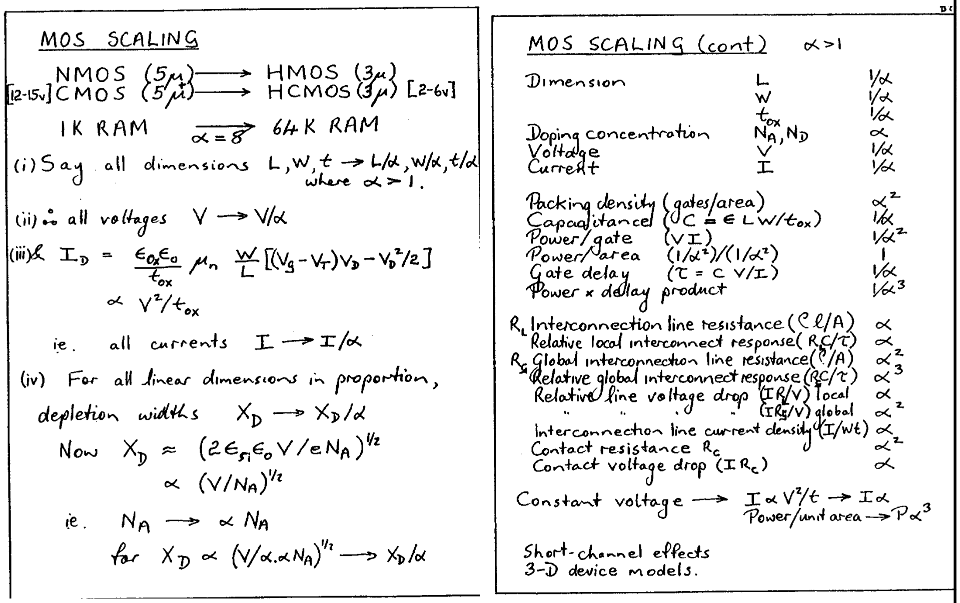


Figure 5-12: CMOS inverter. Composite layout (a), cross-section (b), and electrical diagram (c).



MOS SCALING

NMOS (5μ) ⟶ HMOS (3μ)
[12-15v] CMOS (5μ) ⟶ HCMOS (3μ) [2-6v]

1K RAM $\xrightarrow[\alpha=8]{}$ 64K RAM

(i) Say all dimensions $L, W, t \rightarrow L/\alpha, W/\alpha, t/\alpha$ where $\alpha > 1$.

(ii) ∴ all voltages $V \longrightarrow V/\alpha$

(iii) & $I_D = \frac{\epsilon_{ox}\epsilon_0}{t_{ox}} \mu_n \frac{W}{L}[(V_g - V_T)V_D - V_D^2/2]$

$\propto V^2/t_{ox}$

ie. all currents $I \longrightarrow I/\alpha$

(iv) For all linear dimensions in proportion, depletion widths $X_D \longrightarrow X_D/\alpha$

Now $X_D \approx (2\epsilon_{si}\epsilon_0 V/eN_A)^{1/2}$

$\propto (V/N_A)^{1/2}$

ie. $N_A \longrightarrow \alpha N_A$

for $X_D \propto (V/\alpha.\alpha N_A)^{1/2} \longrightarrow X_D/\alpha$

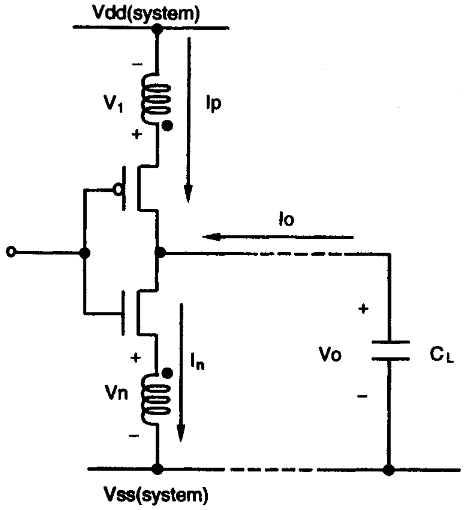
MOS SCALING (cont) $\alpha > 1$

Dimension	L	$1/\alpha$
	W	$1/\alpha$
	t_{ox}	$1/\alpha$
Doping concentration	N_A, N_D	α
Voltage	V	$1/\alpha$
Current	I	$1/\alpha$
Packing density (gates/area)		α^2
Capacitance ($C = \epsilon LW/t_{ox}$)		$1/\alpha$
Power/gate (VI)		$1/\alpha^2$
Power/area ($(1/\alpha^2)/(1/\alpha^2)$)		1
Gate delay ($\tau = CV/I$)		$1/\alpha$
Power × delay product		$1/\alpha^3$
R_L Interconnection line resistance ($\rho l/A$)		α
Relative local interconnect response ($R_L C/\tau$)		α
R_G Global interconnection line resistance (ρ/A)		α^2
Relative global interconnect response ($R_G C/\tau$)		α^3
Relative line voltage drop (IR_L/V) local		α
" " " " (IR_G/V) global		α^2
Interconnection line current density (I/Wt)		α
Contact resistance R_c		α^2
Contact voltage drop (IR_c)		α

Constant voltage ⟶ $I \propto V^2/t \rightarrow I\alpha$
Power/unit area ⟶ $P\alpha^3$

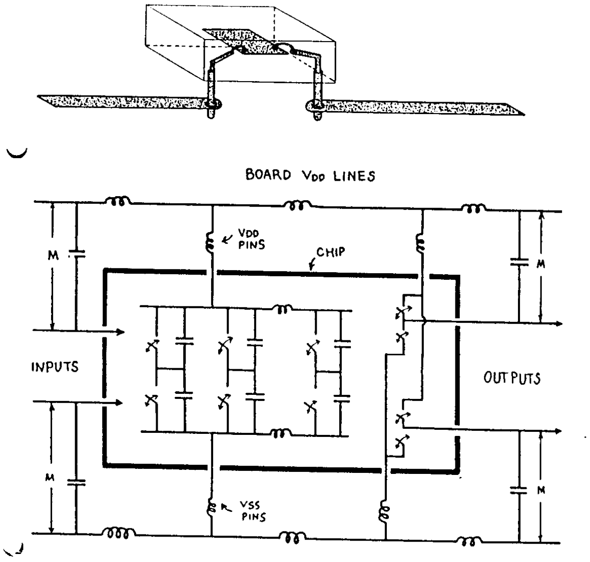
Short-channel effects
3-D device models.

6. Delta-I (ΔI) switching noise



$\Delta V = L\, di/dt$

Figure 2.83 Driver circuit for the calculation of the mutual effect between L_{vss} and L_{vdd} on V_n.



BOARD V_{SS} LINES

GURE 7.10 Power-distribution path in an integrated circuit. The IC die, nding wire, distribution layer on the chip carrier, and the package pins and wer lines on the board are shown. The electrical model of this structure is strated at the bottom. Here M represents the mutual inductance between the nal and power/ground planes.

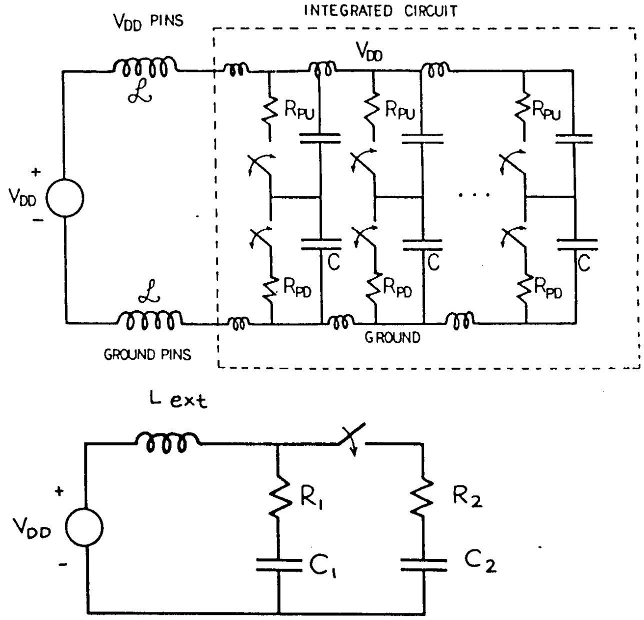


FIGURE 7.11 Electrical model for the on-chip circuitry of a CMOS ch a detailed model, (bottom) a simplified model

Example to show typical values

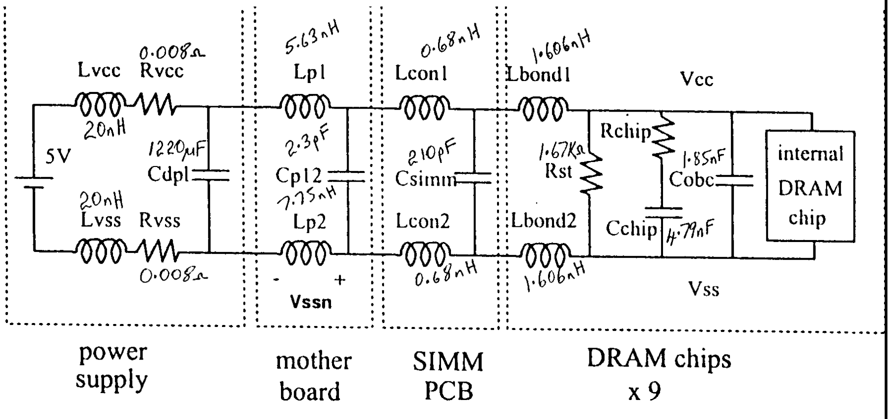
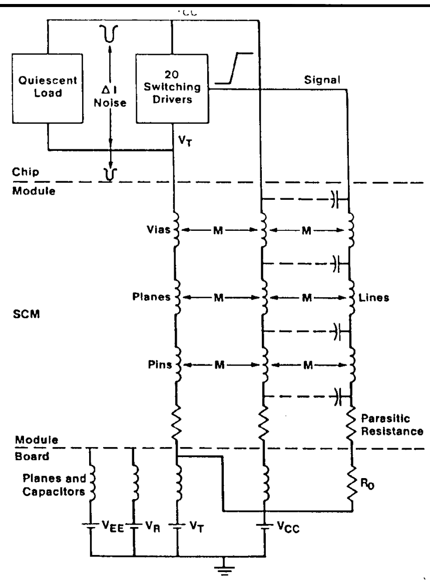


Fig. 15. Simplified equivalent circuit of the test setup shown in Fig. 14.



Mutual Inductances

Figure 3-15. Equivalent Circuit of Package. Used for Determining L_{eff}.