Lecture Objectives

• Introduce first-level interconnect technologies:
  – wire-bond, TAB & flip-chip
• Introduce standard SMT & PTH packages
  – (surface mount technology & pin through hole)
• Introduce MCM, COB, DCA, CSP, WLP, etc
  – (multi-chip modules, chip on board, direct chip attach, chip-scale package, wafer-level packaging)
• Introduce basic packaging acronyms
Packaging Technologies

- Single-chip packages (SCPs)
- Multi-chip modules (MCMs)
- Encapsulation
- Wire Bond
- TAB (tape automated bonding)
- Flip-Chip
- New developments (SiP, PoP, etc)

Single-Chip Packages:

- 1st level interconnects: wire-bond, TAB, FC
- 2nd level interconnects: PTH & SMT
- MCMs (multi-chip modules)
- DCA (direct chip attach)
- CSP (chip scale packages)
**FIGURE 1-12.** Cutaway view of a postmolded plastic package in the configuration of a dual-line package (DIP).

- Dual-in-line (DIL) plastic package (DIP)

**First-level interconnect**

**Figure 1-2** Common types of first level connections. Chip to common circuit base. (Courtesy E. Larson).

- Wirebond
- TAB
- Flip-chip
  - (Tape-automated bonding)
Figure 1.1 Cross-section of a typical plastic-encapsulated single-chip package

Figure 1.2 Cross-section of a typical ceramic single-chip package
Figure 1.3 Cross-section of a typical metal single-chip package

Second-level package attach

FIGURE 1-6. A multilayer circuit board showing the attachment of through-hole and surface mount packages. Surface mounting allows attachment of components to both sides of the board and a higher wiring density in the board since it permits blind vias that do not occupy the grid point throughout the entire board depth.

- SMT & PTH
Substrate Vias

PCB (printed circuit board) or PWB (printed wiring board)
Multi-layer laminate
Drilled, electroplated Cu
Copper paste (ALIVH), silver loaded (ECA) epoxies, etc

Das et al, ECTC 2009, 591-598

BaTiO₃ NPs
## Through-hole Mount Packages

<table>
<thead>
<tr>
<th>Package Type</th>
<th>Shape</th>
<th>Typical Features</th>
<th>Material</th>
<th>Lead pitch</th>
<th>Number of Pins</th>
</tr>
</thead>
<tbody>
<tr>
<td>DIP</td>
<td>Double in-line package</td>
<td>2.54 mm (0.100 in)</td>
<td>Ceramic</td>
<td>8 - 64</td>
<td></td>
</tr>
<tr>
<td>SIP</td>
<td>Single in-line package</td>
<td>3.96 mm (0.156 in)</td>
<td>Plastic</td>
<td>3 - 25</td>
<td></td>
</tr>
<tr>
<td>ZIP</td>
<td>Zif (Zero insertion force) package</td>
<td>2.54 mm (0.100 in)</td>
<td>Plastic</td>
<td>16 - 28</td>
<td></td>
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<tr>
<td>S-DIP</td>
<td>Single dual in-line package</td>
<td>2.54 mm (0.100 in)</td>
<td>Plastic</td>
<td>20 - 64</td>
<td></td>
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<tr>
<td>SK-DIP</td>
<td>Small dual in-line package</td>
<td>2.34 mm (0.092 in)</td>
<td>Ceramic</td>
<td>24 - 32</td>
<td></td>
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<tr>
<td>PGA</td>
<td>Pin grid array</td>
<td>2.54 mm (0.100 in)</td>
<td>Ceramic</td>
<td>32 - 200</td>
<td></td>
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</tbody>
</table>

## Surface Mount Packages

<table>
<thead>
<tr>
<th>Package Type</th>
<th>Shape</th>
<th>Typical Features</th>
<th>Material</th>
<th>Lead pitch</th>
<th>Number of Pins</th>
</tr>
</thead>
<tbody>
<tr>
<td>SOP</td>
<td>Small outline package</td>
<td>1.27 mm (0.050 in)</td>
<td>Plastic</td>
<td>8 - 40</td>
<td></td>
</tr>
<tr>
<td>QFP</td>
<td>Quad flat package</td>
<td>0.5 mm</td>
<td>Plastic</td>
<td>48 - 200</td>
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<tr>
<td>FFP</td>
<td>Flat package of flex</td>
<td>1.27 mm (0.050 in)</td>
<td>Ceramic</td>
<td>20 - 80</td>
<td></td>
</tr>
<tr>
<td>LCC</td>
<td>Leadless chip carrier</td>
<td>1.27 mm (0.050 in)</td>
<td>Ceramic</td>
<td>20 - 40</td>
<td></td>
</tr>
<tr>
<td>P-LCC</td>
<td>Plastic leadless chip carrier</td>
<td>1.27 mm (0.050 in)</td>
<td>Ceramic</td>
<td>16 - 134</td>
<td></td>
</tr>
<tr>
<td>VQFP</td>
<td>Very small outline flat package</td>
<td>0.4 mm</td>
<td>Ceramic</td>
<td>32 - 200</td>
<td></td>
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</tbody>
</table>

**FIGURE 3.10** Various types of integrated circuit packages and mounting techniques: (a) Dual-in-line package (DIP), (b) pin grid array (PGA), (c) J-lead, (d) Gull-wing, (e) leadless chip carrier, (f) gull-wing/leadless chip carrier, (g) flip-chip mounting with collapsible solder balls, and (h) tape-automated bonding (TAB) applied directly on the PC board.
Cavity-down BGAs like ASAT's flex-tape BGA (FTBGA) let the chip dissipate heat through the top of the package with the help of a copper heat-spreader. Die-bonding wires are connected to the same side of the substrate as solder balls, so signals don’t have to pass through vias. Although more expensive than cavity-up PBGAs, cavity-down designs can house higher power, higher performance devices for a lot less than the cost of a ceramic BGA.

- BGA packages

Basic MCM/Microsystem concept

**Figure 1-1** MCM architecture (schematic).
Figure 9-12. Thin-Film Multichip Package. After Jensen, Ref. [42], 1986.

- Cu/PI thin-film MCM-D

Figure 2-14a Schematic of workstation module.

- Flip-chip (C4) BGA (C5) MCM-C
• Standard package MCMs (MCM-C or MCM-L)
Figure 13.61 Cost comparison between various multichip packages [13.7].
Encapsulation: “Glob-top”

Figure 15.14 Glob-topping a ball grid array (BGA) device.

COB/DCA encapsulation

- Syringe dispense

Figure 6-40. TAB Encapsulation. A single-orifice nozzle dispenses encapsulant on the bonded chip.
• Squeegee print

Encapsulation: Cavity-fill
Encapsulation: Transfer molding

(a)  
(b)  
(c)  
(d)  

Encapsulation: Underfill

Underfill

Solders
Ball

Interposer

Solder Ball

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• Underfill (flip-chip)

Figure 1: DCA General Process Flow
Table 1: CSP Package Classification

<table>
<thead>
<tr>
<th>Category</th>
<th>Type</th>
<th>Example</th>
<th>Companies</th>
</tr>
</thead>
<tbody>
<tr>
<td>Flip Chip</td>
<td>TAB, Flip chip</td>
<td><img src="image1" alt="Example" /></td>
<td>GE, Sony, Mitsubishi, NEC, Texas Instruments, and licensees</td>
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<tr>
<td></td>
<td>Wire Bonding</td>
<td><img src="image2" alt="Example" /></td>
<td>Fujitsu, Mitsubishi, Sharp, Texas Instruments, and others</td>
</tr>
<tr>
<td>Flex Substrate</td>
<td>Flip chip</td>
<td><img src="image3" alt="Example" /></td>
<td>Citizen Watch, Kyocera, Matsushita, Motorola, Infineon, Infineon Electric, Toshiba, Sony</td>
</tr>
<tr>
<td></td>
<td>Wire Bonding</td>
<td><img src="image4" alt="Example" /></td>
<td>Amkor, Anaren, Fujitsu, National Semiconductor, NEC, Sony</td>
</tr>
<tr>
<td>Custom Lead Frame</td>
<td>TAB, Flip chip</td>
<td><img src="image5" alt="Example" /></td>
<td>Rohm</td>
</tr>
<tr>
<td></td>
<td>Wire Bonding</td>
<td><img src="image6" alt="Example" /></td>
<td>Amkor, Anaren, Fujitsu, Hitachi, OKI, LG Semiconductor, Toshiba</td>
</tr>
<tr>
<td>Wire Level Assembly</td>
<td>Redistribution</td>
<td><img src="image7" alt="Example" /></td>
<td>ChipWorks, EPIC, IME (Sing), NEC, Sandia Labs, Lattice</td>
</tr>
<tr>
<td></td>
<td>Substrate</td>
<td><img src="image8" alt="Example" /></td>
<td>ChipWorks and licensees, ChipWorks Technology</td>
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</table>

Source: TechSearch International, Inc.

32
In Tessera’s Micro BGA (μBGA), a layer of compliant silicone elastomer absorbs the shear stress caused by thermal-expansion mismatch between the silicon die and the organic interconnect. The S-shaped ribbon leads, supported by the compliant silicone encapsulant, accommodate the bending forces.

Figure 1: Schematic of a SLICC package.
Fig. 1  Perspective view of the molded chip scale package

Wire Bond
Figure 5.1 Geometric parameters of a typical wirebonded structure

Figure 2-7b State of the art wire bonding (1.25 mil Al wire, 465 I/O, 4.8 mil pitch).
Figure 3.4 Ultrasonic wedge bonding: (a) ultrasonic wedge bonding tool with typical dimensions; (b) ultrasonic wedge bonding process.
Figure 14.1 Effect of the position of the hook on the bond-pull force
Figure 8-16. Idealized Wirebond Configuration. A transverse load is applied to the wirebond. The top figure illustrates the vertical projection of the wire and the melt front approaching at a mean velocity $u$. Deflection $H_0$ illustrated for increasing higher flow Reynolds numbers to show the ultimate collapse of the wire. For a package with a pad spacing of 0.254 mm, wire sweep occurs at $Re = 0.0156$. This critical value is governed by the wire properties, the flow characteristics, and the package configuration.
Figure 9-12 Schematic illustration of the TAB concept.

Figure 9-16 Important features of a TAB tape design.

- TAB tape chip carrier
- Inner lead bonding (to chip)

Figure 4-19  Details of chip in position for ILB.

Figure 4-18  Inner lead bonding process. (a) Film tape with speckled holes. (b) Overall process and enlarged view of tape leads and bond; (c) Inner lead bonding with thermode down, support carrier up; (d) Chip attached to tape with thermode up, support carrier down; (e) Balancing to next chip bonding position.

• Outer lead excision, bending, attach to board

Figure 4-26. Steps of outer lead bonding: (a) excising; (b) lead forming; (c) transporting; (d) welding or soldering.

• Outer lead bonding (thermode).

Figure 6-41. TAB Outer Lead Bonding (OLB). After the TAB package is excised from the tape and placed on the substrate or board, it is normally solder bonded.

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**TAB variations**

- **Recessed Mount**
- **Flip-TAB Mount**
- **Face-up Mount**

*Figure 6.10* TAB mounting options
Figure 7.9 Wafer bumping process flow
TAB variations

Figure 6.1 Bumped die TAB

Figure 6.2 Bumped lead TAB

Figure 6.4 Bumpless TAB

Substrate

1: Delamination between lead and bonding pad
2: Fracture at outer lead bond heel
3: Fracture near polymeric support ring
4: Delamination between die and bump
5: Delamination between bump and lead
6: Fracture at inner lead bond heel
7: Fracture of lead

Figure 6.8 Potential failure mechanisms and sites in TAB
Figure 1-18. TAB in Consumer Electronics to Supercomputers.
• Self-alignment →

- Solder bumps
- Solder bumps
  - As printed →
  - Re-flowed →
Figure 1-8. Chip Pad Spacing Requirements.
New developments

WLP & Redistribution

FIGURE 10.11 Typical redistribution technology. (Courtesy of i2M Berlin)
Figure 8

Dendrites can be customized to different applications, the
Fig. 1. Intrinsic stress vs Ar pressure for DC magnetron sputtering of 80-20 Mo-Cr alloy (by weight). The exact shape of the curve changes with sputtering conditions and material, but this general behavior is characteristic of metal sputtering. [1, 3]

Fig. 2. Perspective view of spring finger, showing released and stress-relaxed cantilever portion within passivation window area and showing anchored portion to the right.

FIGURE 3.16 Insulated metal substrate
Figure 1.11 NEC’s 3-D stack-up chip scale package (CSP) for memory devices.
Lecture Summary

- Standard packages
  - Encapsulation
- First level interconnect (chip to package):
  - Wire-bond, TAB, flip-chip (C4)
- Second-level interconnect (package to board):
  - PTH, SMT, PGA, BGA (C4/C5), etc
- MCMs, CSPs, WLP, etc

Homework #1

Dally, Lall & Suhling:

Problems:

<table>
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<tr>
<th>Problem</th>
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<th>2.2</th>
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