ECE414/514
Electronics Packaging
Spring 2012 Lecture 2

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Lecture Objectives

- Introduce first-level interconnect technologies:
  - wire-bond, TAB & flip-chip
- Introduce standard SMT & PTH packages
  - (surface mount technology & pin through hole)
- Introduce MCM, COB, DCA, CSP, WLP, etc
  - (multi-chip modules, chip on board, direct chip attach, chip-scale package, wafer-level packaging)
- Introduce basic packaging acronyms

Packaging Technologies

- Single-chip packages (SCPs)
- Multi-chip modules (MCMs)
- Encapsulation
- Wire Bond
- TAB (tape automated bonding)
- Flip-Chip
- New developments (SiP, PoP, etc)

Single-Chip Packages:

- 1st level interconnects: wire-bond, TAB, FC
- 2nd level interconnects: PTH & SMT
- MCMs (multi-chip modules)
- DCA (direct chip attach)
- CSP (chip scale packages)

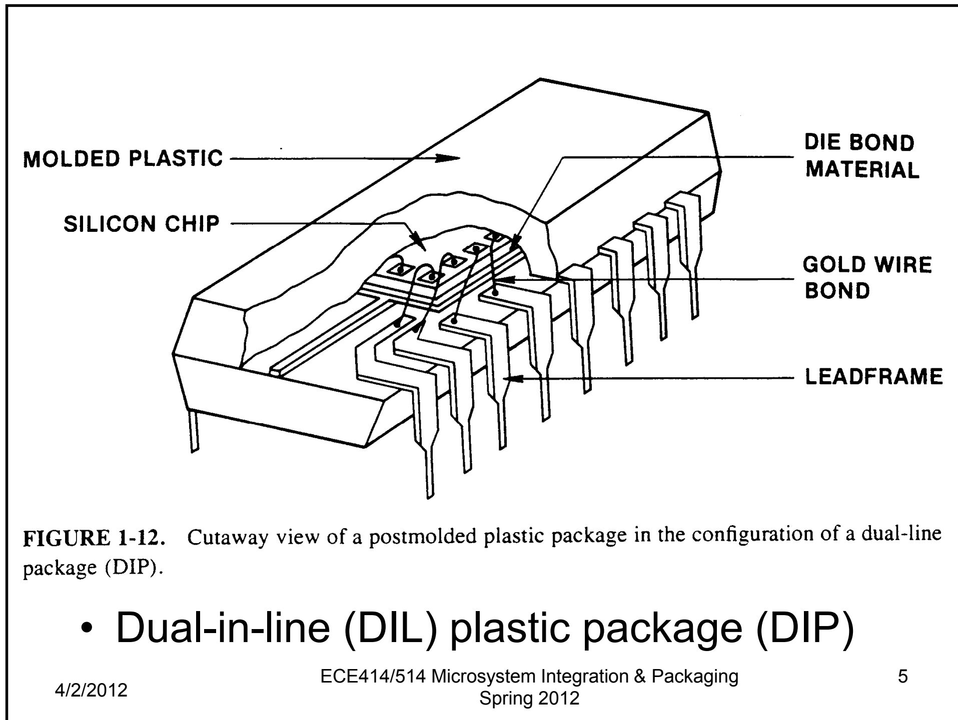

FIGURE 1-12. Cutaway view of a postmolded plastic package in the configuration of a dual-line package (DIP).

- Dual-in-line (DIL) plastic package (DIP)

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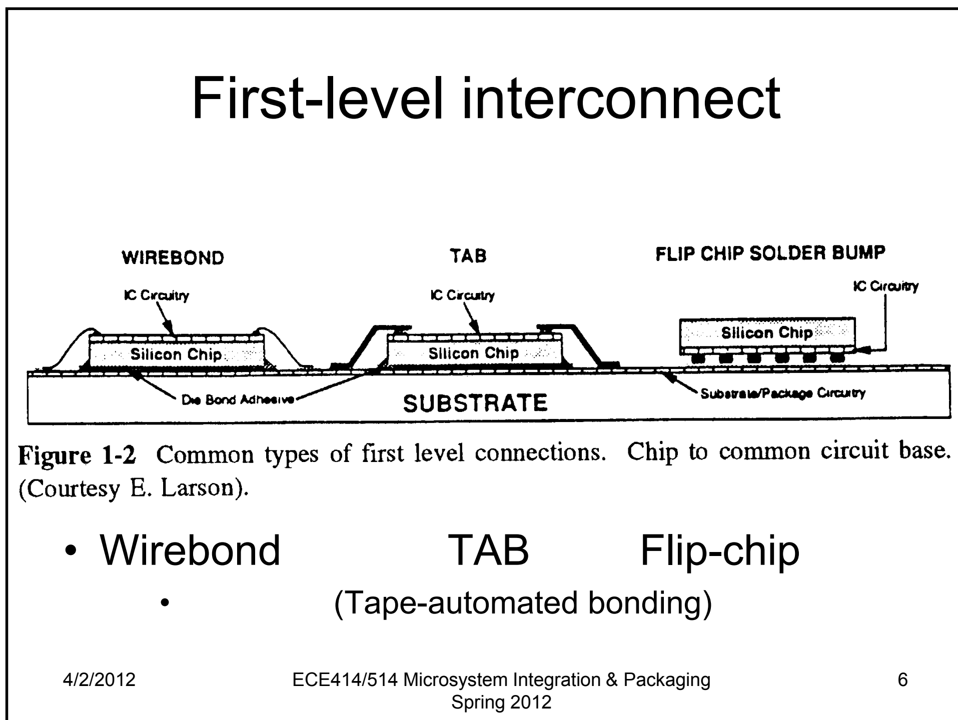

First-level interconnect

Figure 1-2 Common types of first level connections. Chip to common circuit base. (Courtesy E. Larson).

- Wirebond TAB Flip-chip
  - (Tape-automated bonding)

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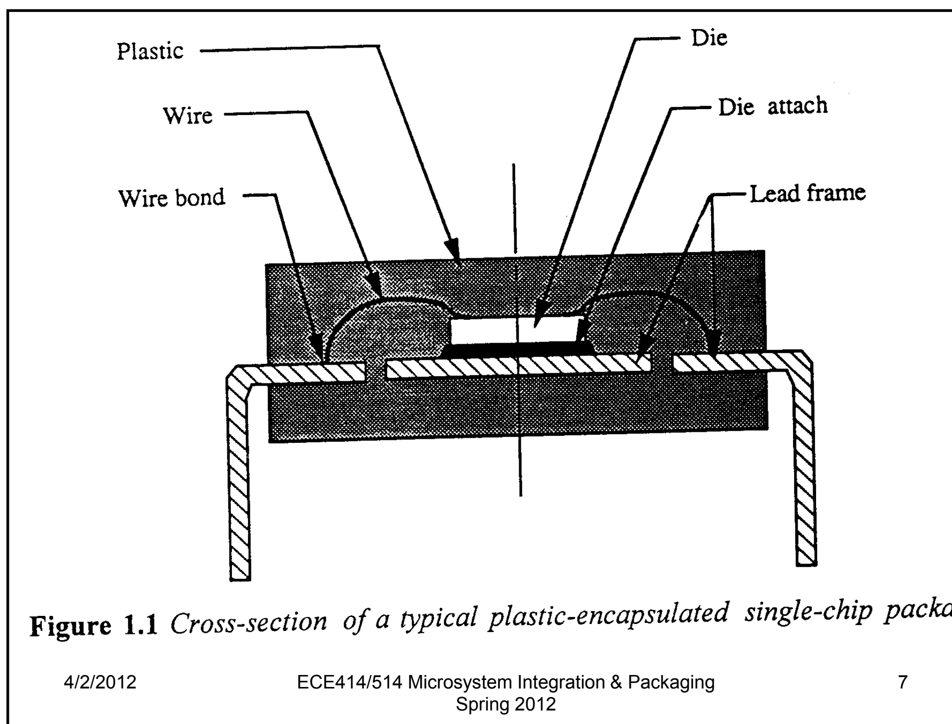


Figure 1.1 *Cross-section of a typical plastic-encapsulated single-chip packag*

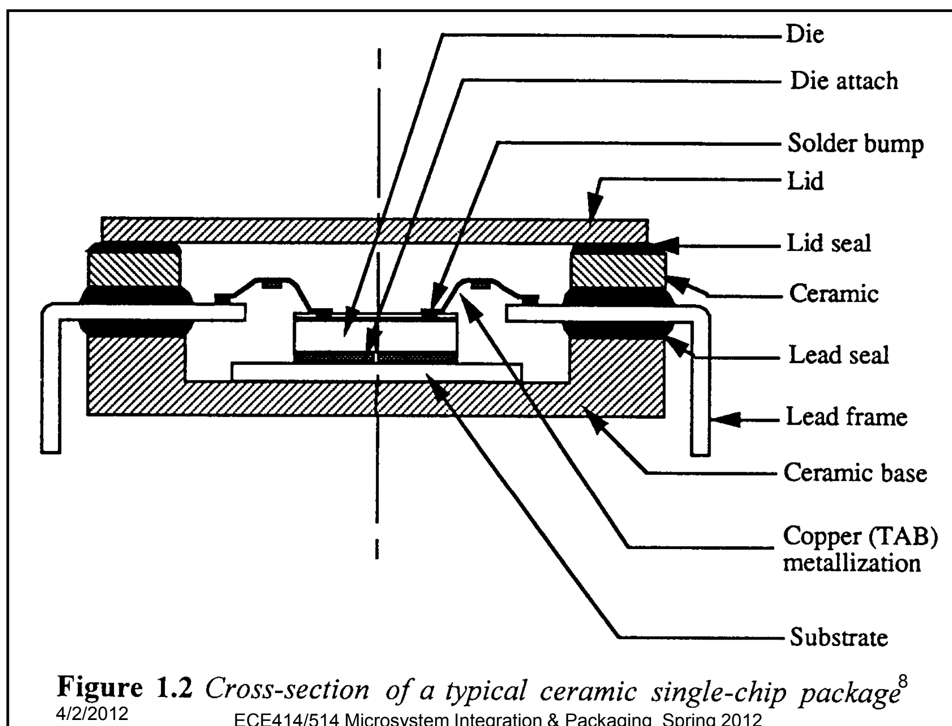


Figure 1.2 *Cross-section of a typical ceramic single-chip package*

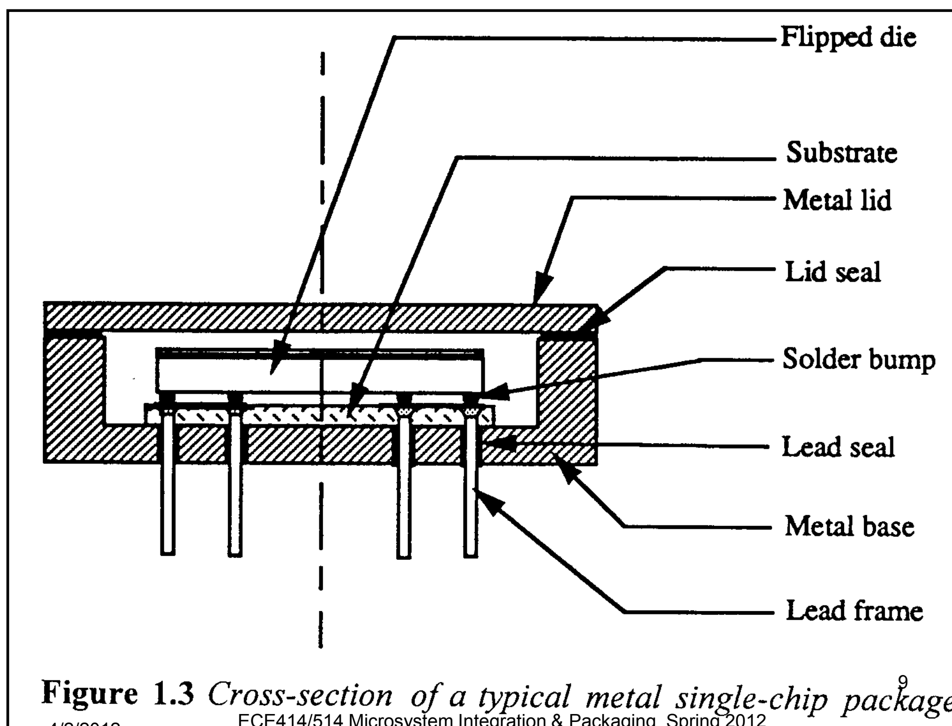


Figure 1.3 *Cross-section of a typical metal single-chip package*

Second-level package attach

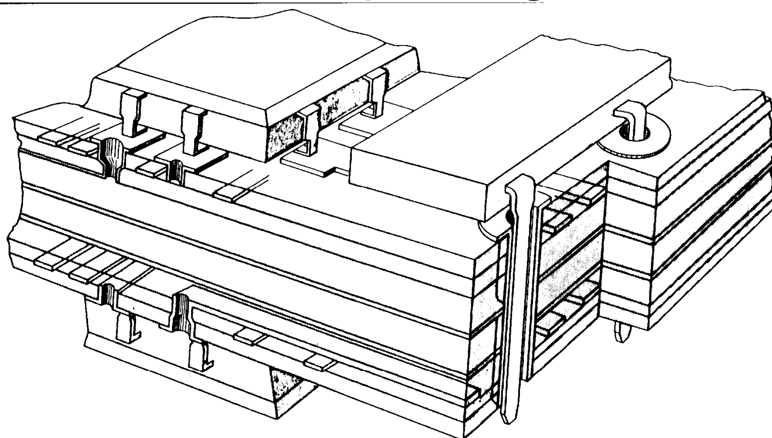
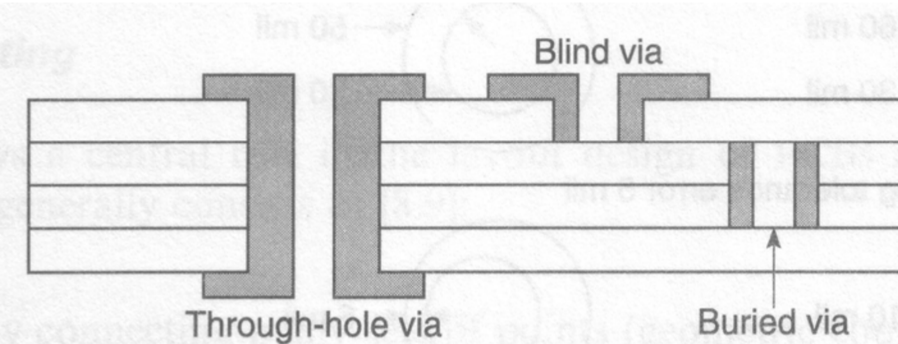


FIGURE 1-6. A multilayer circuit board showing the attachment of through-hole and surface mount packages. Surface mounting allows attachment of components to both sides of the board and a higher wiring density in the board since it permits blind vias that do not occupy the grid point throughout the entire board depth.

- SMT & PTH

Substrate Vias

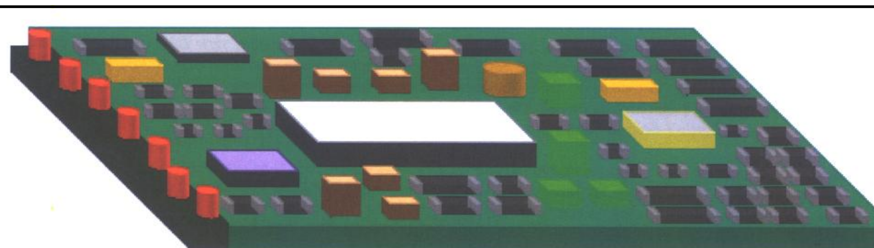


PCB (printed circuit board) or PWB (printed wiring board)

Multi-layer laminate

Drilled, electroplated Cu

Copper paste (ALIVH), silver loaded (ECA) epoxies, etc



Das et al, ECTC 2009, 591-598

Figure 11: PWB vs SiP

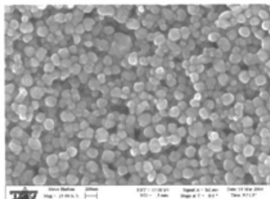


Figure 3: Larger area SEM images of RC3 nanocomposites.

$BaTiO_3$ NPs

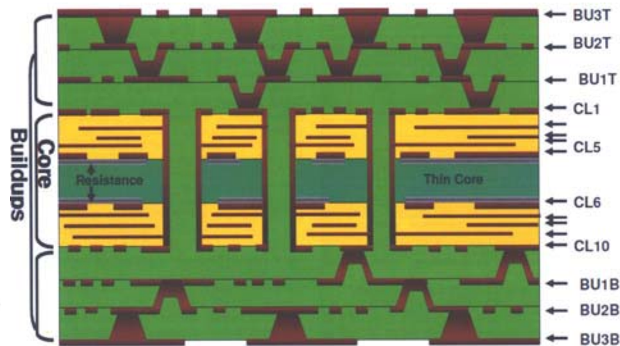


Figure 2: System in a Package (SiP) 3-[10-3] cross section using resin coated copper capacitive (RC3) materials. Substrate cross section ...

Through hole mount	Shape	Typical features		
		Material	Lead pitch	# of I/O pins
DIP Dual in-line package		Ceramic Plastic	• 2.54 mm (100mil)	8 - 64
SIP Single in-line package		Plastic	• 2.54 mm (100mil) • 1 direction lead	3 - 25
ZIP Zigzag in-line package		Plastic	• 2.54 mm (100mil) • 1 direction lead	16 - 24
S-DIP Shrink dual in-line package		Plastic	• 1.778 mm (70mil)	20 - 64
SK-DIP Skinny dual in-line package		Ceramic Plastic	• 2.54 mm • half- size pitch in the width direction	24 - 32
PGA Pin grid array		Ceramic Plastic	• 2.54 mm (100mil)	

Figure 3.6 *Through-hole mount-package profiles*

Surface mount	Shape	Typical features		
		Material	Lead pitch	# of I/O pins
SOP Small outline package		Plastic	• 1.27mm (50mil) • 2 direction lead	8 - 40
QFP Quad flat-pack		Plastic	• 1.0 mm • 0.8 mm • 0.65 mm • 4 direction lead	88 - 200
FPG Flat package of glass		Ceramic	• 1.27 mm (50mil) • 0.762mm (30mil) • 2 direction lead • 4 direction lead	20 - 80
LCC Leadless chip carrier		Ceramic	• 1.27mm (50mil) • 1.016mm (40mil) • 0.762mm (30mil)	20 - 40
PLCC Plastic leaded chip carrier		Ceramic	• 1.27mm (50mil) • j-shaped bend • 4 direction lead	18 - 124
VSQF Very small quad flatpack		Ceramic	• 0.5mm	32 - 200

Figure 3.7 *Surface-mount package profiles*

- PTH
- PGA
- SMT:
  - J-lead
  - Gull-wing
  - Leadless
- COB/DCA
  - flip-chip
  - TAB

PACKAGE
LEAD
SOLDER
PC BOARD
(a)
(b)
(c)
(d)
(e)
(f)
(g)

FIGURE 3.10 Various types of integrated circuit packages and mounting techniques: (a) Dual-in-line package (DIP), (b) pin grid array (PGA), (c) J-leaded chip carrier, (d) gull-wing-leaded chip carrier, (e) leadless chip carrier, (f) flip-chip mounting with collapsible solder balls, and (g) tape-automated bonding (TAB) applied directly on the PC board

Copper heat spreader
Die
Die-attach epoxy
Nickel surface
Solder ball
Signal-line wire bond
Solder mask
Encapsulant
Ground-line wire bond
Copper line layer
Polyimide layer
Adhesive

Cavity-down BGAs like ASAT's flex-tape BGA (FTBGA) let the chip dissipate heat through the top of the package with the help of a copper heat-spreader. Die-bonding wires are connected to the same side of the substrate as solder balls, so signals don't have to pass through vias. Although more expensive than cavity-up PBGAs, cavity-down designs can house higher power, higher performance devices for a lot less than the cost of a ceramic BGA.

- BGA packages

Basic MCM/Microsystem concept

FIRST LEVEL CONNECTION
SECOND LEVEL CONNECTION
CHIP
CHIP
CHIP
COMMON CIRCUIT BASE
MCM PACKAGE
PRINTED WIRING BOARD (PWB)

Figure 1-1 MCM architecture (schematic).

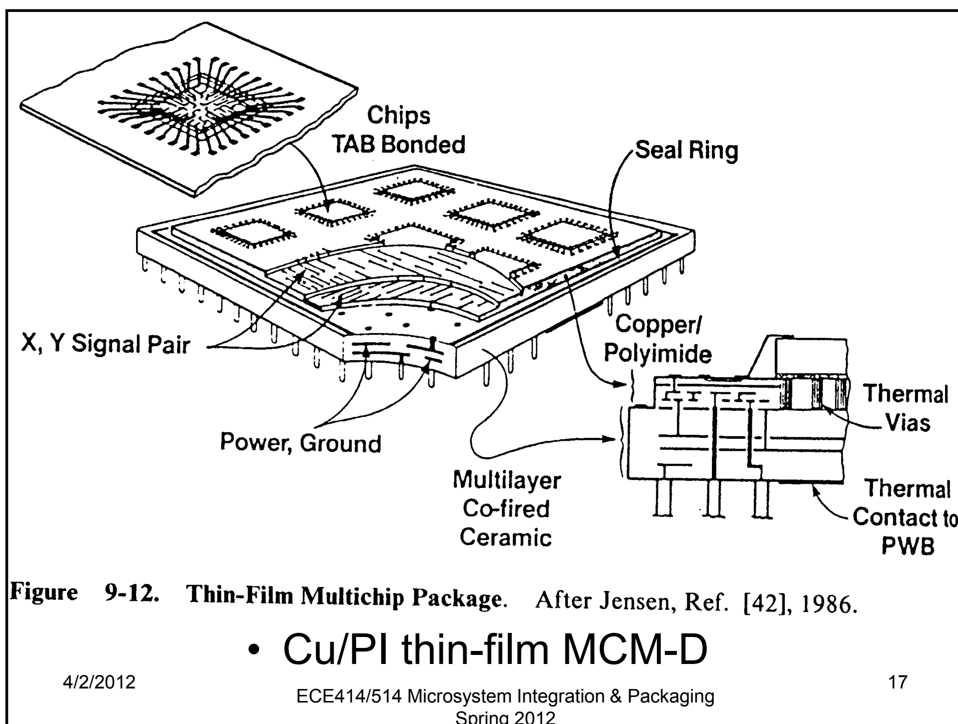


Figure 9-12. Thin-Film Multichip Package. After Jensen, Ref. [42], 1986.

- Cu/PI thin-film MCM-D

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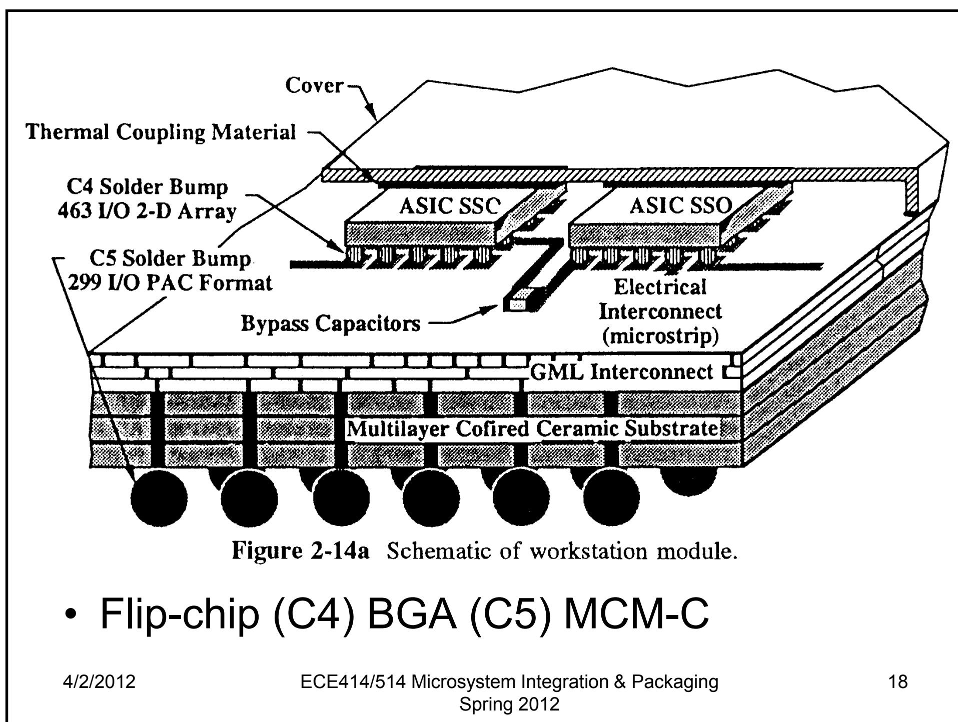

Figure 2-14a Schematic of workstation module.

- Flip-chip (C4) BGA (C5) MCM-C

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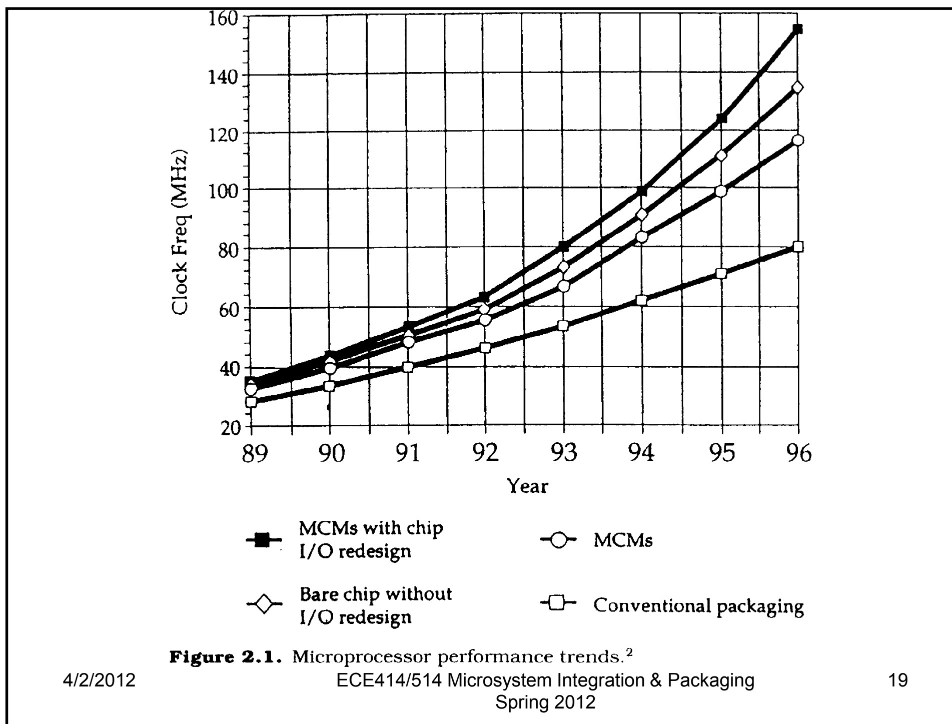
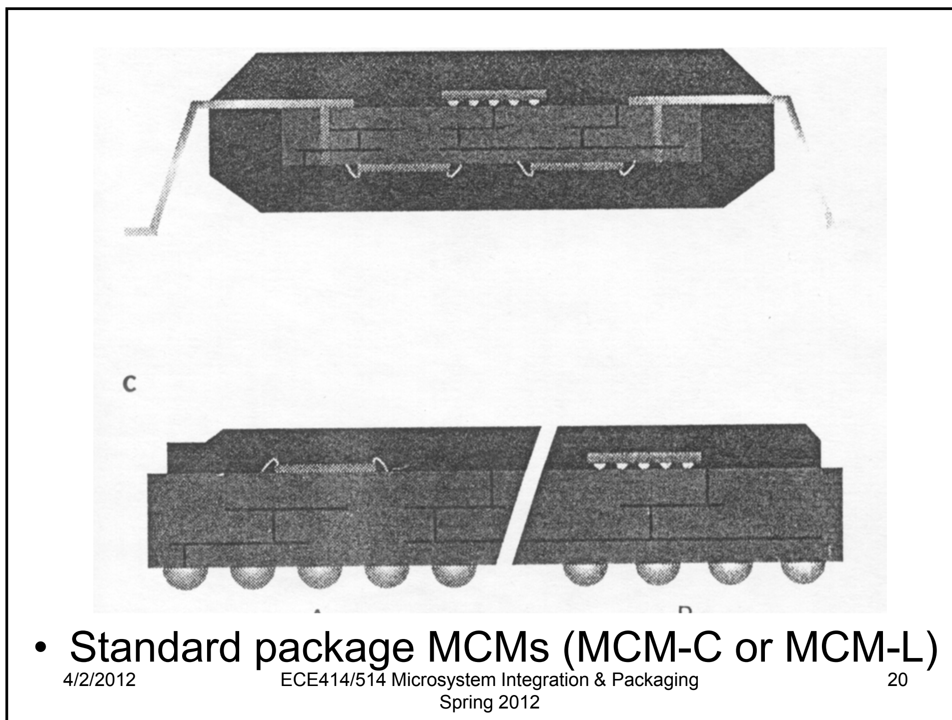


Figure 2.1. Microprocessor performance trends.[2]



- Standard package MCMs (MCM-C or MCM-L)

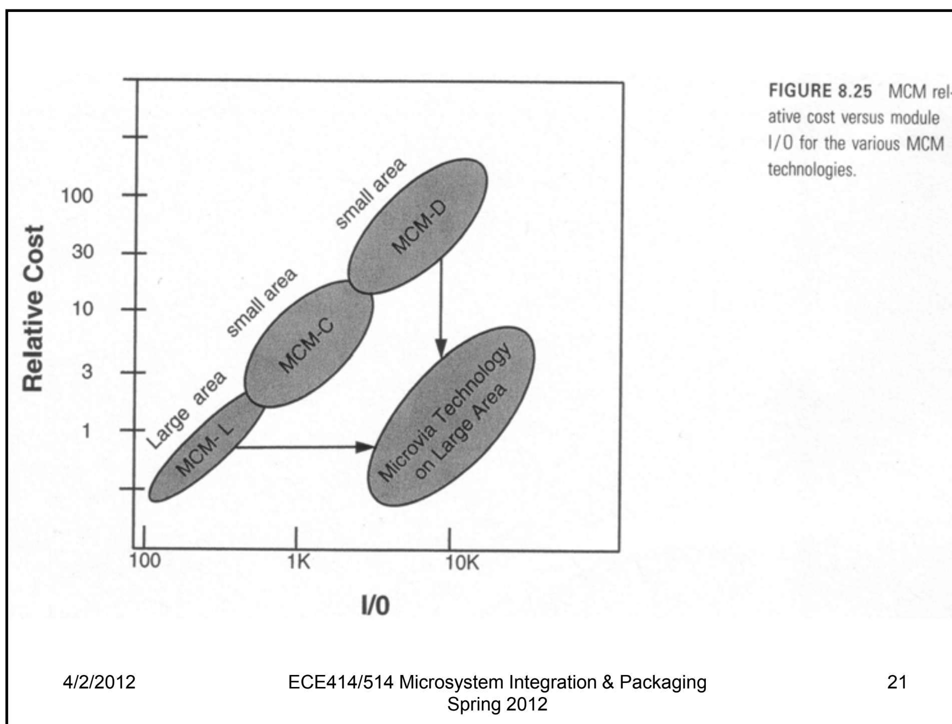


FIGURE 8.25 MCM relative cost versus module I/O for the various MCM technologies.

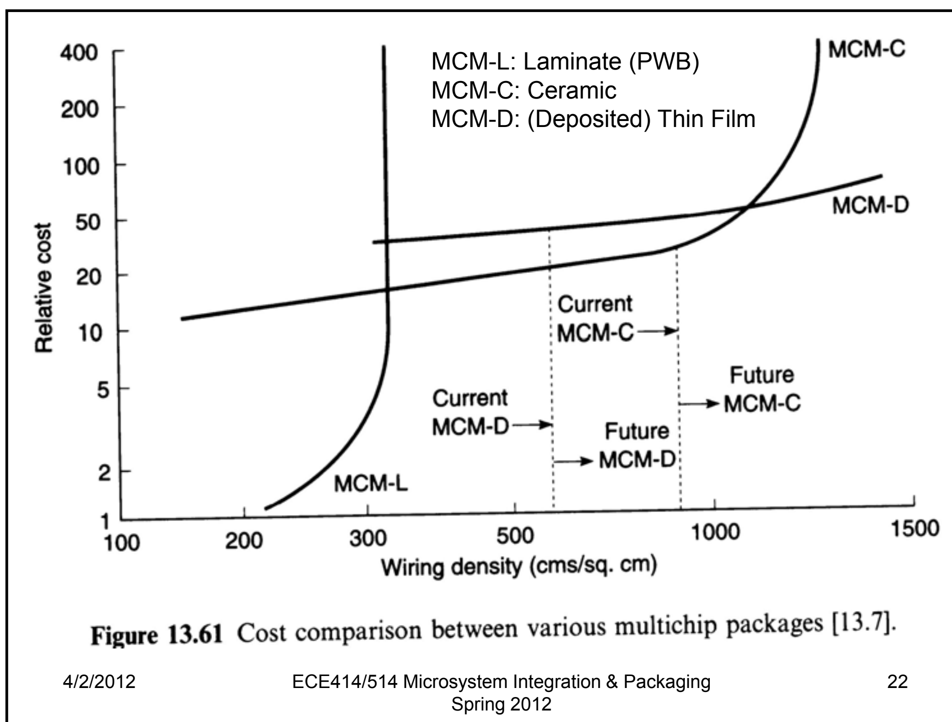


Figure 13.61 Cost comparison between various multichip packages [13.7].

Encapsulation: "Glob-top"

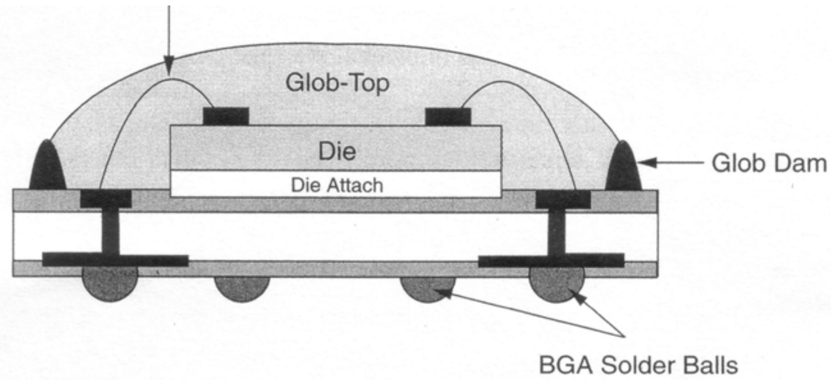
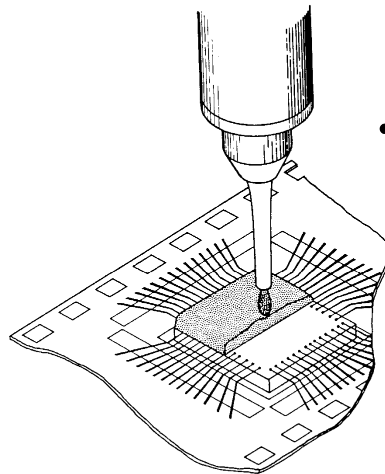


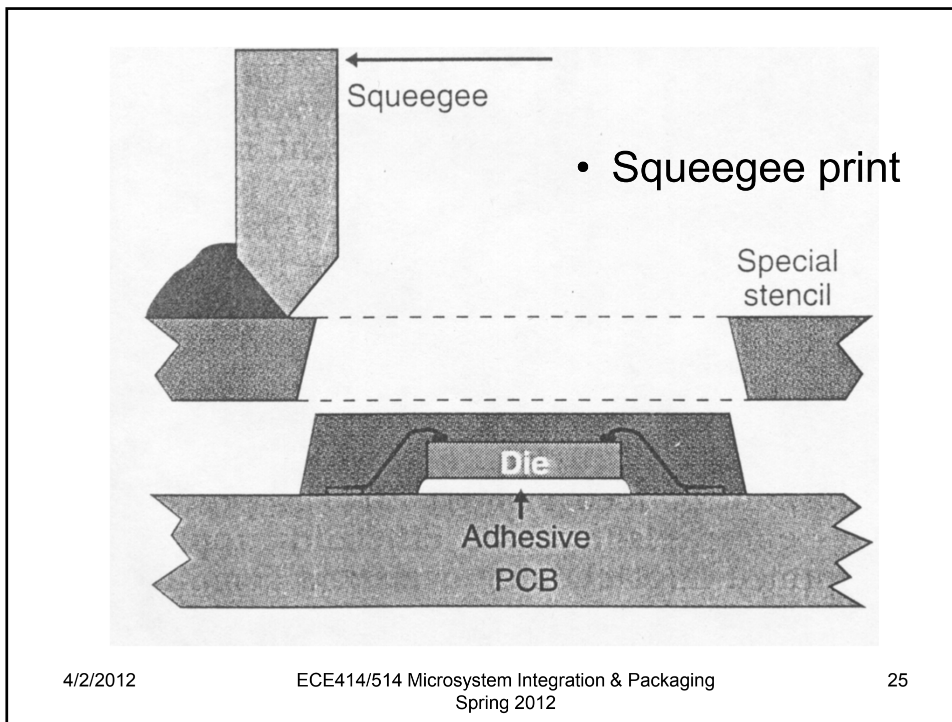
FIGURE 15.14 Glob-topping a ball grid array (BGA) device.

COB/DCA encapsulation



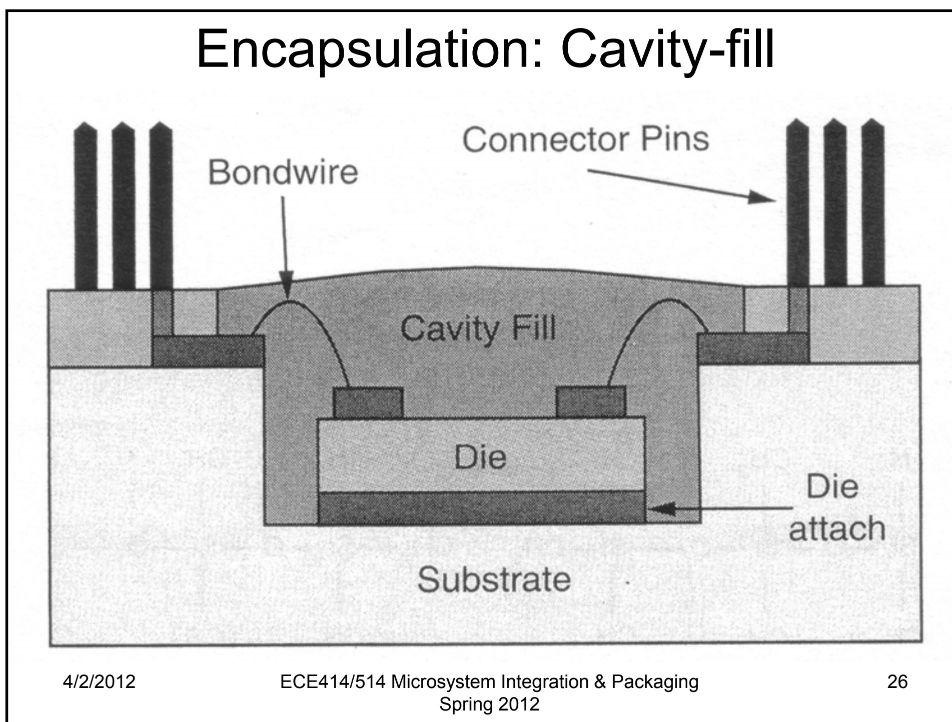
- Syringe dispense

Figure 6-40. TAB Encapsulation. A single-orifice nozzle dispenses encapsulant on the bonded chip.



- Squeegee print

Encapsulation: Cavity-fill



Encapsulation: Transfer molding

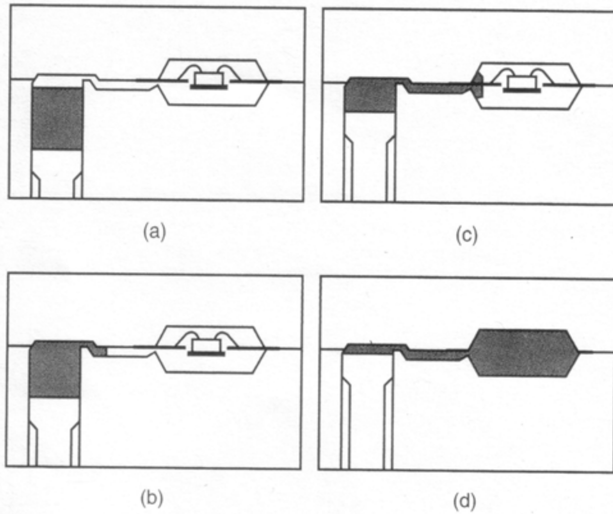
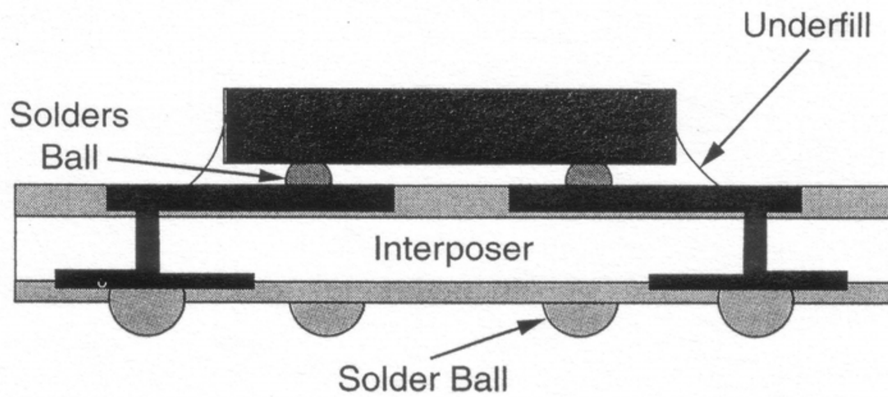


FIGURE 15.13 A typical transfer molding process.

Encapsulation: Underfill



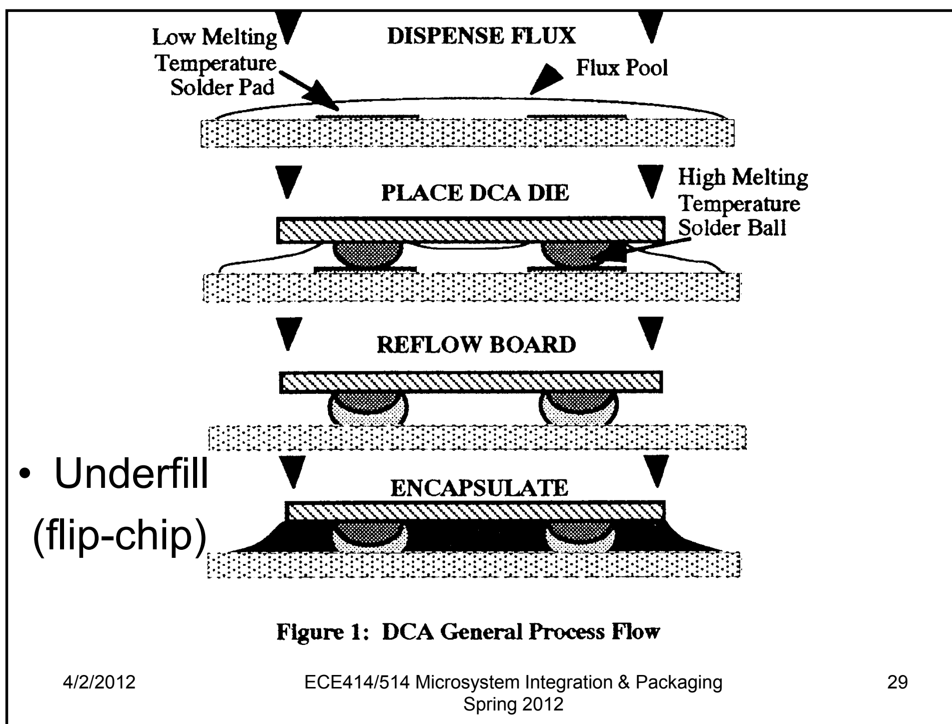


Figure 1: DCA General Process Flow

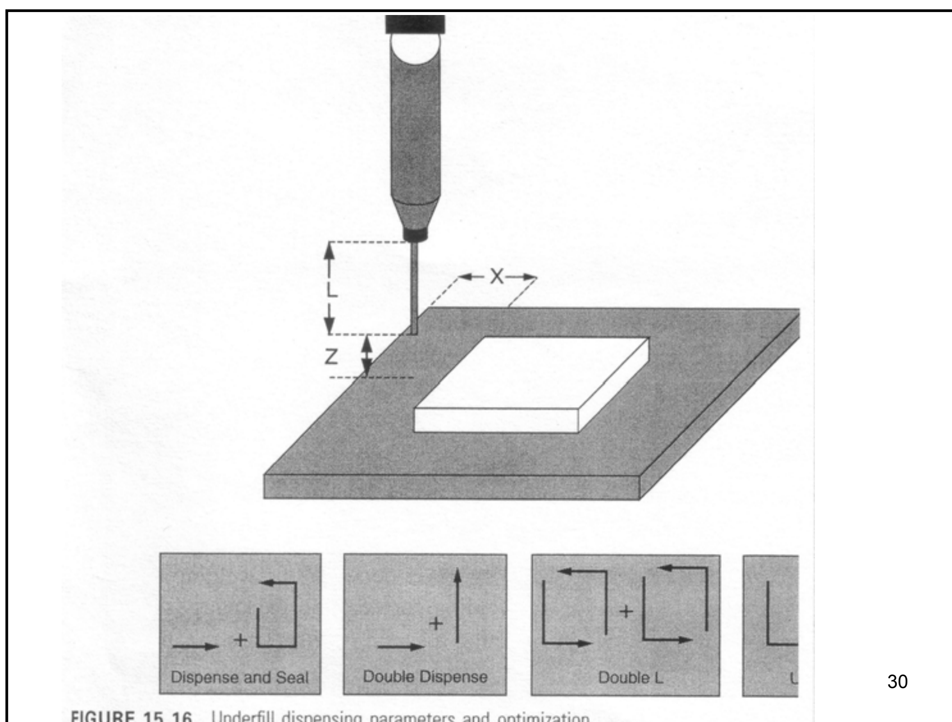


FIGURE 15.16 Underfill dispensing parameters and optimization.

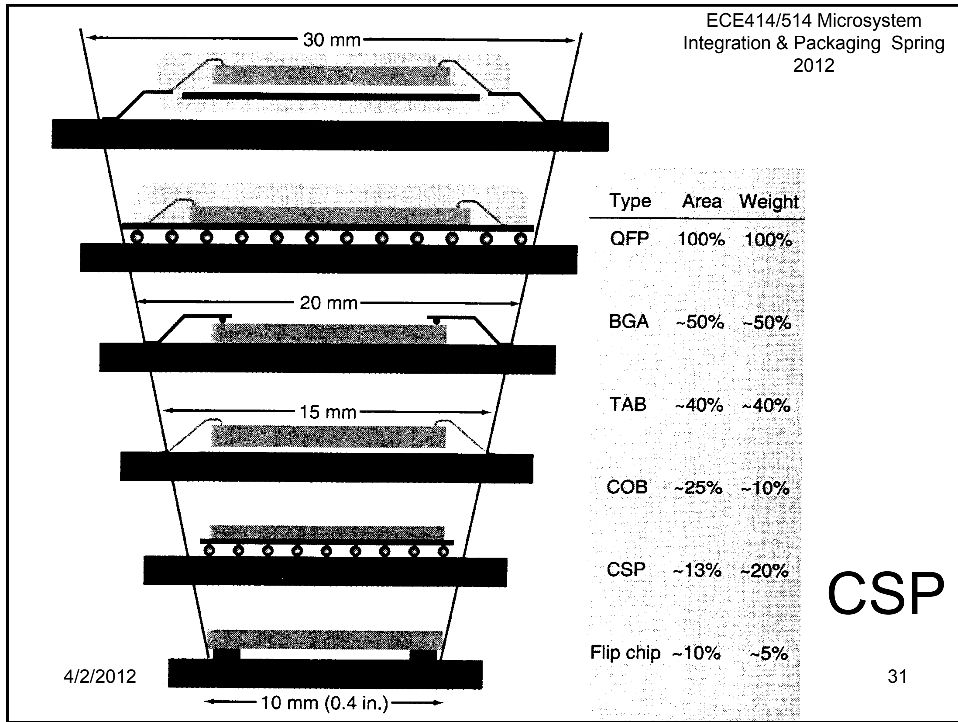


Table 1: CSP Package Classification

Category	Type	Example	Companies
Flex Circuit Interposer	TAB /flip chip		GE,Sony, Mitsubishi, NEC, Tessera and licensees
	Wire bonding		Fujitsu, Mitsubishi, Sharp, TI Japan, Toshiba
Rigid Substrate	Flip chip		Citizen Watch, Kyocera, Matsushita, Motorola, Nikko, Oki Electric, Toshiba, Sony
	Wire bonding		Amkor/Anam, Fujitsu, National Semiconductor, NEC, Sony
Custom Lead Frame	TAB /flip chip		Rohm
	Wire bonding		Amkor/Anam, Fujitsu, Hitachi Cable, LG Semicon, Toshiba
Wafer-Level Assembly	Redistribution		ChipScale, EPIC, IME (Sing.), NEC, Sandia Nat'l. Labs.
	Substrate		ChipScale and licensees, ShellCase, Tessera, [illegible]

Source: TechSearch International, Inc.

Micro BGA absorbs thermal expansion

Encapsulant
Ribbon leads
Flex-circuit interconnect
Die
Compliant layer
Substrate

In Tessera's Micro BGA (μBGA), a layer of compliant silicone elastomer absorbs the shear stress caused by thermal-expansion mismatch between the silicon die and the organic interconnect. The S-shaped ribbon leads, supported by the compliant silicone encapsulant, accommodate the bending forces.

0.298-0.370"
0.014-0.050"
0.270" (0.270 x 0.242)
0.014-0.050"
Silicon IC
Cu
97Pb/3Sn
40Pb/60Sn
0.016"
0.003-0.005"
0.003-0.005"
0.0008-0.001"
0.008-0.012"
FR-4 or BT epoxy
0.020"
Cu-Ni
Au
36Pb/62Sn/2Ag
0.012"
0.0222"
0.032"
FR4 Board
0.030-0.060"

Figure 1: Schematic of a SLICC package.

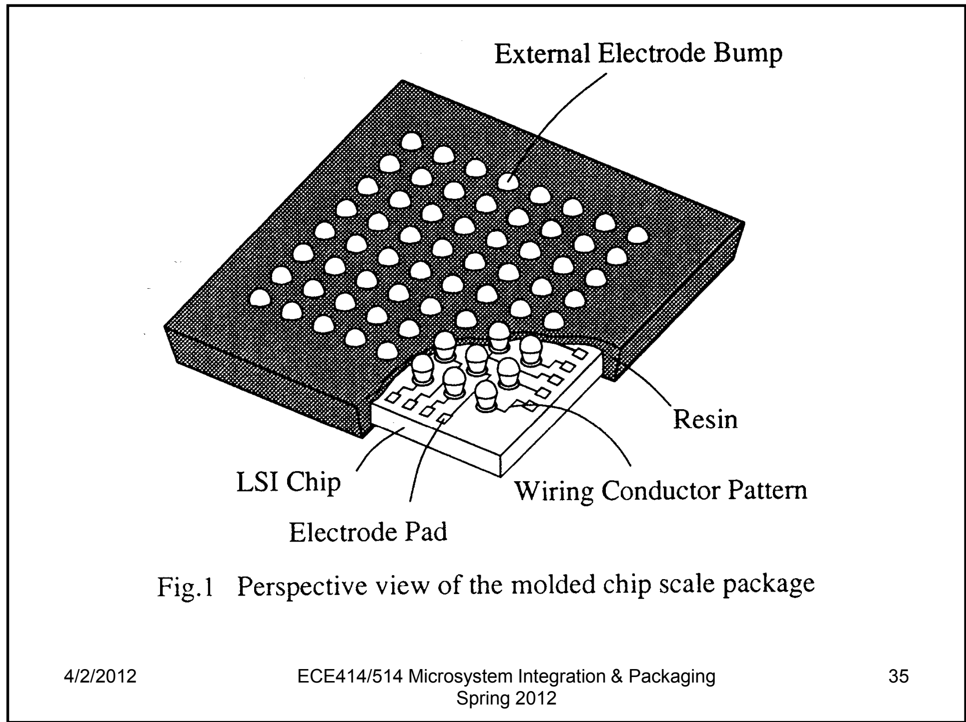
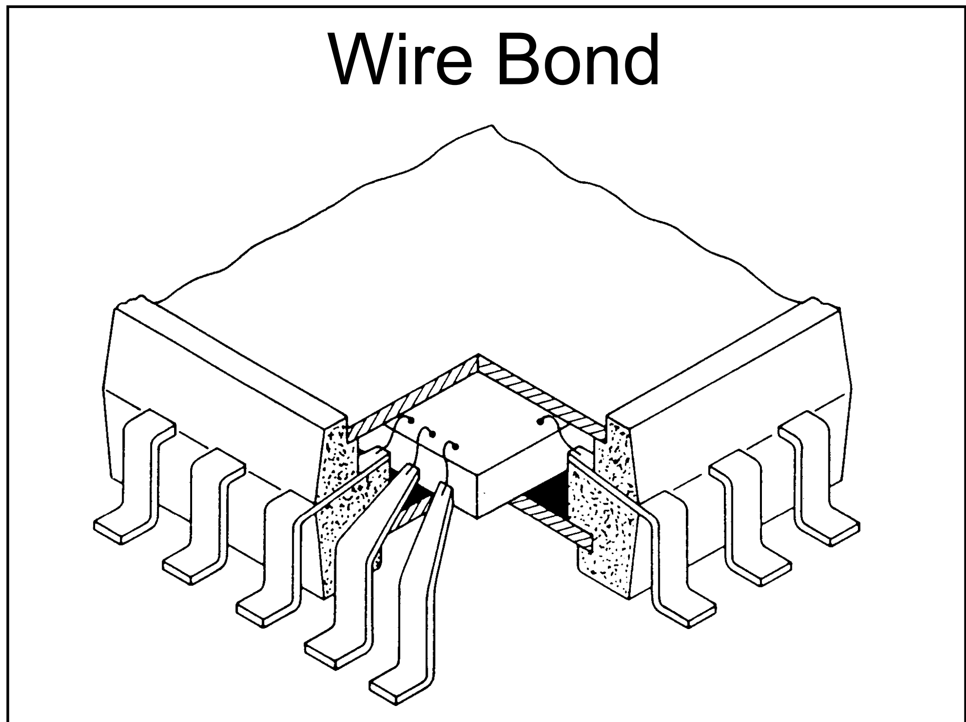


Fig.1 Perspective view of the molded chip scale package

Wire Bond



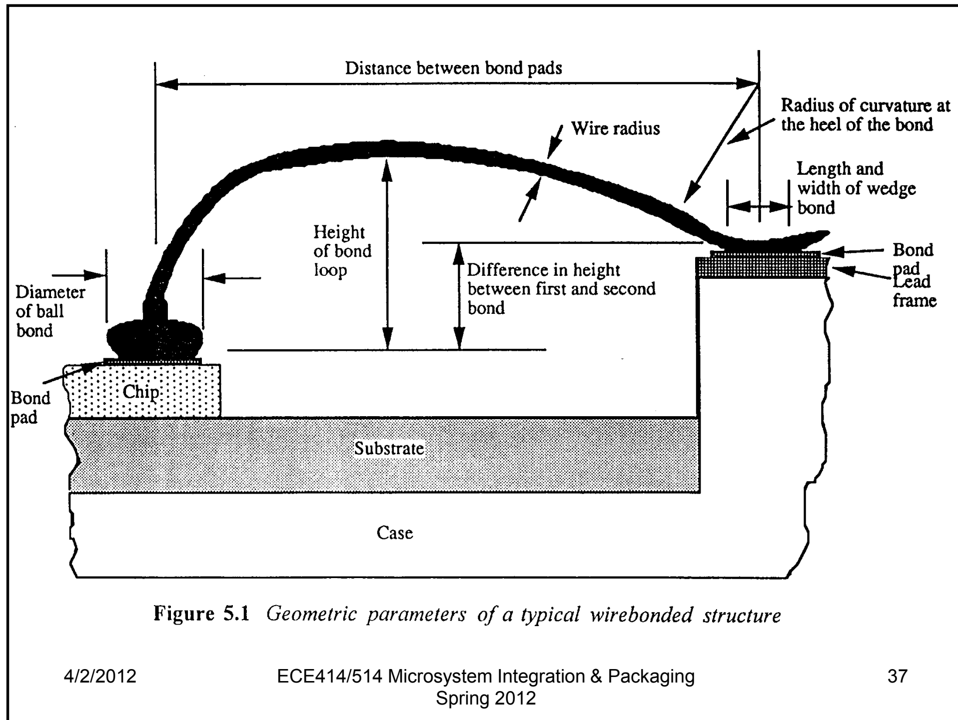


Figure 5.1 *Geometric parameters of a typical wirebonded structure*

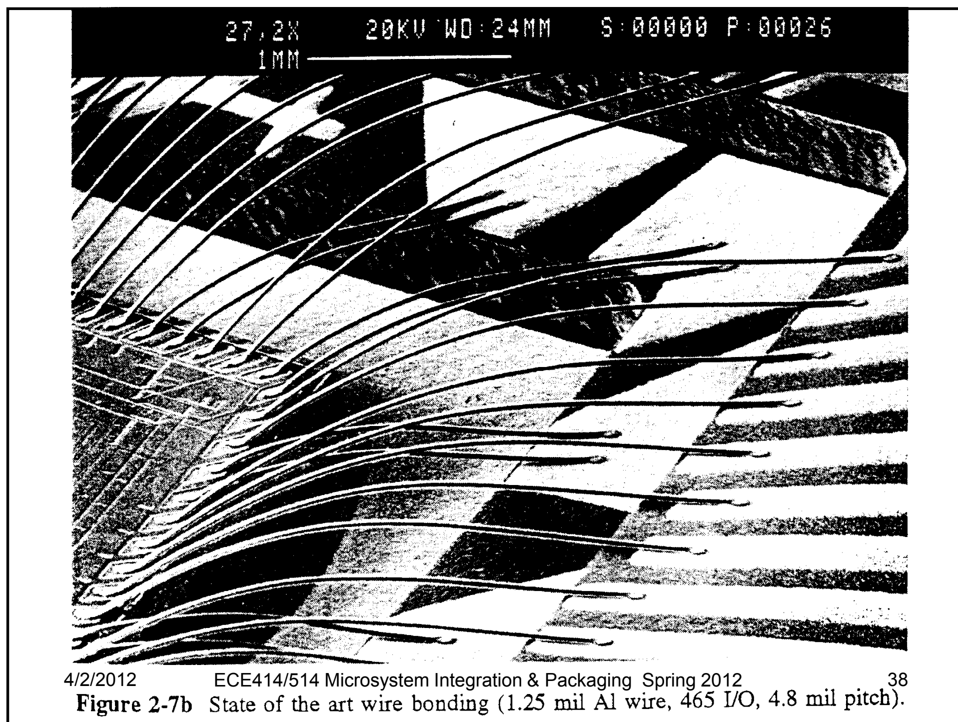
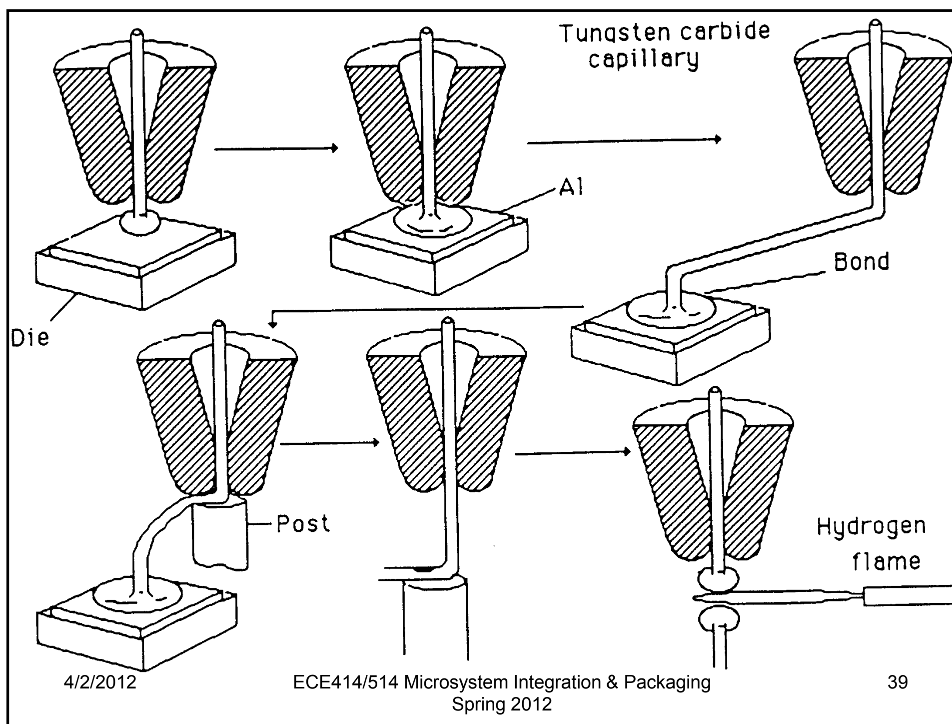
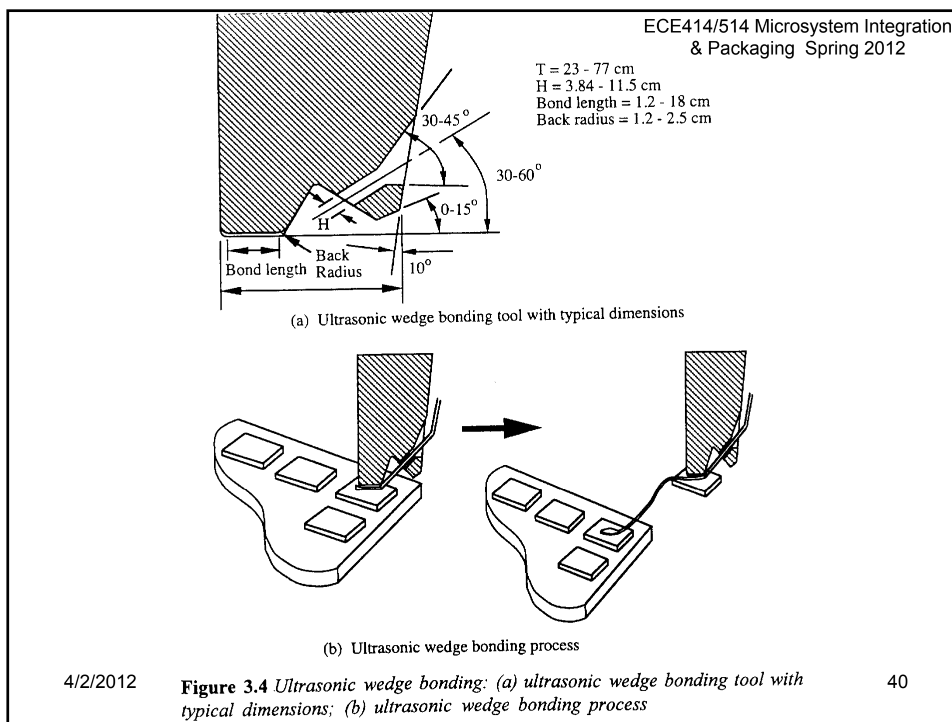


Figure 2-7b State of the art wire bonding (1.25 mil Al wire, 465 I/O, 4.8 mil pitch).

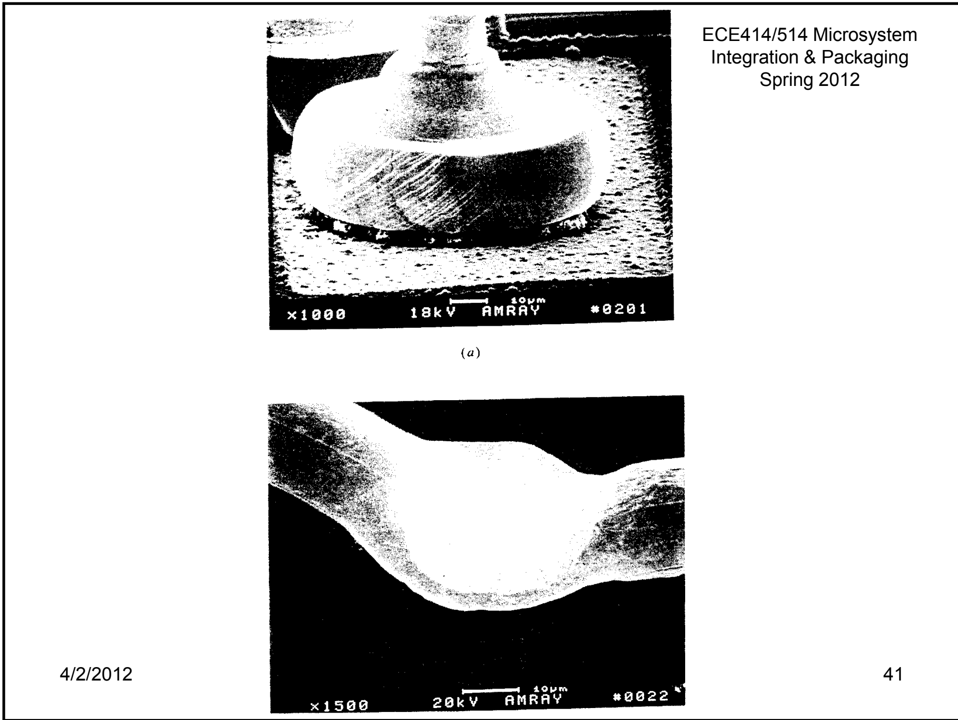




(a) Ultrasonic wedge bonding tool with typical dimensions

(b) Ultrasonic wedge bonding process

Figure 3.4 *Ultrasonic wedge bonding: (a) ultrasonic wedge bonding tool with typical dimensions; (b) ultrasonic wedge bonding process*



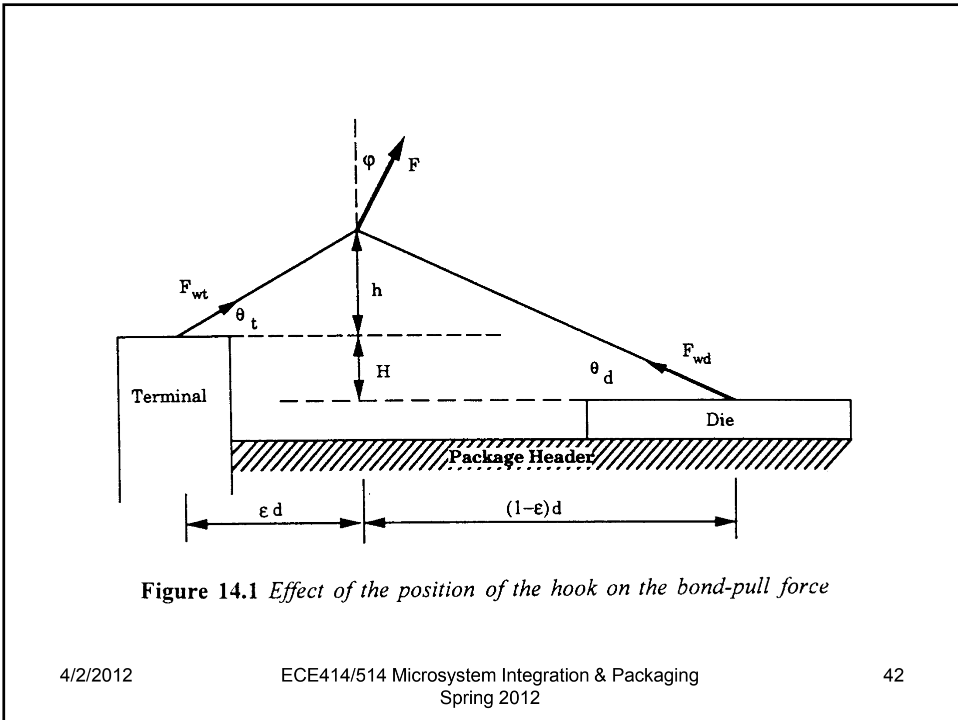


Figure 14.1 *Effect of the position of the hook on the bond-pull force*

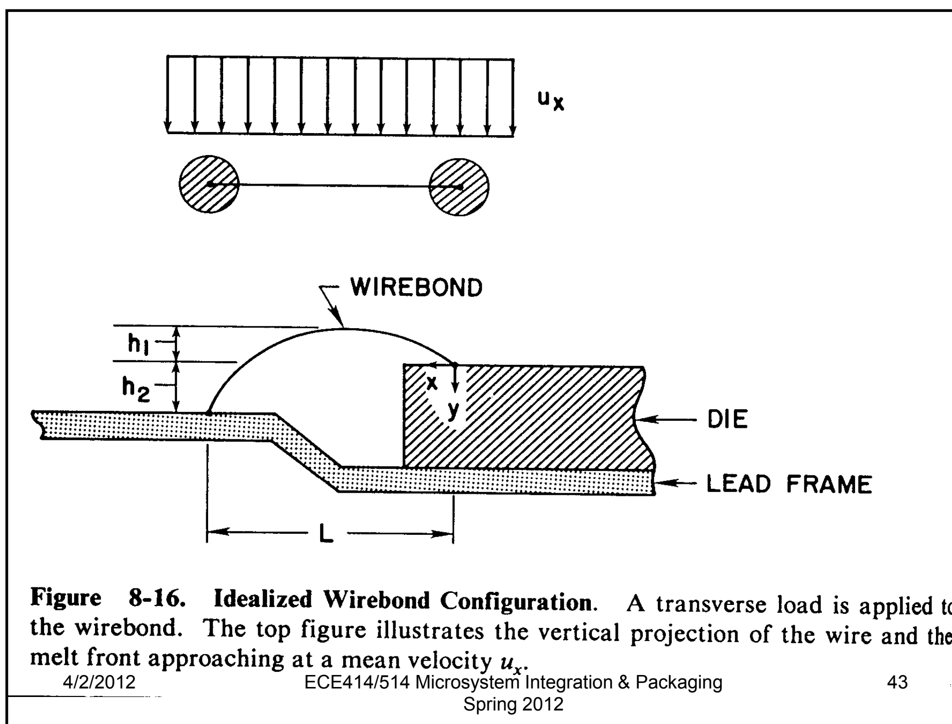


Figure 8-16. Idealized Wirebond Configuration. A transverse load is applied to the wirebond. The top figure illustrates the vertical projection of the wire and the melt front approaching at a mean velocity u_x.

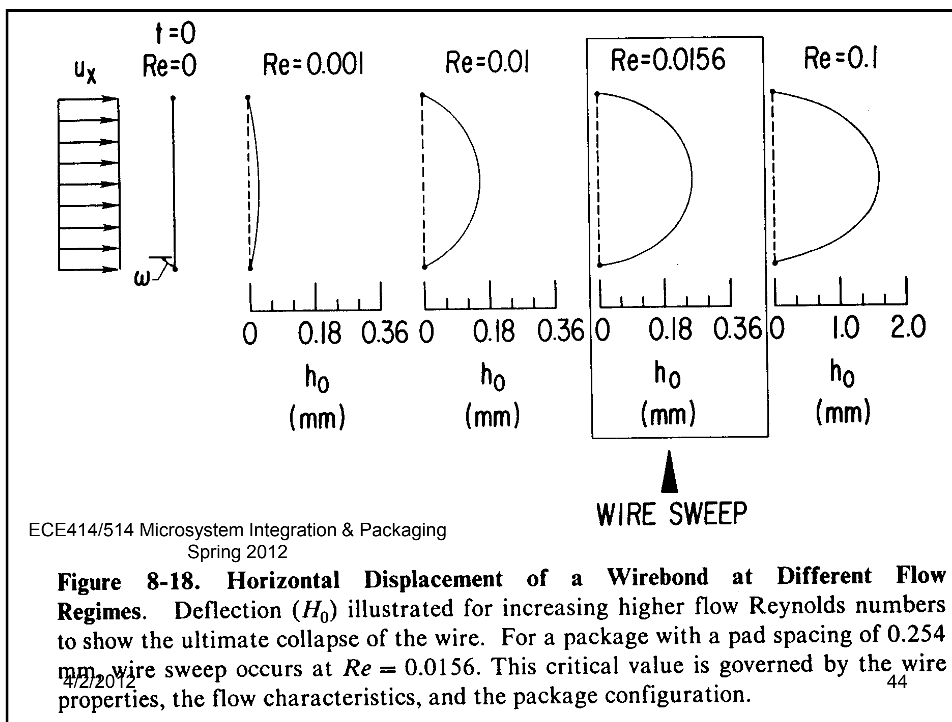


Figure 8-18. Horizontal Displacement of a Wirebond at Different Flow Regimes. Deflection (H_0) illustrated for increasing higher flow Reynolds numbers to show the ultimate collapse of the wire. For a package with a pad spacing of 0.254 mm, wire sweep occurs at $Re = 0.0156$. This critical value is governed by the wire properties, the flow characteristics, and the package configuration.

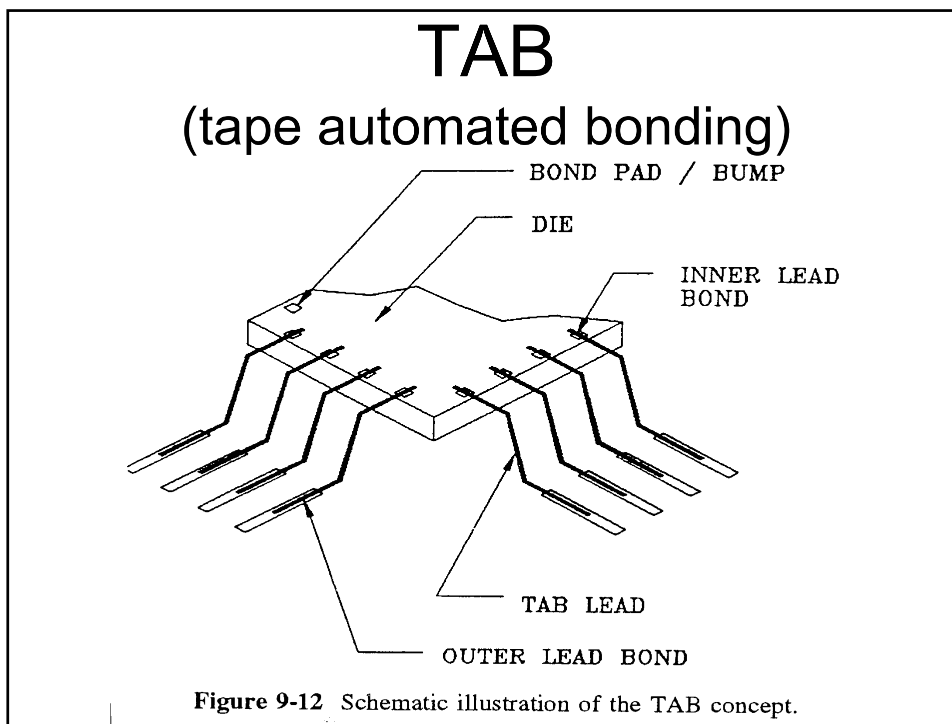


Figure 9-12 Schematic illustration of the TAB concept.

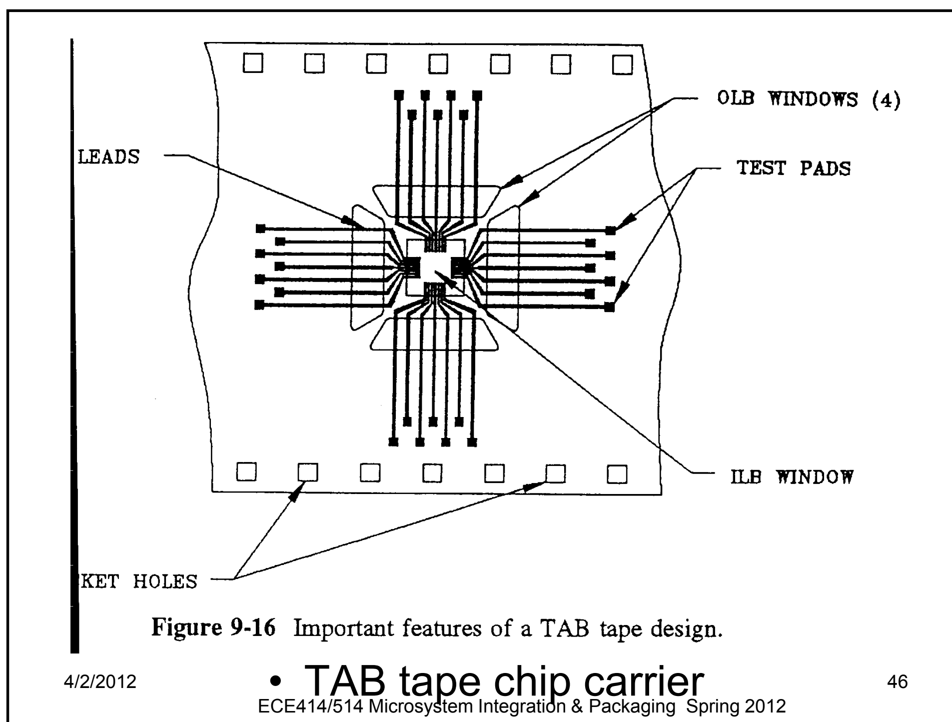


Figure 9-16 Important features of a TAB tape design.

Figure 4-19 Details of chip in position for ILB.

- Inner lead bonding (to chip)

- Inner lead bonding

Figure 4-18 Inner lead bonding process. (a) Film tape with sprocket holes. (b) Overall process and enlarged view of tape leads and bonds. (c) Inner lead bonding with thermode down, support carrier up. (d) Chip attached to tape with thermode up, support carrier down. (e) Indexing to next chip-bonding position.

(*Source: Electronic Materials Handbook, Vol. 1: Packaging*, p. 232.)

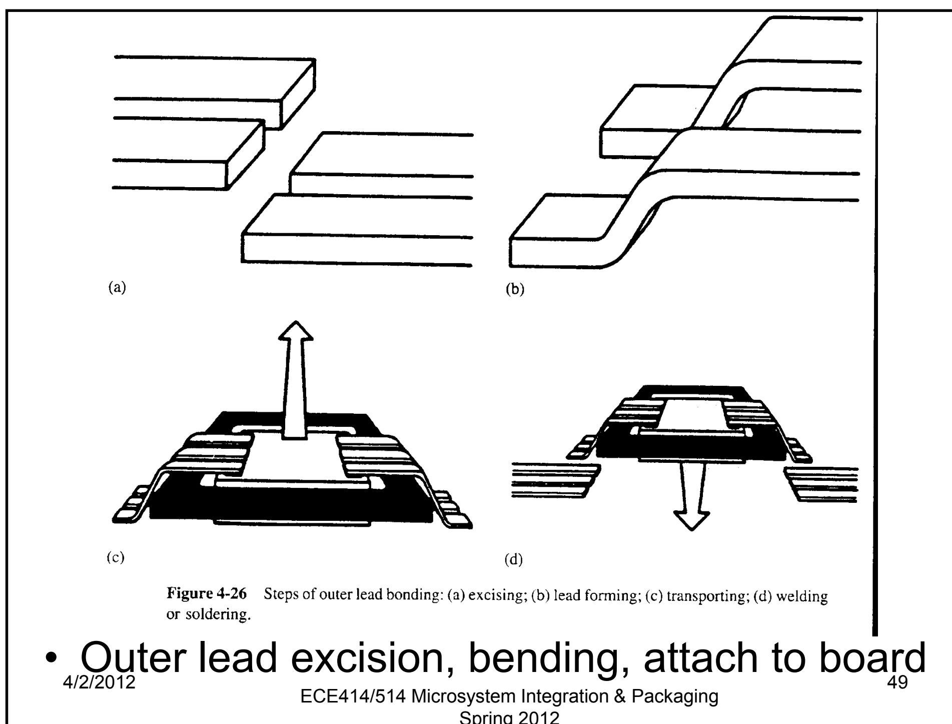


Figure 4-26 Steps of outer lead bonding: (a) excising; (b) lead forming; (c) transporting; (d) welding or soldering.

- Outer lead excision, bending, attach to board

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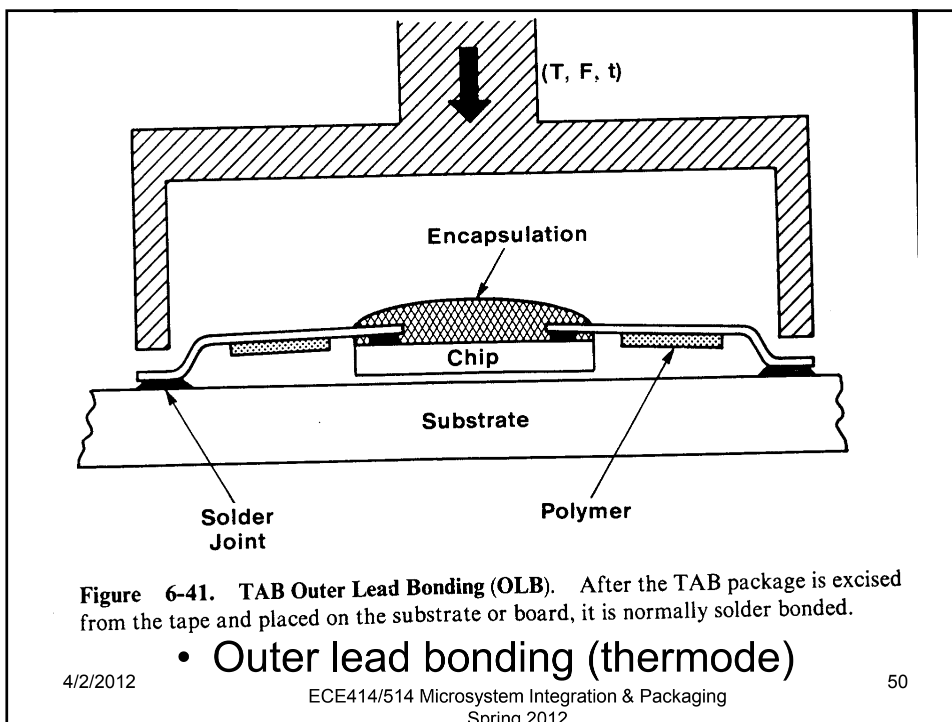

Figure 6-41. TAB Outer Lead Bonding (OLB). After the TAB package is excised from the tape and placed on the substrate or board, it is normally solder bonded.

- Outer lead bonding (thermode)

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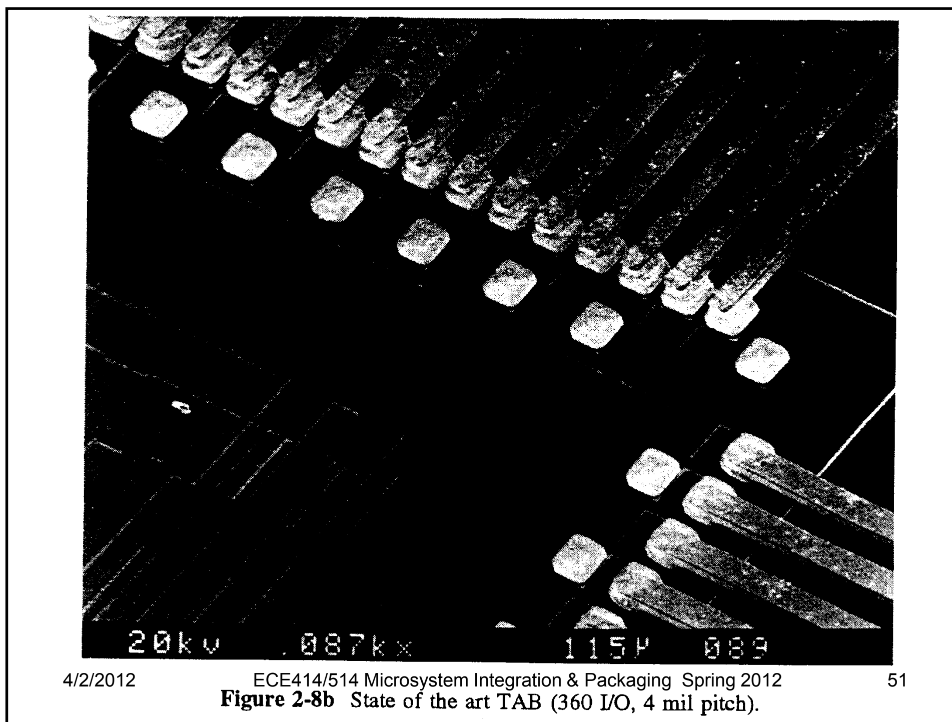


Figure 2-8b State of the art TAB (360 I/O, 4 mil pitch).

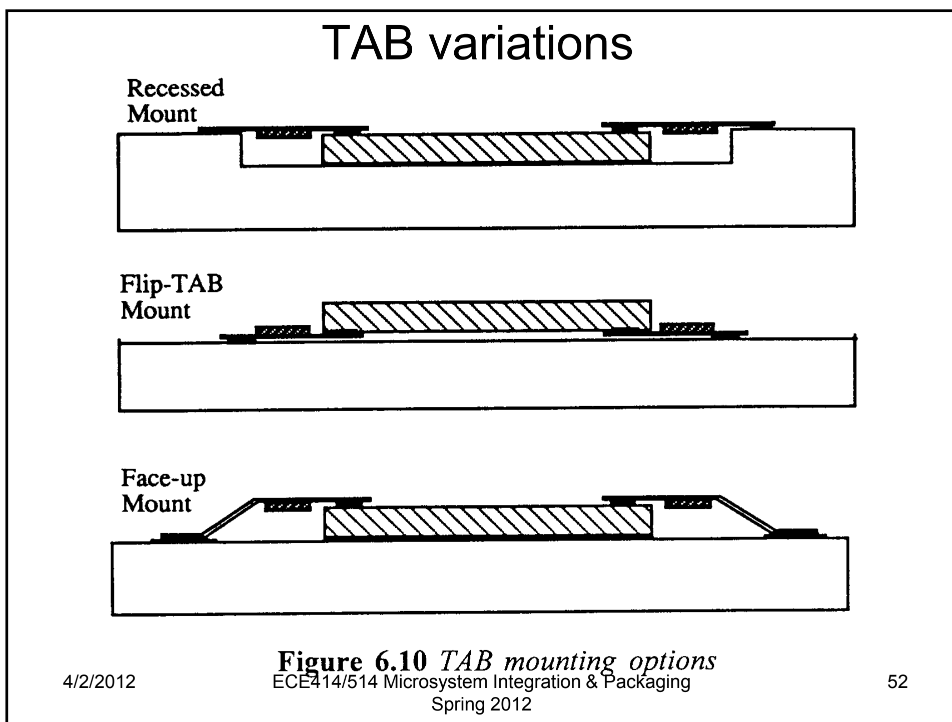


Figure 6.10 *TAB mounting options*

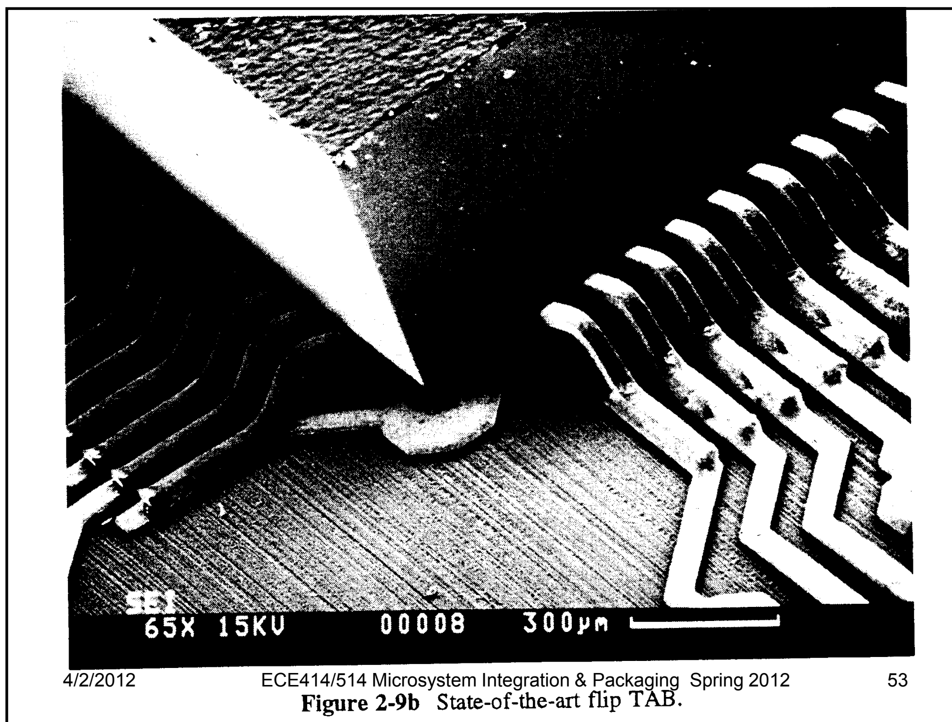


Figure 2-9b State-of-the-art flip TAB.

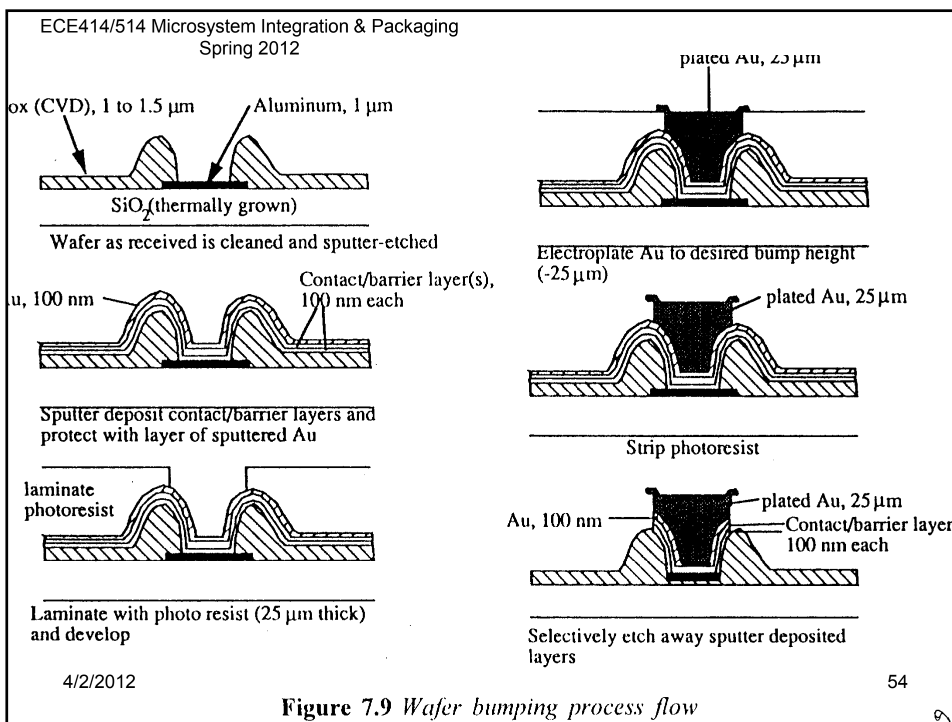


Figure 7.9 *Wafer bumping process flow*

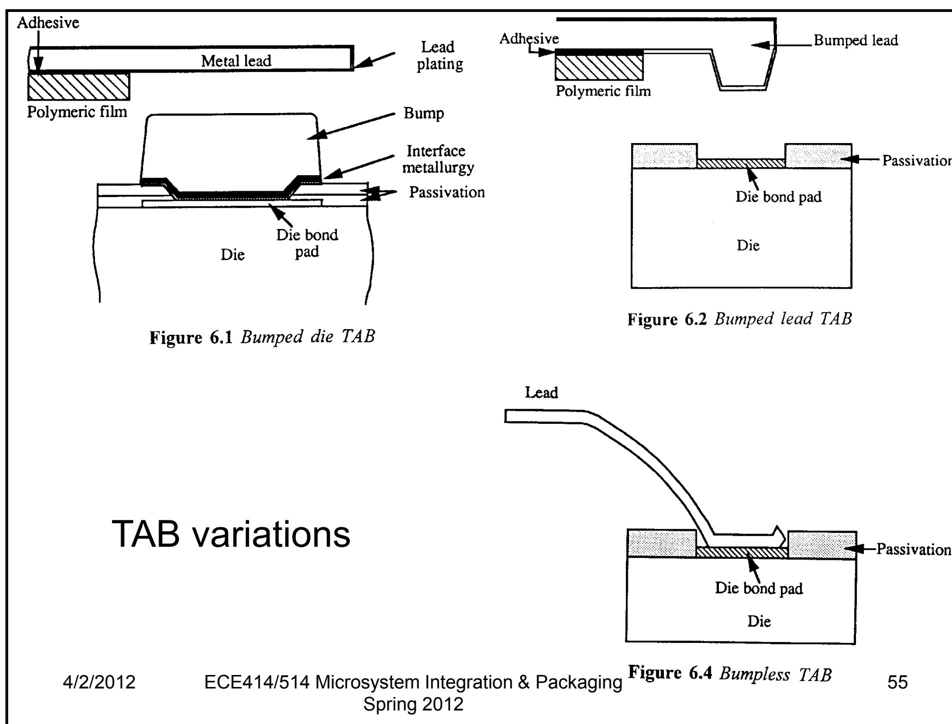


Figure 6.1 *Bumped die TAB*
Figure 6.2 *Bumped lead TAB*
Figure 6.4 *Bumpless TAB*

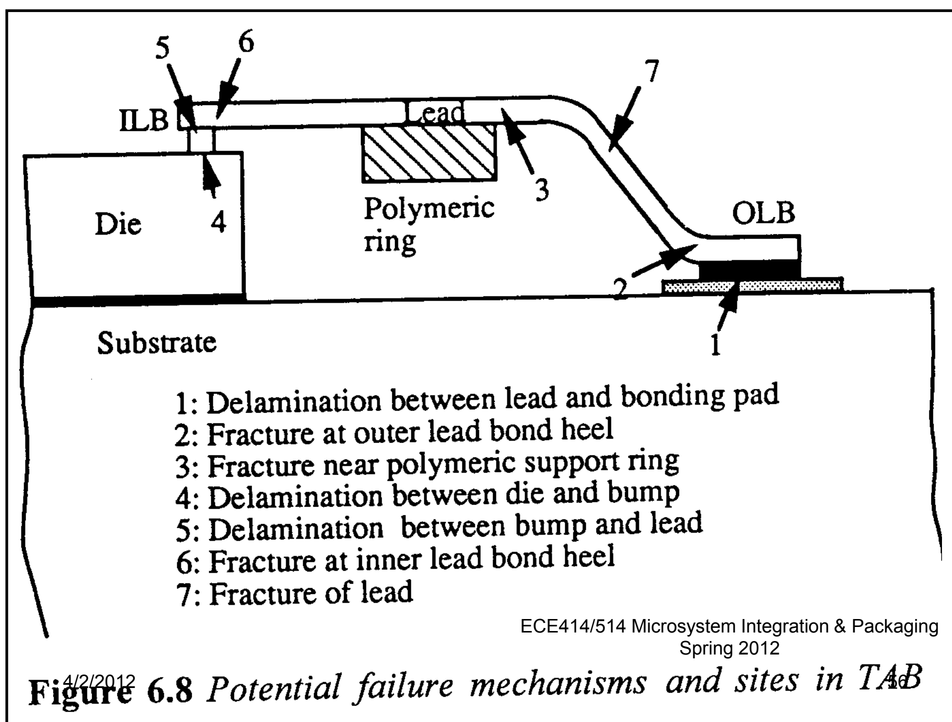


Figure 6.8 *Potential failure mechanisms and sites in TAB*

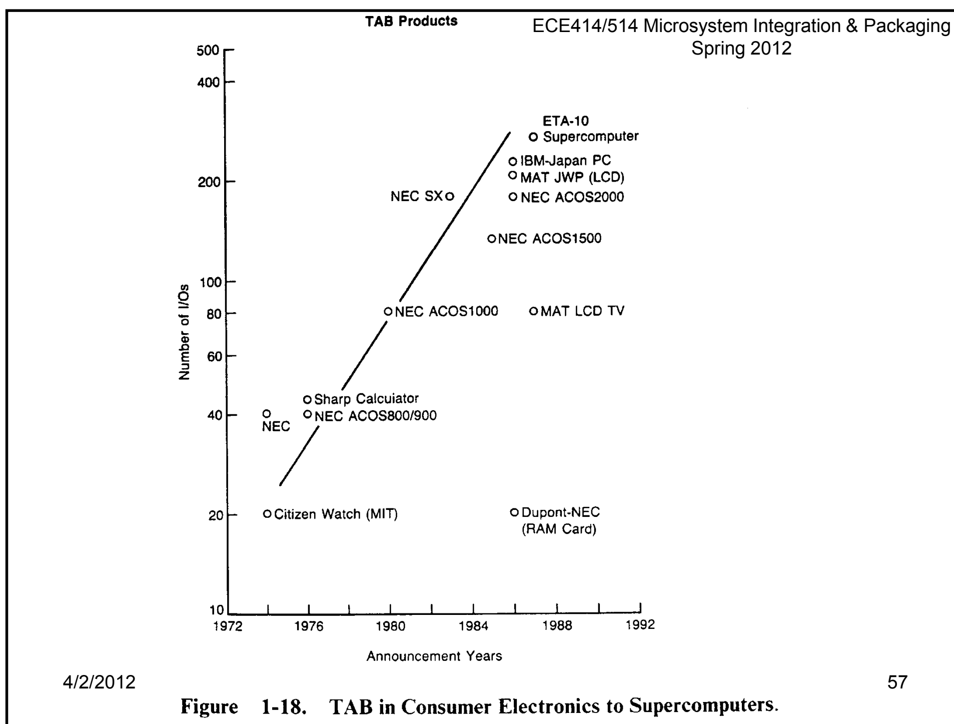


Figure 1-18. TAB in Consumer Electronics to Supercomputers.

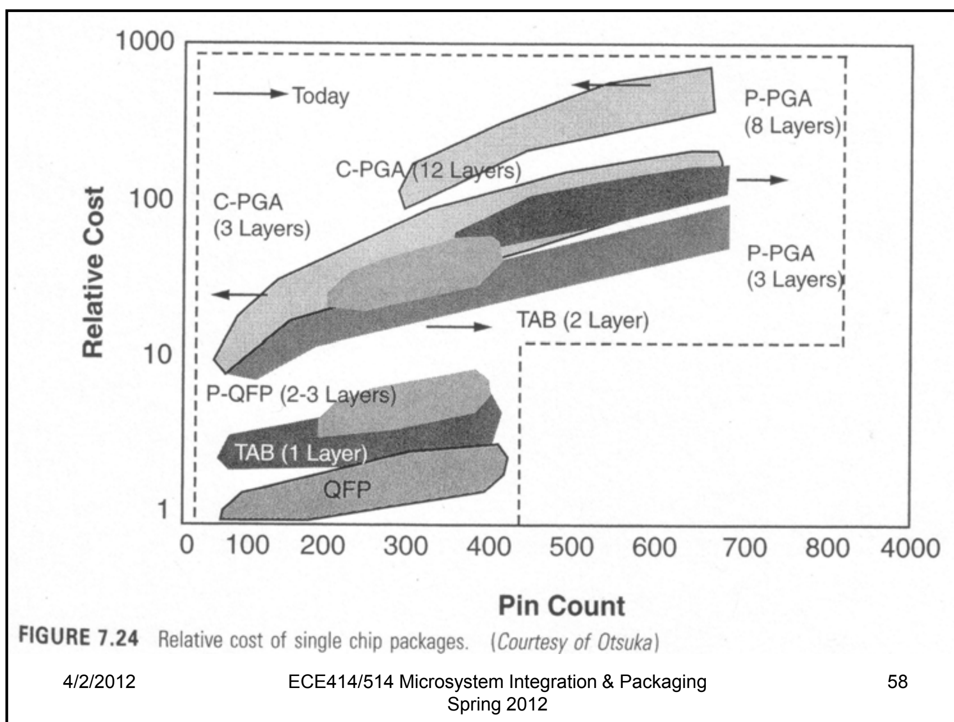


FIGURE 7.24 Relative cost of single chip packages. (*Courtesy of Otsuka*)

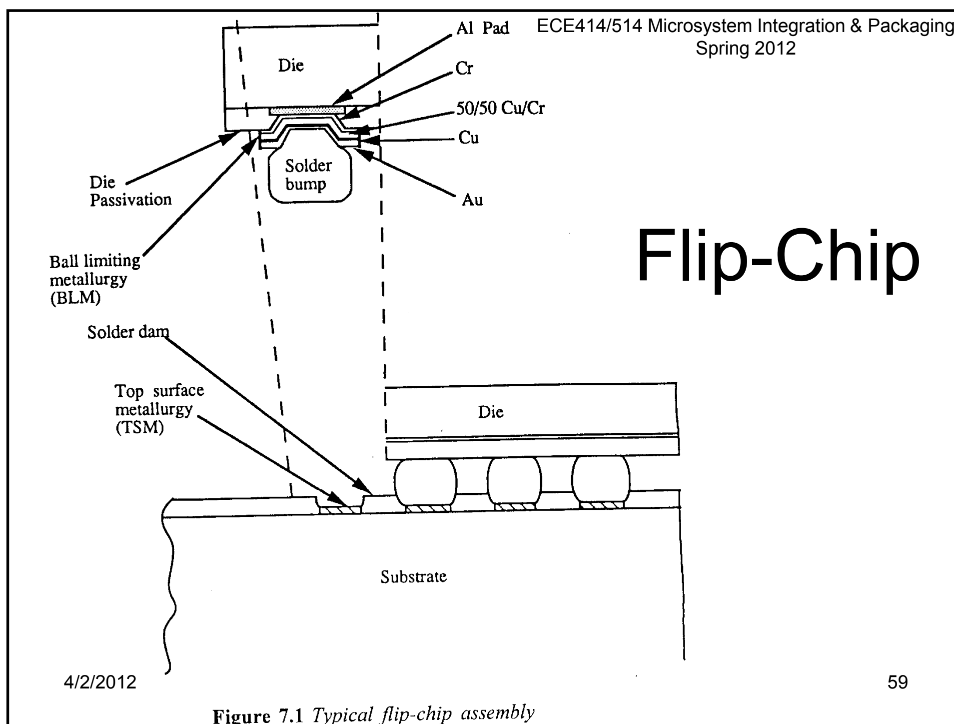
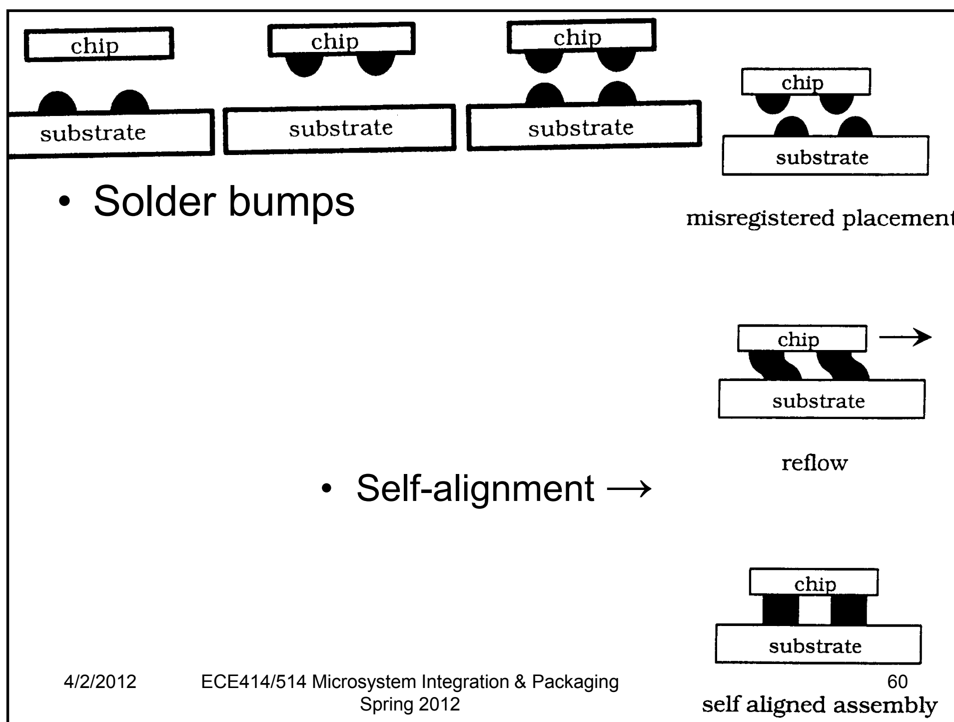


Figure 7.1 *Typical flip-chip assembly*



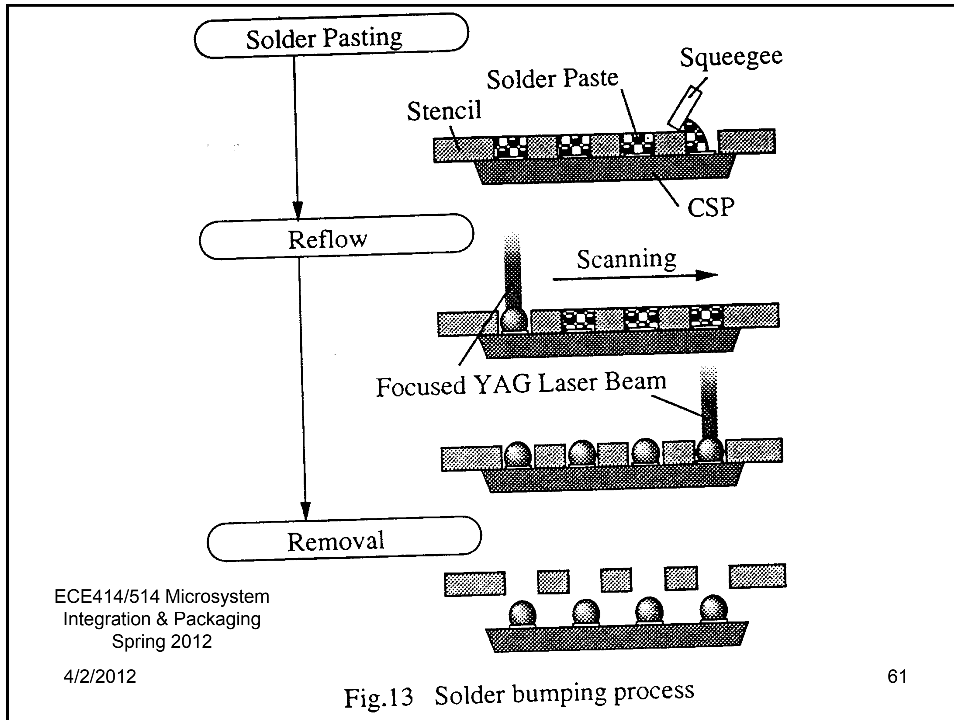
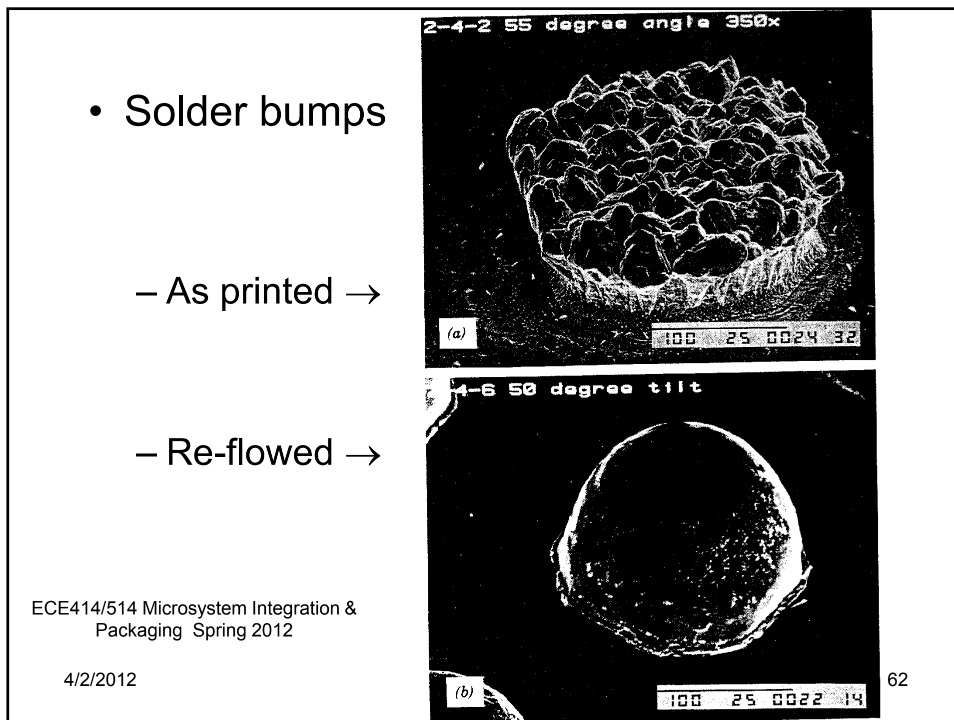


Fig.13 Solder bumping process



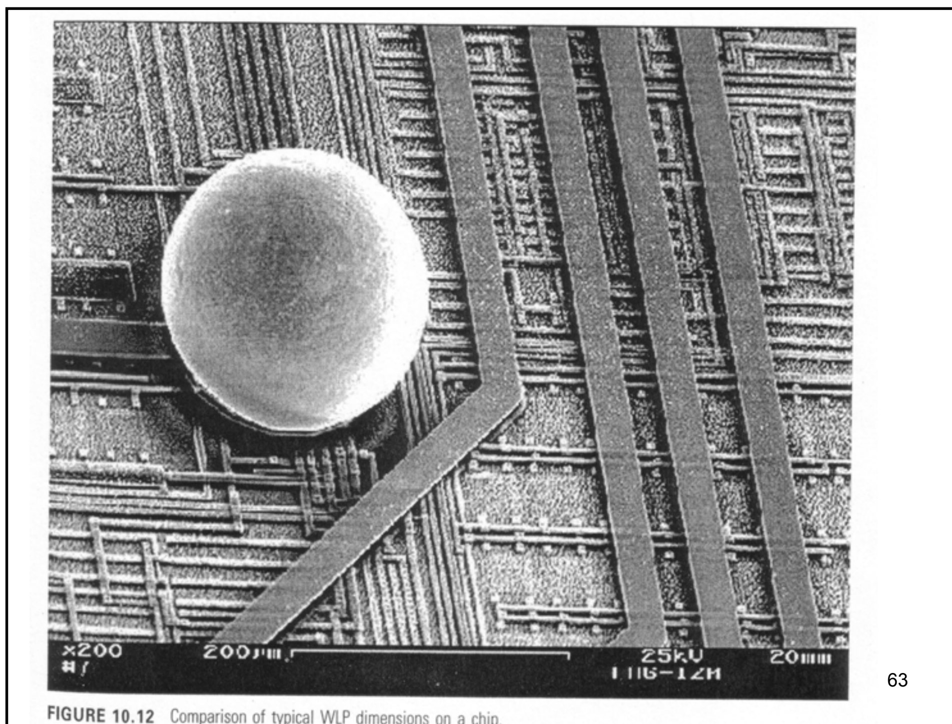


FIGURE 10.12 Comparison of typical WLP dimensions on a chip

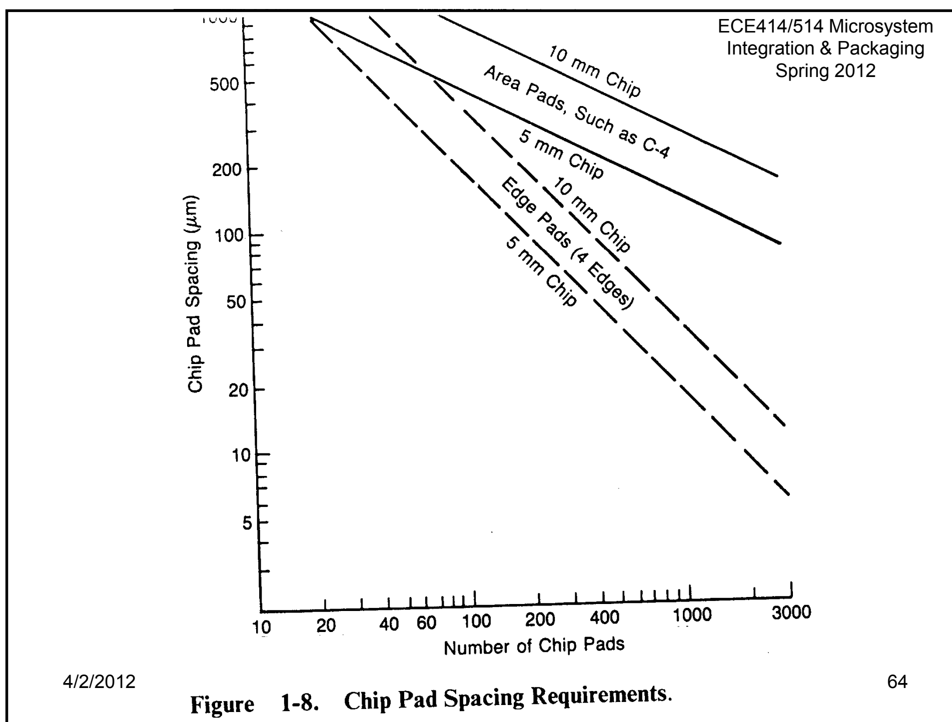


Figure 1-8. Chip Pad Spacing Requirements.

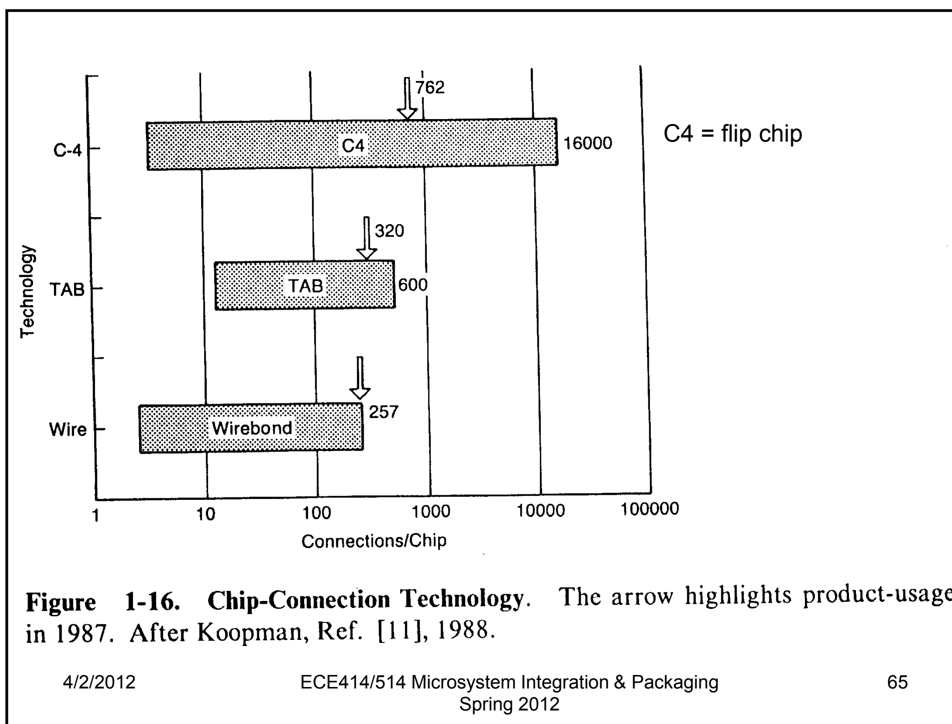


Figure 1-16. Chip-Connection Technology. The arrow highlights product-usage in 1987. After Koopman, Ref. [11], 1988.

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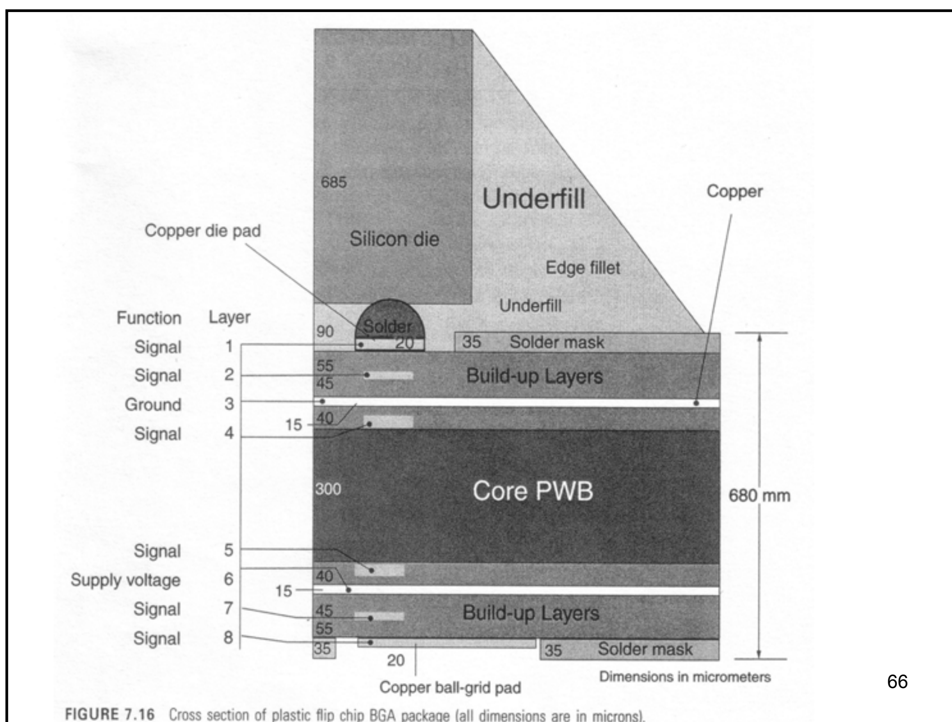

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FIGURE 7.16 Cross section of plastic flip chip BGA package (all dimensions are in microns).

New developments

WLP & Redistribution

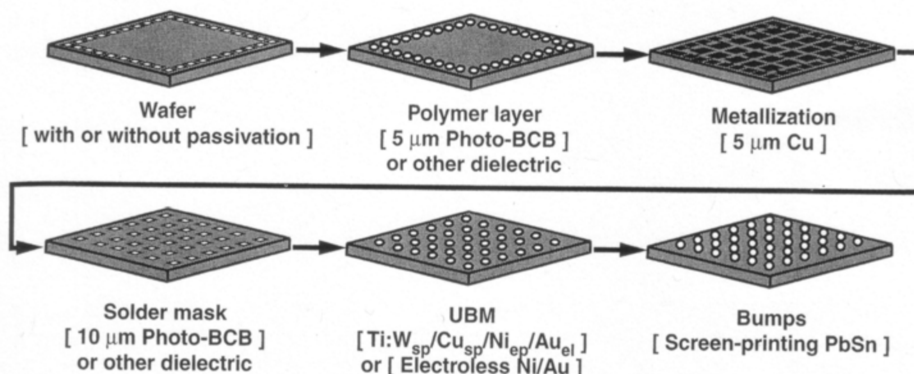


FIGURE 10.11 Typical redistribution technology. (*Courtesy of IZM Berlin*)

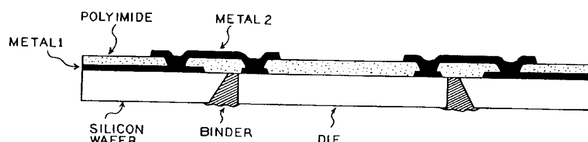


FIGURE 3.24 Silicon-in-silicon hybrid. The dice are stuffed through chemically etched holes in the wafer and glued down by polyimide or epoxy binding. A final level of metal interconnects the chips and the global lines on the wafer.

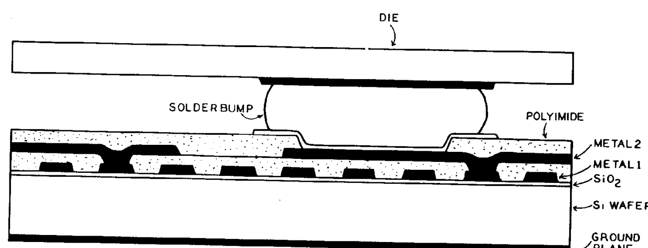


FIGURE 3.23 Silicon-on-silicon hybrid. Two levels of aluminum or copper interconnections are fabricated on a silicon wafer. Polyimide is used as the inter-metal insulator. Later separately fabricated chips are flip-mounted on the wafer using solder balls.

Figure 8

Dendrites can be customized to different applications, the

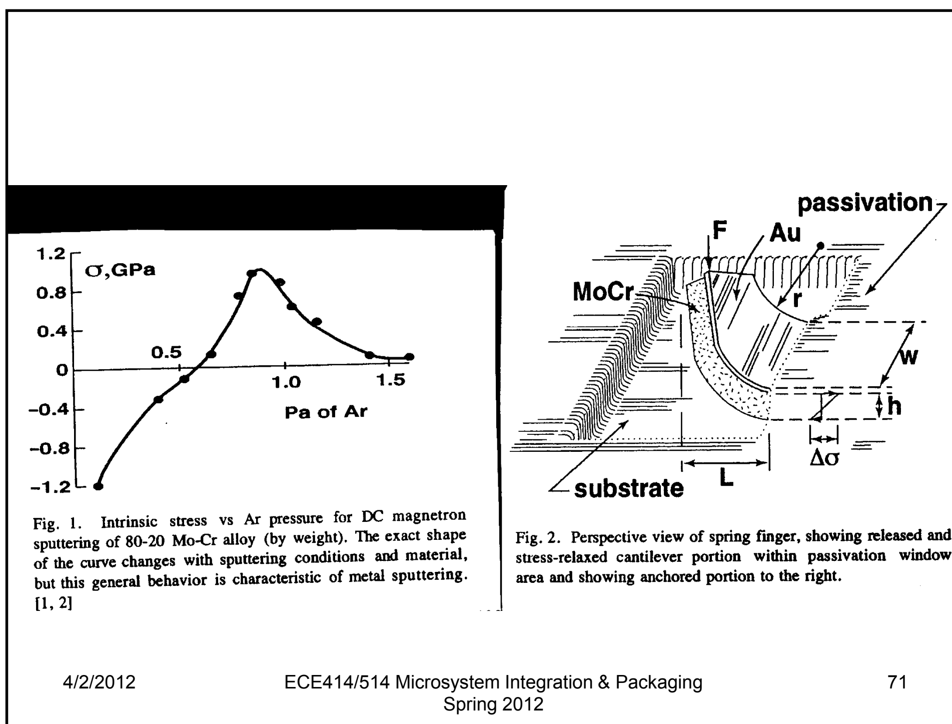


Fig. 1. Intrinsic stress vs Ar pressure for DC magnetron sputtering of 80-20 Mo-Cr alloy (by weight). The exact shape of the curve changes with sputtering conditions and material, but this general behavior is characteristic of metal sputtering. [1, 2]

Fig. 2. Perspective view of spring finger, showing released and stress-relaxed cantilever portion within passivation window area and showing anchored portion to the right.

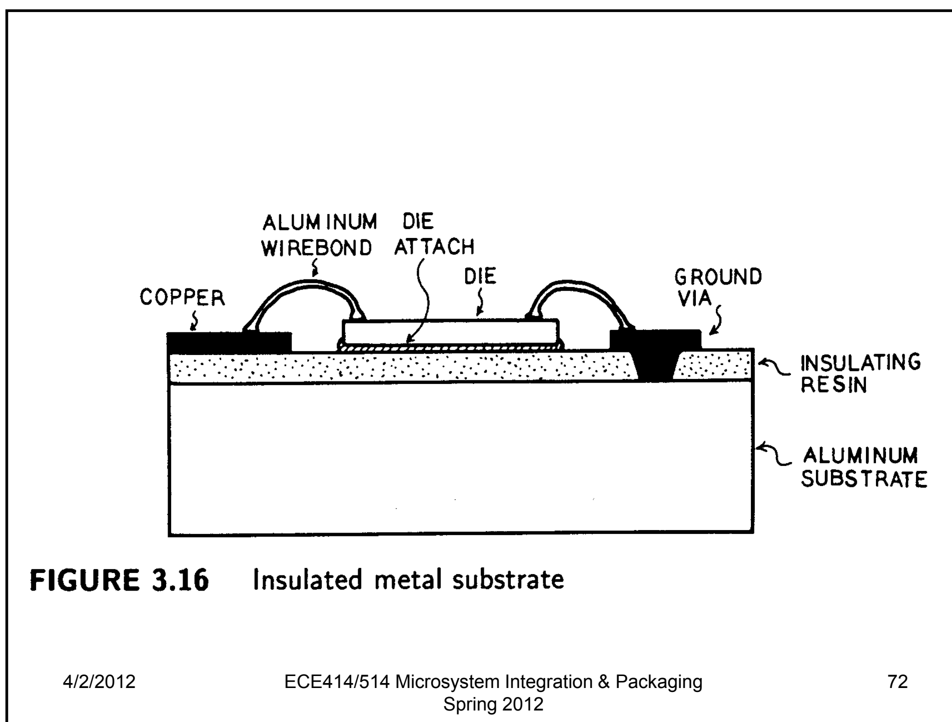


FIGURE 3.16 Insulated metal substrate

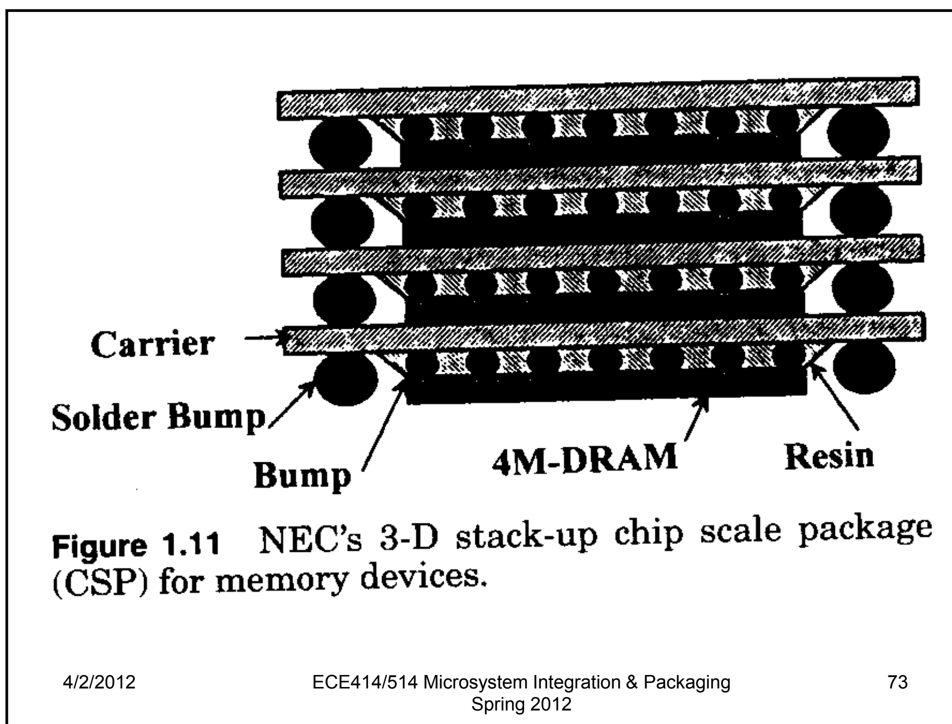
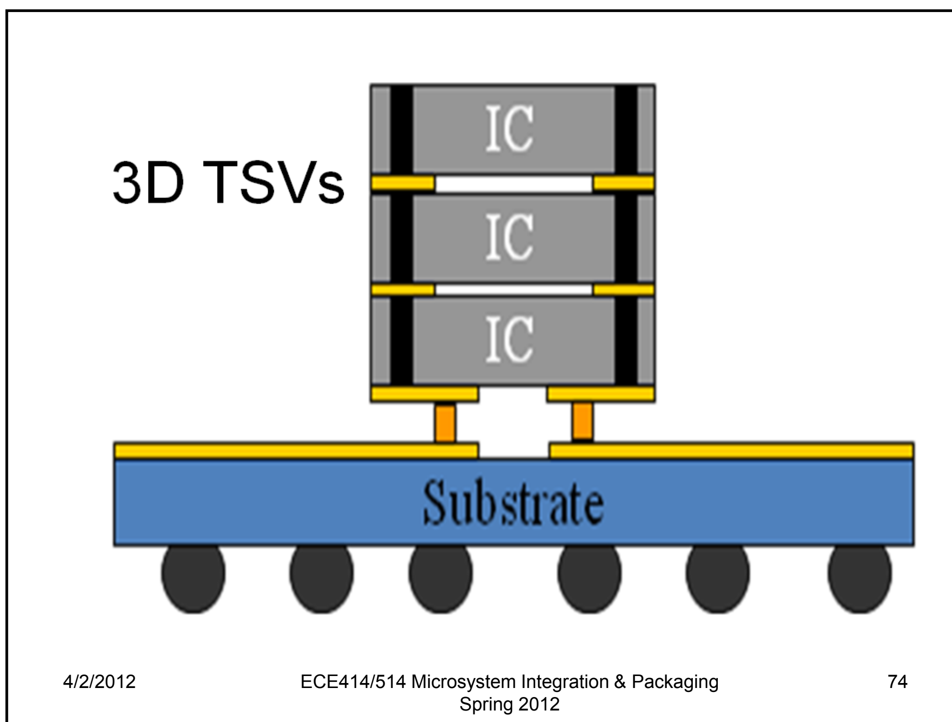


Figure 1.11 NEC's 3-D stack-up chip scale package (CSP) for memory devices.



Lecture Summary

- Standard packages
  - Encapsulation
- First level interconnect (chip to package):
  - Wire-bond, TAB, flip-chip (C4)
- Second-level interconnect (package to board):
  - PTH, SMT, PGA, BGA (C4/C5), etc
- MCMs, CSPs, WLP, etc

Homework #1

Dally, Lall & Suhling:

Problems:

1.10	2.2	2.36
1.12	2.17	2.37
1.14	2.33	4.18
1.21	2.34	