ECE414/514
Electronics Packaging
Spring 2012 Lecture 11
Thermal A
Thermal Conduction

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Lecture topics

- Introduction: Package cooling
- Conduction paths in packaging
- Thermal resistances
- Interface contact resistance
- PWB modeling
- Convection effects
- Transient effects
- Thermal diffusion and pulsed sources

Objectives

- Understand the roles of conduction, convection, and radiation in chip cooling
- Be able to identify and model conduction paths by numerical calculation
- Understand the origins of second order effects:
  – Composite media, transients, pulsed sources

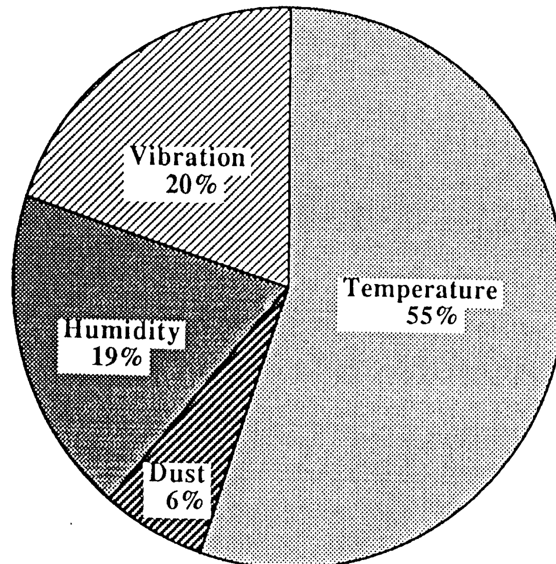
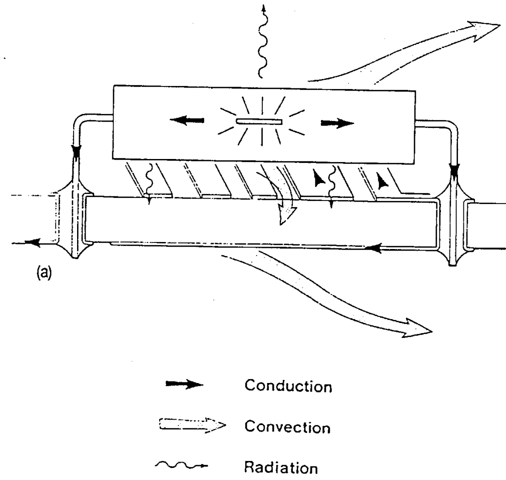


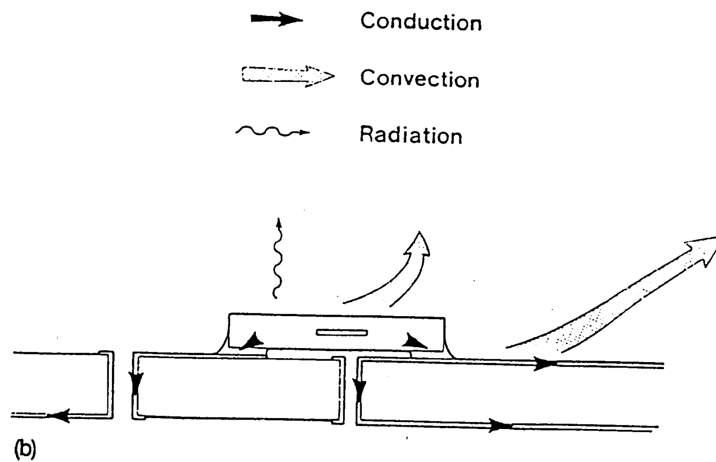
Figure 1.18 Sources of stress in electronic equipment.

Heat dissipation from PTH pkg

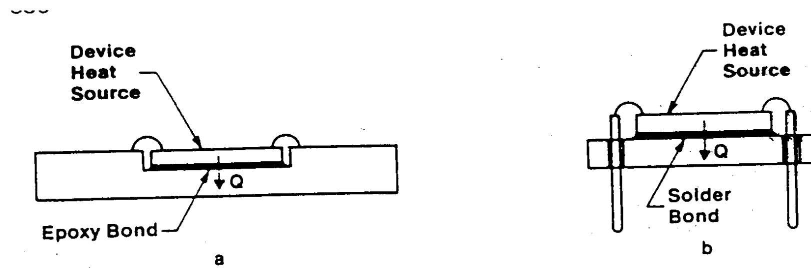


Heat dissipation from a SMT pkg

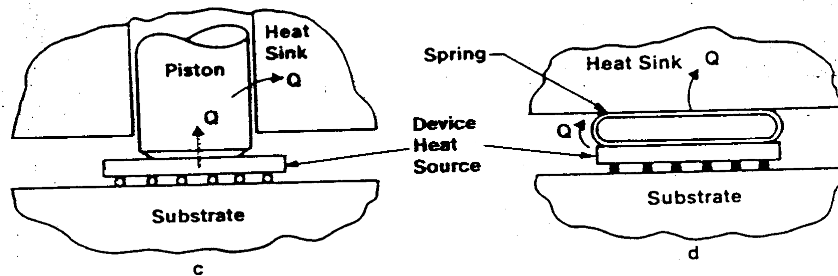
Conduction
Convection
Radiation

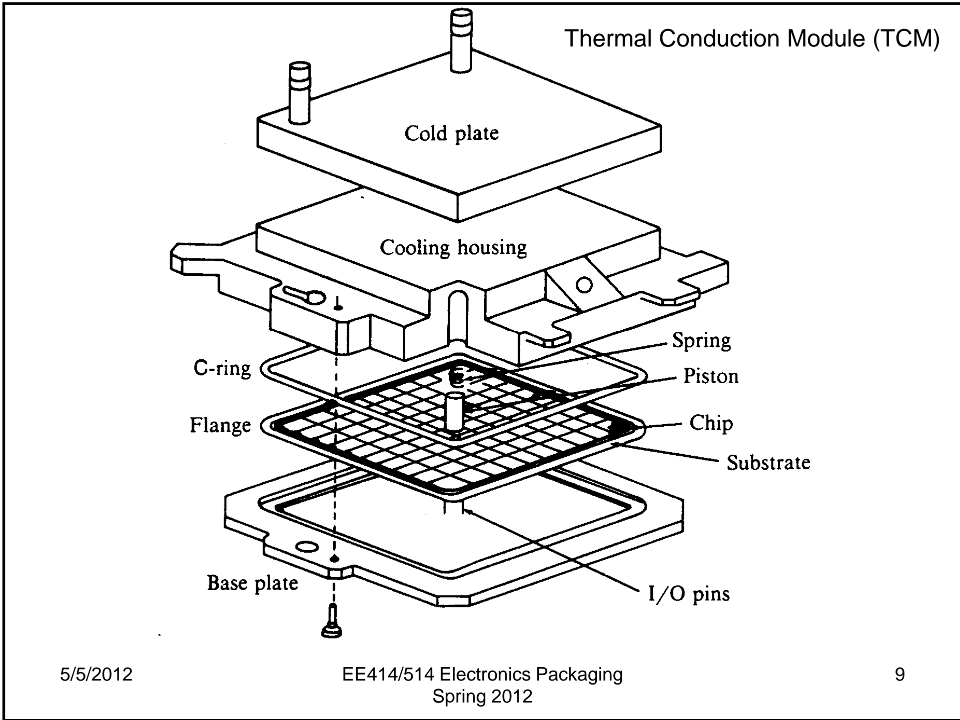


Cooling: Basic



Cooling: Heat sinks




Thermal Conduction Module (TCM)
Cold plate
Cooling housing
Spring
C-ring
Piston
Flange
Chip
Substrate
Base plate
I/O pins
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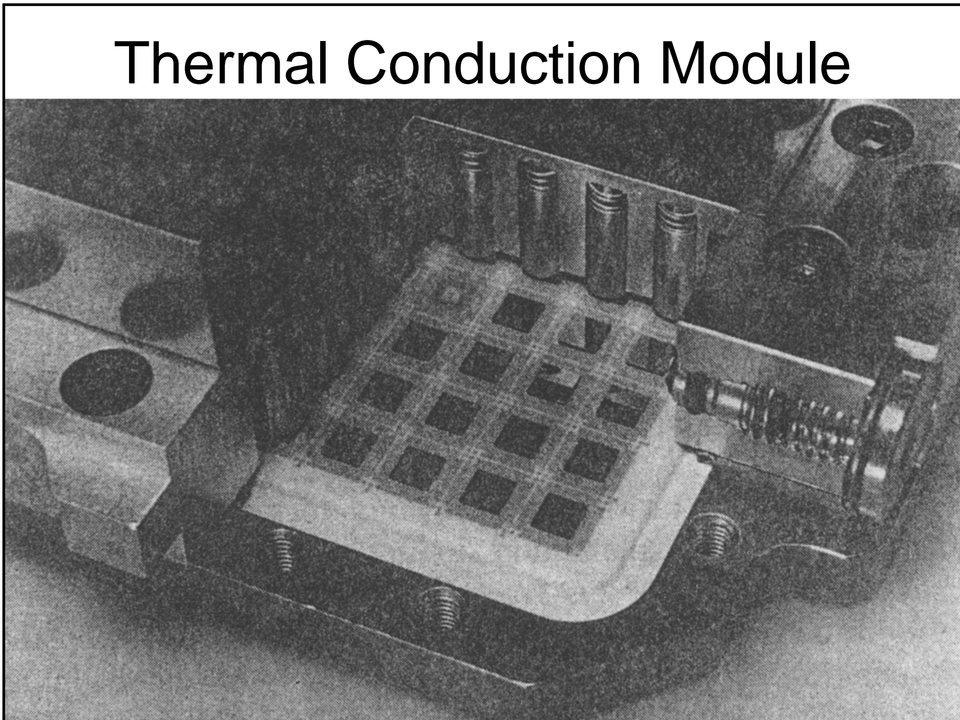
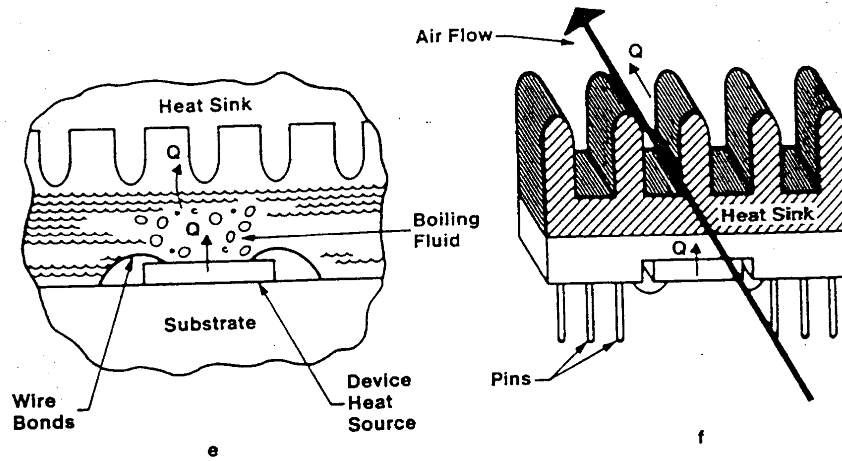

Thermal Conduction Module

Cooling: Boiling/Air-cooled



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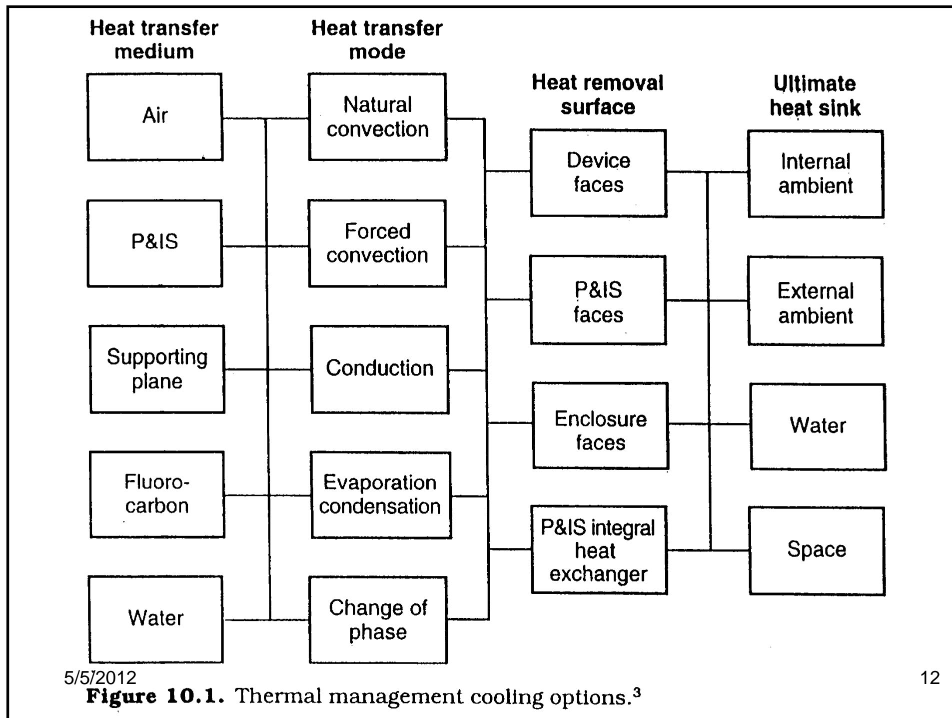

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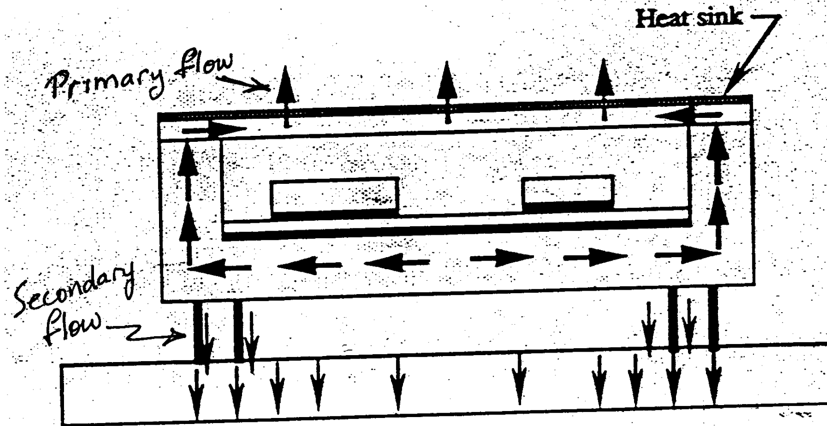
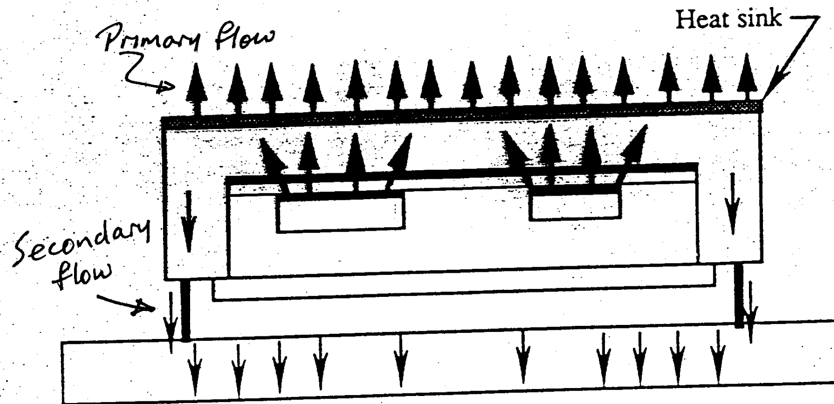
Figure 10.1. Thermal management cooling options.[3]

Cavity-up package with heat-sink



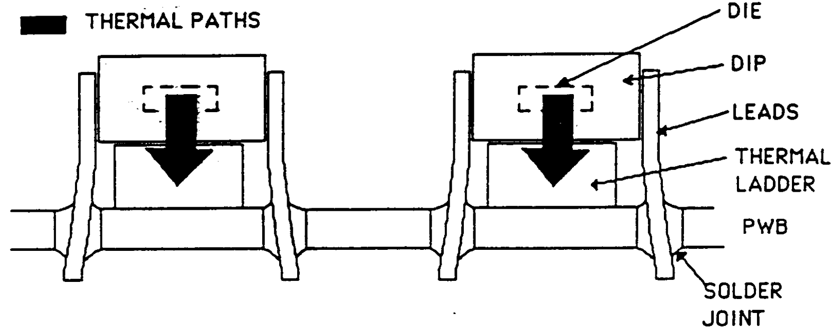
a. Cavity-up package

Cavity-down pkg with heat-sink



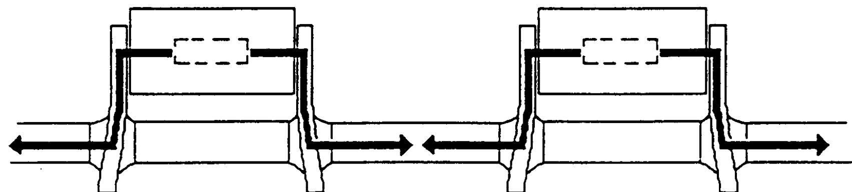
b. Cavity-down package

Thermal ladder



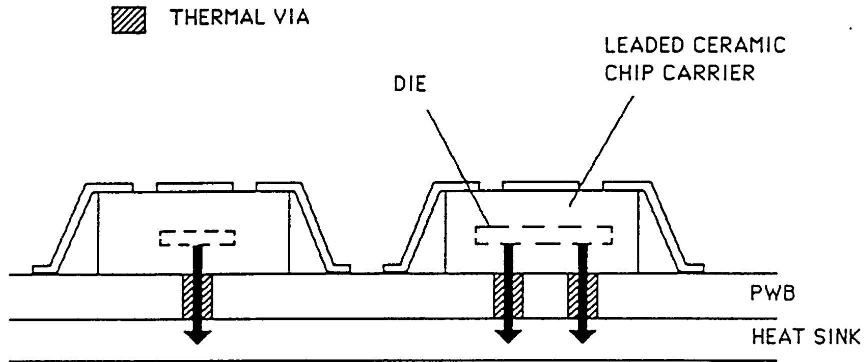
(a) INSERTION MOUNT ORGANIC PWB WITH THERMAL LADDER. HEAT IS DISSIPATED FROM THE DIE THROUGH THE DIP PACKAGE FLOOR TO THE HEAT SINK

DIL PTH in PWB



(b) INSERTION MOUNTED ORGANIC PWB. SINCE THE DIP STANDS OFF THE PWB, THE HEAT MUST BE TRANSFERRED FROM THE DIE, THROUGH THE DIP PACKAGE, THROUGH THE LEADS, THROUGH THE SOLDER, TO THE PWB, OUT TO AN EDGE SUPPORT HEAT SINK.

SMT with thermal vias



(c) LEADED SURFACE MOUNTED ORGANIC PWB WITH CAVITY UP CHIP CARRIERS

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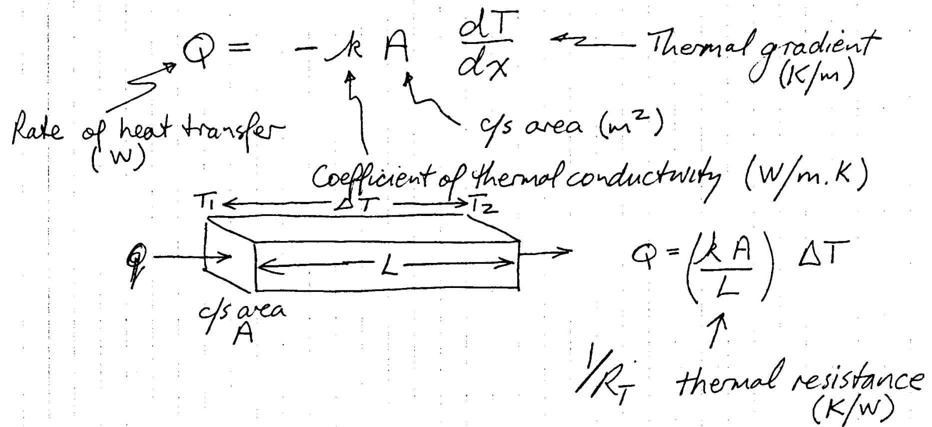
Heat Transfer: Conduction



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Generalization

Generalized case: $\nabla^2 T + \frac{Q_i}{k} = \frac{1}{\alpha}\frac{\partial T}{\partial t}$

$\left(\nabla^2 = \frac{\partial^2}{\partial x^2} + \frac{\partial^2}{\partial y^2} + \frac{\partial^2}{\partial z^2}\right)$

Q_i: internal heat sources (W/m^3)

α thermal diffusivity (m^2/s) $= k/c\rho$

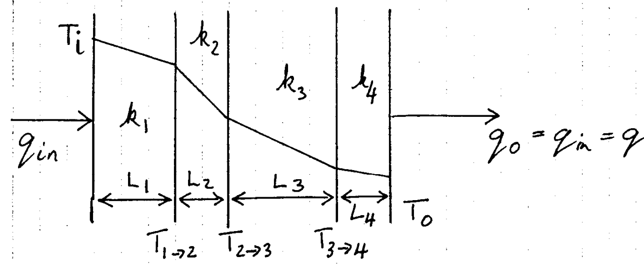
Specific heat ($J/Kg K$) → c; density (Kg/m^3) → ρ

For steady state $\partial T/\partial t = 0$ $\quad \nabla^2 T \rightarrow -Q_i/k$ (Poisson's Eqⁿ)

& for no internal sources $Q_i = 0$ $\quad \nabla^2 T \rightarrow 0$ (LaPlace's Eqⁿ)

1D case $\longrightarrow \frac{dT}{dx} = \text{const.}$

Multiple layers



$$\left.\begin{aligned} T_i - T_{1\to2} &= q\,(L_1/k_1 A) \\ T_{1\to2} - T_{2\to3} &= q\,(L_2/k_2 A) \\ T_{2\to3} - T_{3\to4} &= q\,(L_3/k_3 A) \\ T_{3\to4} - T_o &= q\,(L_4/k_4 A) \end{aligned}\right\}$$

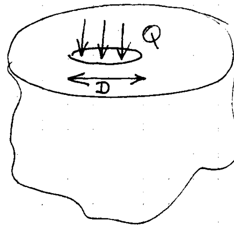
$$\begin{aligned} \Delta T &= T_i - T_o \\ &= \frac{q}{A}\left(\frac{L_1}{k_1} + \frac{L_2}{k_2} + \frac{L_3}{k_3} + \frac{L_4}{k_4}\right) \\ &= q\,(R_{T1} + R_{T2} + R_{T3} + R_{T4}) \end{aligned}$$

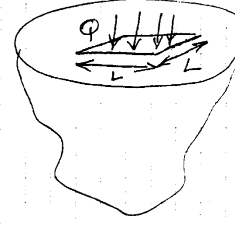
Heat transfer: Chip to Chip Carrier

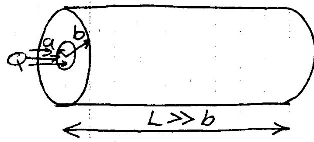
Approximation for heat transfer from small sources:

$\Delta T = Q(R_{TS} + R_T)$

Additional term due to constriction from small area.



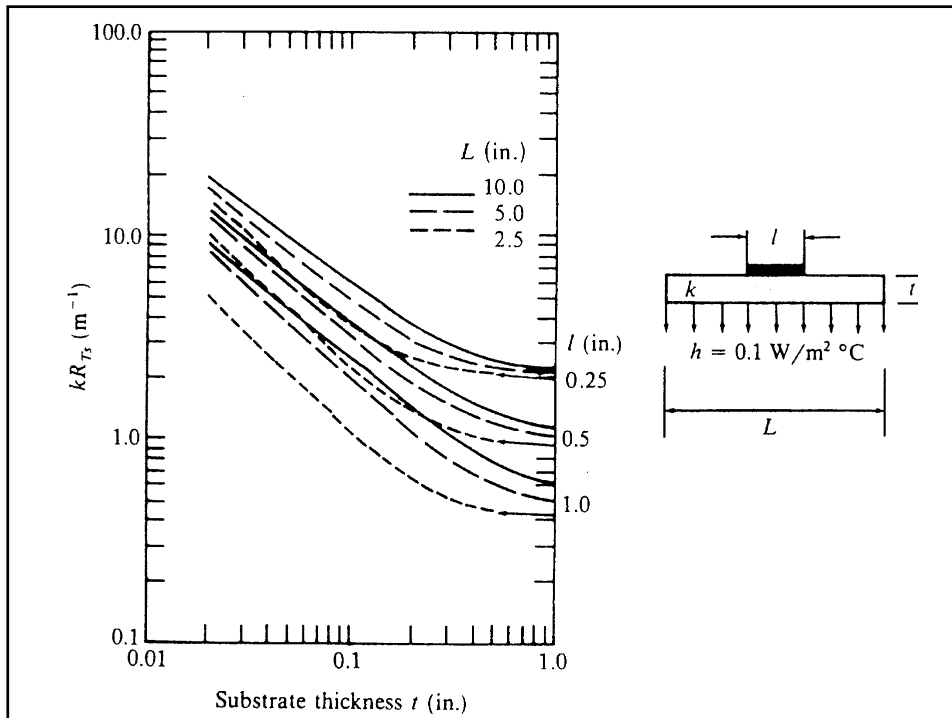




Circular source
$R_{TS} = 16/3\pi^2 Dk$
$= 0.54/Dk$

Square source
$R_{TS} = 0.55/Lk$

$R_{TS} = (1/2\sqrt{\pi}ak)(1 - \frac{a}{b})^{3/2}$



Numerical example

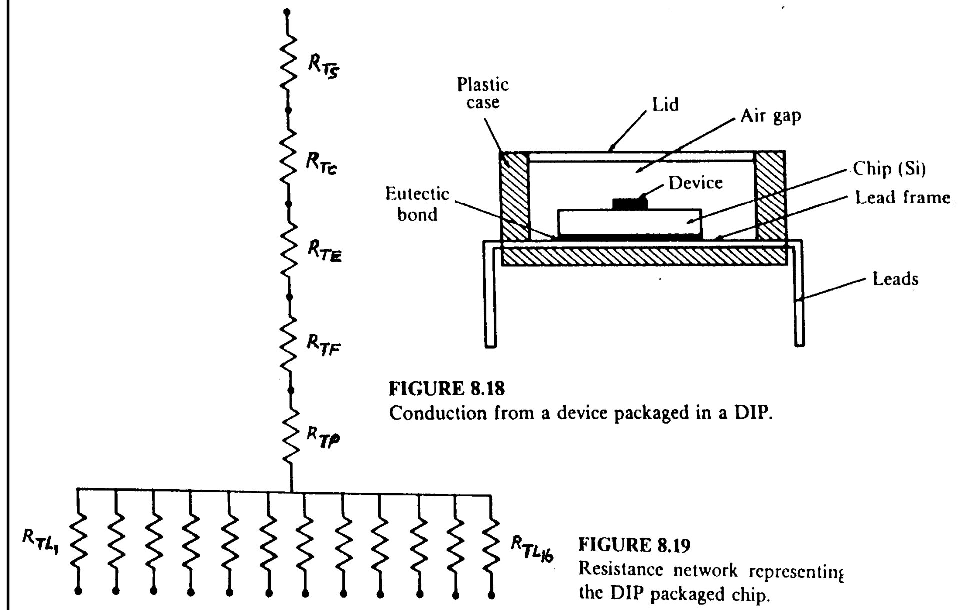


FIGURE 8.18
Conduction from a device packaged in a DIP.

FIGURE 8.19
Resistance network representing the DIP packaged chip.

Calculation: part 1

~~material involved~~. Begin at the top of the resistance network with the first resistor R_{T_s}. This thermal resistance, due to the spreading of heat from the device to the chip, is estimated from Eq. (8.50) as

$$\begin{aligned} R_{T_s} &= \left[1/(2\sqrt{\pi}\, ak)\right]\left[1 - (a/b)\right]^{3/2} \\ &= \left[1/(2\sqrt{\pi} \times 0.0005 \times 154)\right]\left[1 - (0.5/2)\right]^{3/2} \\ &= 2.38°\mathrm{C/W} \end{aligned}$$

where we have selected the following quantities:

$a = 0.5$ mm is the radius of the circular area of the device
$b = 2$ mm is the radius of an inscribed circle on a 4×4 mm chip
$k = 154$ W/m °C for silicon

The resistance of the chip, eutectic bond and the lead frame are determined from $R = L/(kA)$ as follows:

Calculation: part 2

For the silicon chip:

$$R_{TC} = 0.508 \times 10^{-3}/(154 \times 16 \times 10^{-6}) = 0.21°\text{C/W}$$

where $L = 0.508$ mm is the chip thickness
$A = 16\ \text{mm}^2$ is the chip area

For the eutectic bond:

$$R_{TE} = 0.05 \times 10^{-3}/(296 \times 16 \times 10^{-6}) = 0.01°\text{C/W}$$

where $L = 0.05$ mm is the bond thickness
.$k = 296$ W/m °C is the coefficient of thermal conductivity for the AuGe solder

For the lead frame:

$$R_{TF} = 0.25 \times 10^{-3}/(381 \times 16 \times 10^{-6}) = 0.08°\text{C/W}$$

where $L = 0.25$ mm is the frame thickness
$k = 381$ W/m °C is the coefficient for copper

Calculation: part 3

The thermal resistance from the base of the lead frame to the leads can only be approximated because of the complexity of the geometry as indicated in Fig. 8.20. Several simplifications are made in determining the thermal resistance R_{TP}:

$$R_{TP} = 0.2 \times 10^{-3}/(1 \times 4 \times 10^{-6}) = 50°\text{C/W}$$

where $L = 0.2$ mm the average space between the base and the leads
$k = 1$ W/m °C for the plastic insulation filling this space
$A = 4\ \text{mm}^2$ for all 16 leads each 0.25 mm thick and 1 mm wide

This thermal resistance is extremely high and, while the calculation is approximate, it does indicate the difficulty in dissipating heat in a molded plastic chip carrier.

Calculation: part 4

The final thermal resistance to be determined is for the individual leads from the heat frame to the exterior of the DIP:

$$R_{TL} = 6 \times 10^{-3}/(381 \times 0.25 \times 10^{-6}) = 63°C/W$$

where $L = 6$ mm is the average lead length. The 16 individual leads are equivalent to 16 resistances in parallel that can be combined to give

$$R_{TLe} = R_{Tl}/N = 63/16 = 3.94°C/W$$

Summing the resistances in the network to obtain the total resistance $R_T = 56.62°C/W$ is shown in Table 8.5. For a chip dissipating 0.5 W housed in this plastic DIP-type chip carrier, the ΔT between the junction and the case is determined from Eq. (8.25) as

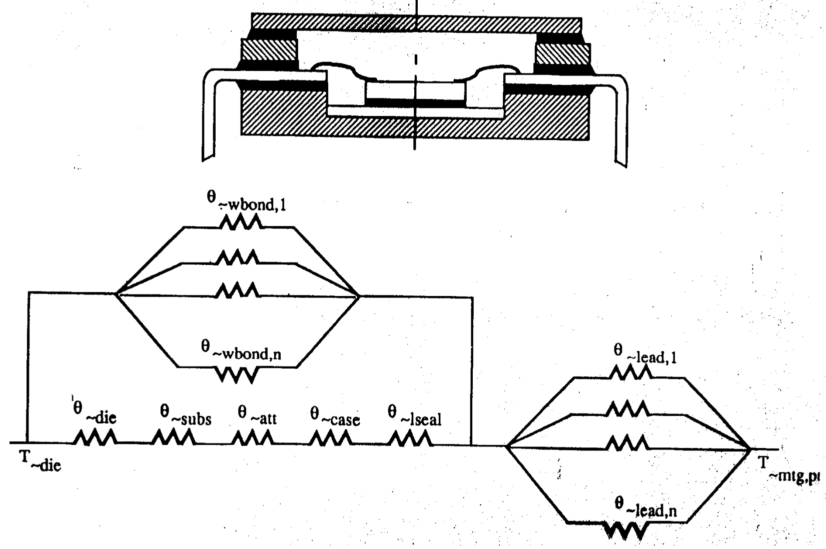
$$\Delta T = qR_T = 0.5 \times 56.62 = 28.31°C$$

Calculation: Summary

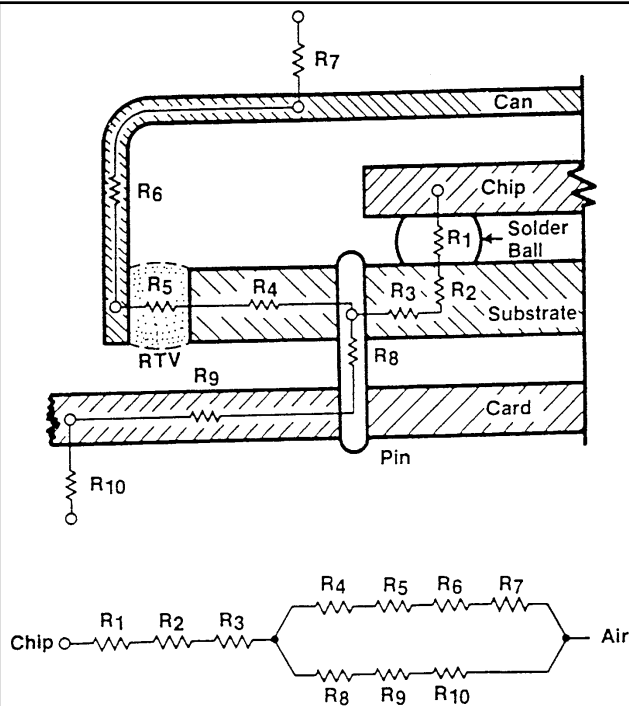
TABLE 8.5
Listing of resistances for the various components in the heat path for a plastic DIP

Component	Symbol	Resistance (°C / W)
Spreading	R_{TS}	2.38
Chip	R_{TC}	0.21
Eutectic bond	R_{TE}	0.01
Lead frame	R_{TF}	0.08
Plastic	R_{Tp}	50.0
Leads (effective)	R_{TLe}	3.94
Total	R_T	56.62

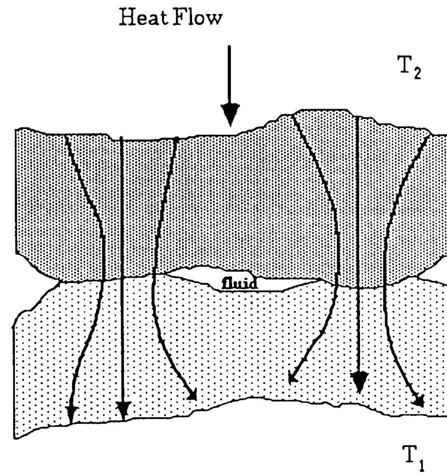
Package model #2



Package model #3



Heat flow across contacts



$q = (T_2 - T_1)/R_{contact}$

$R_{contact} = 1/h_c A_{apparent}$

h_c : Contact Coefficient

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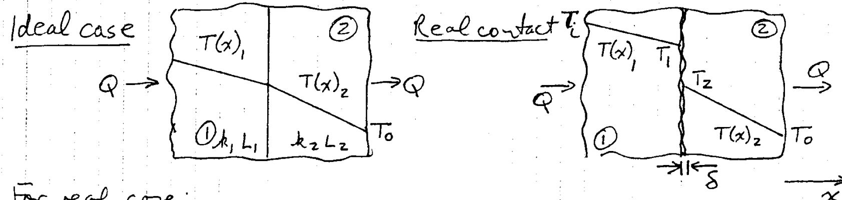
Contact/Interface Resistance



For real case:

$$T_i - T_1 = Q L_1 / k_1 A$$

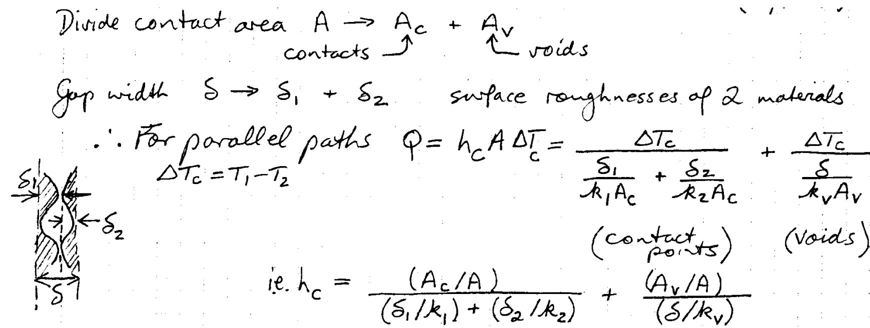
$$T_1 - T_2 = Q / h_c A \quad \text{where } h_c \text{ represents effective } k/L \text{ for partial gaps.}$$

$$T_2 - T_o = Q L_2 / k_2 A$$

$$\therefore \Delta T = T_i - T_o = (Q/A)\left[(L_1/k_1) + (1/h_c) + (L_2/k_2)\right]$$

h_c is "contact coefficient" $(W/m^2 K)$

Contact coefficient



Contact coefficient approx'n

In practice — δ's etc difficult to find

∴ Approximation $h_c = 0.55\, m \left(\frac{k}{\sigma}\right)\left(\frac{P}{H}\right)^{0.85}$

where $k = \frac{2 k_1 k_2}{k_1 + k_2}$ & $\sigma^2 = \sigma_1^2 + \sigma_2^2$

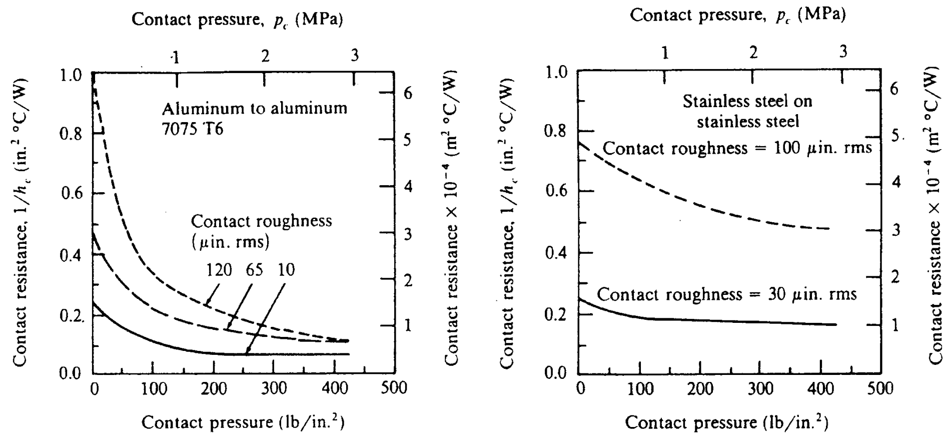
σ_1, σ_2 rms surface roughnesses

m rms slope of contact asperities

P contact pressure

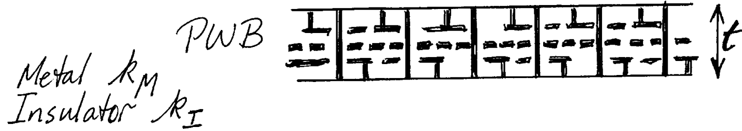
H hardness of softer material (~3x yield strength)

Contact heat transfer coeff: pressure



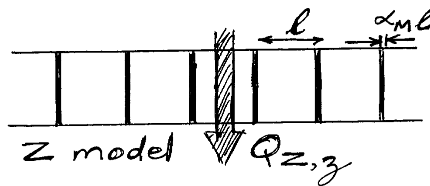
Heat conduction through PWBs

PWB



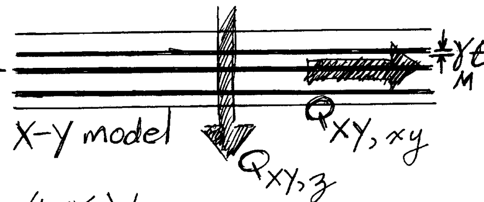
Metal k_M

Insulator k_I



$$k_{Z,z} = \alpha_M k_M + (1-\alpha_M) k_I$$

Z model $Q_{Z,z}$



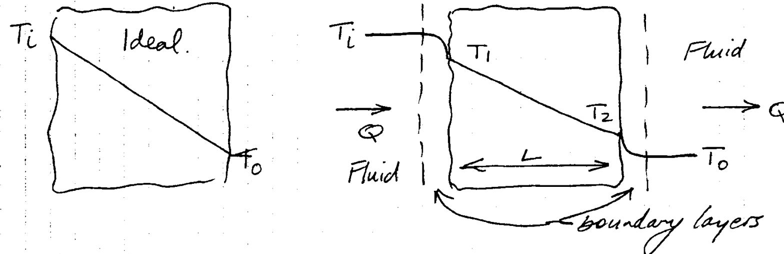
$$k_{XY,z} = \frac{1}{\frac{\gamma_M}{k_M} + \frac{1-\gamma_M}{k_I}}$$

X-Y model $Q_{XY,xy}$ $Q_{XY,z}$

$$k_{XY,xy} = \gamma_M k_M + (1-\gamma_M) k_I$$

Effect of Convection on Conduction

In practice, surface temperatures of solids NOT ambient, etc due to surface boundary layers)



Heat transfer across boundary layers by convection

$$\left.\begin{aligned} T_i - T_1 &= Q/h_i A \\ T_1 - T_2 &= Q\,L/kA \\ T_2 - T_o &= Q/h_o A \end{aligned}\right\} \Delta T = T_i - T_o = \frac{Q}{A}\left(\frac{1}{h_i} + \frac{L}{k} + \frac{1}{h_o}\right)$$

$$\therefore R_T = A^{-1}\left(\frac{1}{h_i} + \frac{L}{k} + \frac{1}{h_o}\right) \text{ etc.}$$

Transient effects

Device dissipates heat at rate Q_g.

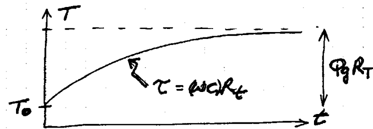
(T, Q_g, R_T, w,c, T_o ambient)

$$Q_g = \frac{T - T_o}{R_T} + (wc)\frac{dT}{dt}$$

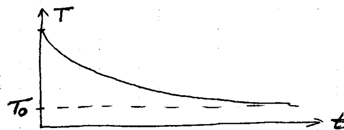
gives $\frac{dT}{dt} + \frac{T}{wcR_T} = \frac{1}{wc}\left(Q_g + \frac{T_o}{R_t}\right)$

solution $T = A \exp -\frac{t}{wcR_t} + Q_g R_T + T_o$

If $T = T_o$ at $t = 0$



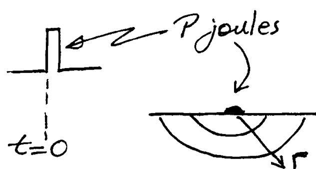
If Q_g turned off at $t=0$



Thermal cycling profile as devices turned on & off.

Thermal capacitance $C = wc = \rho \times vol \times c$ ← specific heat

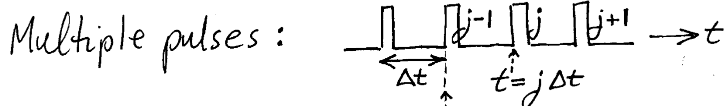
Thermal Diffusion



$$T(t,r) = \frac{P/\rho c}{4(\pi K t)^{3/2}} \exp -\left(\frac{r^2}{4Kt}\right)$$

K = thermal diffusivity $= \frac{k}{\rho c}$

Multiple pulses :



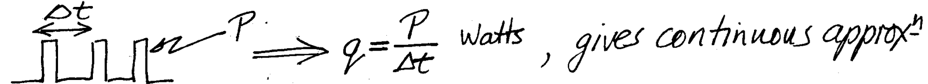
$t = (j-1)\Delta t$

Superposition (discrete pulses)

$$T_D = \sum_{j=1}^{J} \frac{P/\rho c}{4(\pi K)^{3/2}} \frac{1}{[t-(j-1)\Delta t]^{3/2}} \exp - \frac{r^2}{4K[t-(j-1)\Delta t]}$$

Thermal pulses, e.g. CMOS

EFFECTIVE SOURCE for PULSED POWER



$\Rightarrow q = \frac{P}{\Delta t}$ Watts , gives continuous approx^n

$$T_c(r,t) = \frac{q/\rho c}{2\pi K r} \operatorname{erfc} \frac{r}{\sqrt{4Kt}} \xrightarrow{t\to\infty} \frac{q/\rho c}{2\pi K r} = \frac{q}{(2\pi r) k}$$