# ECE414/514
# Electronics Packaging
## Spring 2012 Lecture 1

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# A. Introduction

- 1 Course review; the package roadblock to system performance
- 2 Packaging technologies

# B. Electrical

- 3 CMOS technology; R, L, & C; ground planes; delta-I noise
- 4 Transmission line theory
- 5 Reflections; EMI/EMC
- 6 Crosstalk
- 7 Electromagnetic modeling



# C. Mechanical

- 9 Basics: stress modeling, etc
- 10 Thermomechanical stress modeling; vibrations
- 11 Fracture mechanics and fatigue

# D. Thermal

- 12 Conduction
- 13 Convection; radiation



# E. Materials

- 14 Metals, phase diagrams, solder, interfaces, diffusion, intermetallics
- 15 Polymers (chemistry, curing, and properties); plastic packaging

# F. Reliability

- 16 Reliability theory, HAST
- 17 Failure Modes I



## Why is Packaging Important?

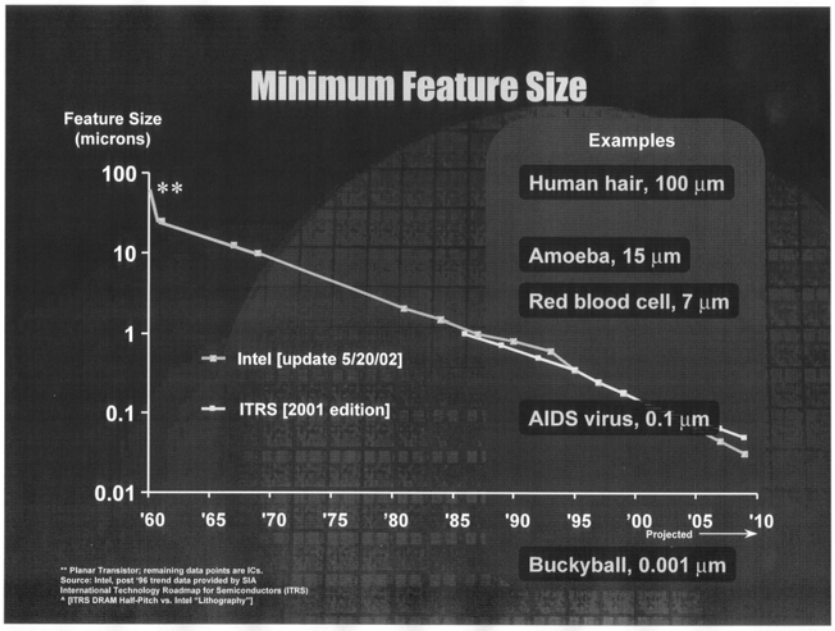
- **Elementary example:**

| | Semiconductor Chip Parameters | |
|---|---|---|
| | **1980** | **1990** |
| **Feature size** | **4 µm** | **1 µm** |
| **Chip area** | **0.3 $cm^2$** | **1.5 $cm^2$** |
| **Gates/chip** | **5,000** | **100,000** |
| **µP clock freq** | **6 MHz** | **40 MHz** |
| **Power** | **2 W** | **10 W** |
| **I/O count** | **64** | **1500** |

# Chip density, power, speed

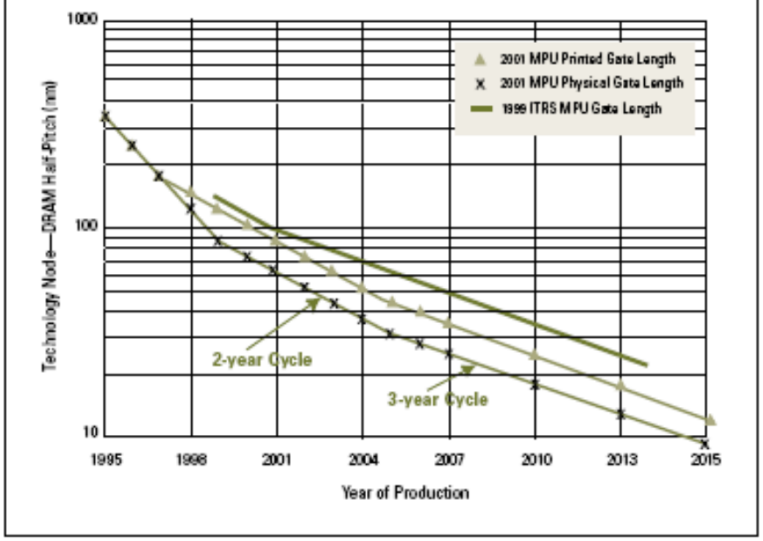
| | 1980 | | 1990 | |
|---|---|---|---|---|
| Ckt size | $L^2$ | $4\mu \rightarrow 1\mu$ | $L^2/16$ | |
| Chip size | $0.3cm^2$ | $5xArea \rightarrow$ | $1.5cm^2$ | |
| Ckts/chip | N | $\rightarrow$ | 5x16N=80N | (20N) |
| Pwr diss$^n$ | 2w | $I \div 4 \rightarrow$ | 80x2w/4=40w | (10w) |
| Clk freq | 6MHz | C/16, I/4 | 24MHz | (40MHz) |





Borsuk & Coffey, Defense Horizons

**Figure 1. IC Feature Gate Size**






# ITRS product categories

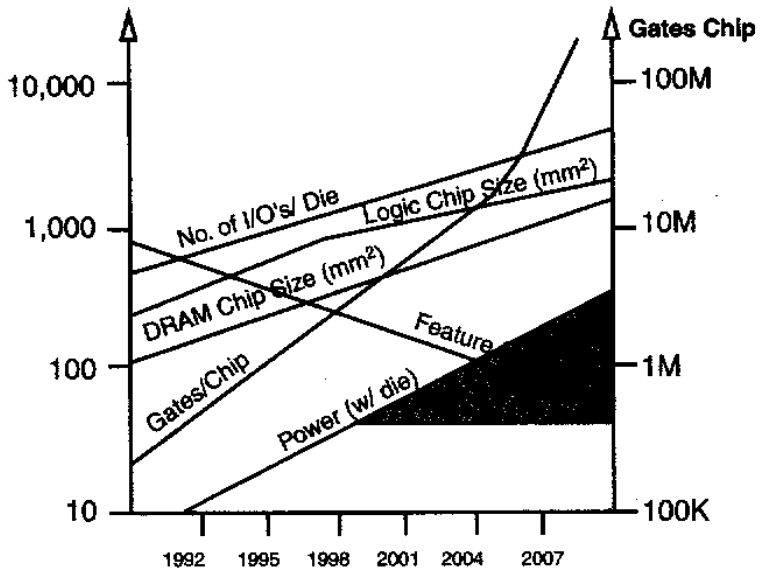
| Product category | Product description |
|---|---|
| Low cost | <$ 300: consumer products, microcontrollers, disk drivers |
| Hand-held | <$ 1000: battery powered products e.g. mobile and cellular products |
| Cost/performance | <$3000: notebooks, desktop personal computers |
| High performance | >$3000:high-end work stations, servers, avionics, supercomputer |
| Harsh environment | Under-the-hood and other hostile environment products |
| Memory | DRAM's, SRAM's |

# ITRS Packaging requirements

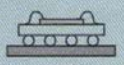
| | 1992 | 1995 | 1998 | 2001 | 2004 | 2007 |
|---|---|---|---|---|---|---|
| Feature Size ($\mu m$) | 0.5 | 0.35 | 0.25 | 0.18 | 0.12 | 0.07 |
| Gates/chip | 300K | 800K | 2M | 5M | 10M | 100M |
| Transistors ($cm^{-2}$) | 0.01B | 0.04B | 0.1B | 0.22B | 0.6B | 2.1B |
| Chip Size ($mm^2$) | | | | | | |
| Logic/Uniprocessor | 250 | 400 | 600 | 800 | 1000 | 1250 |
| DRAM | 132 | 200 | 320 | 500 | 700 | 1000 |
| Maximum Power (W/Die) | | | | | | |
| High Performance | 10 | 15 | 30 | 40 | 40–120 | 40–200 |
| Portable | 3 | 4 | 4 | 4 | 4 | 4 |
| Power Supply Voltage (V) | | | | | | |
| Desktop | 5 | 3.3 | 2.2 | 2.2 | 1.5 | 1.5 |
| Portable | 3.3 | 2.2 | 2.2 | 1.5 | 1.5 | 1.5 |
| No. I/Os | 500 | 750 | 1500 | 2000 | 3500 | 5000 |



# Semi-log Moore's plots of the Road-map data



# Package lead pitch, frequency, power dissipation, comparisons

| Package | DIP | QFP | CSP | Flip Chip |
|---|---|---|---|---|
| Top View Showing Chip to Package Connections |  |  |  |  |
| Plane View Showing Package to Board Connections |  |  |  |  |
| Chip Size (mm × mm) | 5 × 5 | 16 × 16 | 25 × 25 | 36 × 36 |
| Chip Perimeter (mm) | 20 | 64 | 100 | 144 |
| Number of I/Os | 64 | 500 | 1600 | 3600 |
| Chip Pad Pitch (μm) | 312 | 128 | 625 | 600* |
| Package Size (in. × in.) | 3.3 × 1.0 | 2.0 × 2.0 | 1.0 × 1.0 | 1.4 × 1.4 |
| Package Lead Pitch (mils) | 100 | 16 | 25 | 24 |
| Chip Area ($mm^2$) | 25 | 256 | 625 | 1296 |
| Feature Size (μm) | 2.0 | 0.5 | 0.25 | 0.125 |
| Gates/Chip | 30K | 300K | 2M | 10M |
| Chip Area/(70× Feature Size)$^2$ | 1.25K | 200K | 2M | 16.4M |
| Maximum Frequency (MHz) | 5 | 80 | 320 | 1.28 GHz |
| Power Dissipation (W) | 0.5 | 7.5 | 30 | 120 |
| Chip Power Density ($W/cm^2$) | 2.9 | 4.8 | 9.3 | 2.0 |
| Package Power Density ($W/cm^2$) | 0.024 | 0.3 | 4.8 | 9.8 |
| Supply Voltage (V) | 5 | 3.3 | 2.2 | 1.5 |
| Supply Current (A) | 0.1 | 2.3 | 13.6 | 80 |
| *Chip Supply Lead Current Density ($A/mm^2$) | 5.23 | 143 | 11.08 | 31.43 |
| *Package Supply Lead Current Density ($A/mm^2$) | 1.6 | 11.5 | 11.08 | 31.43 |

# Rent's Rule #1



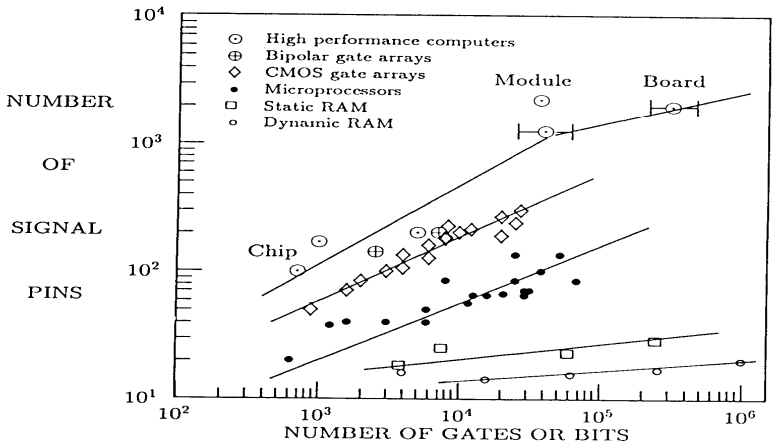



**FIGURE 9.12** Rent's curves according to system and chip types

# Rent's Rule #2



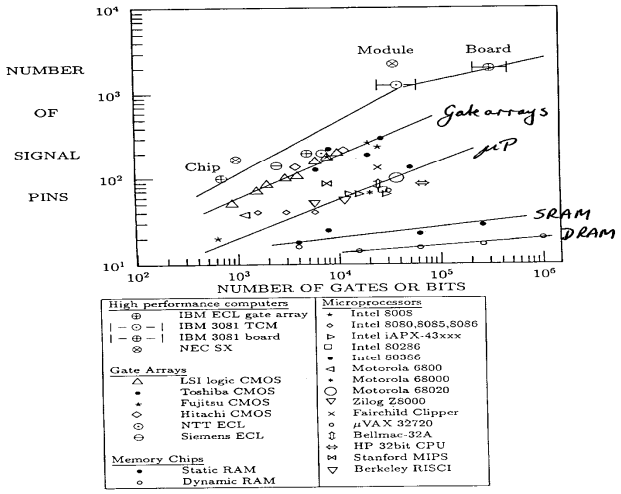
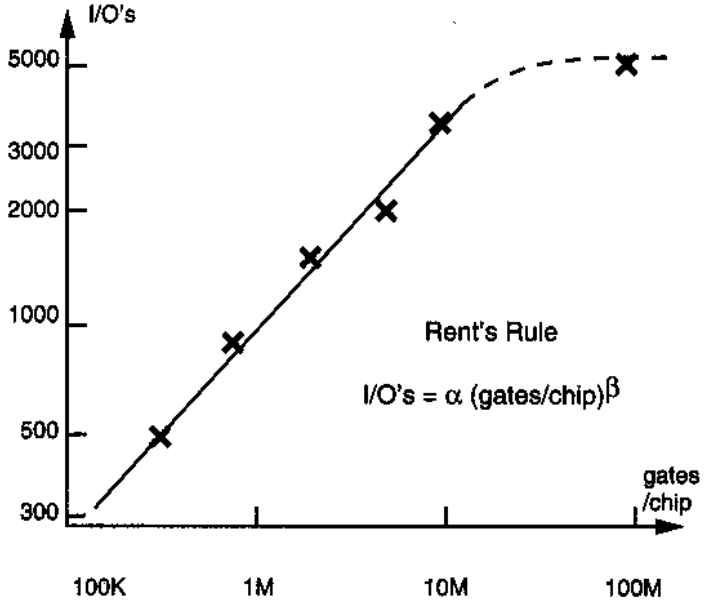



**FIGURE 9.11** Rent's curves for various digital systems. Data points are classified according to product identification.



# Rent's rule plot of roadmap data



# Pkg pins ≈ $K_p$(bits or gates)$^{\beta}$

| | $\beta$ | $K_p$ |
|---|---|---|
| SRAM | 0.12 | 6 |
| μP | 0.45 | 0.82 |
| Gate array | 0.50 | 1.9 |
| Computr:chip | 0.63 | 1.4 |
| Computr:syst | 0.25 | 82 |



# Rent's Rule #3

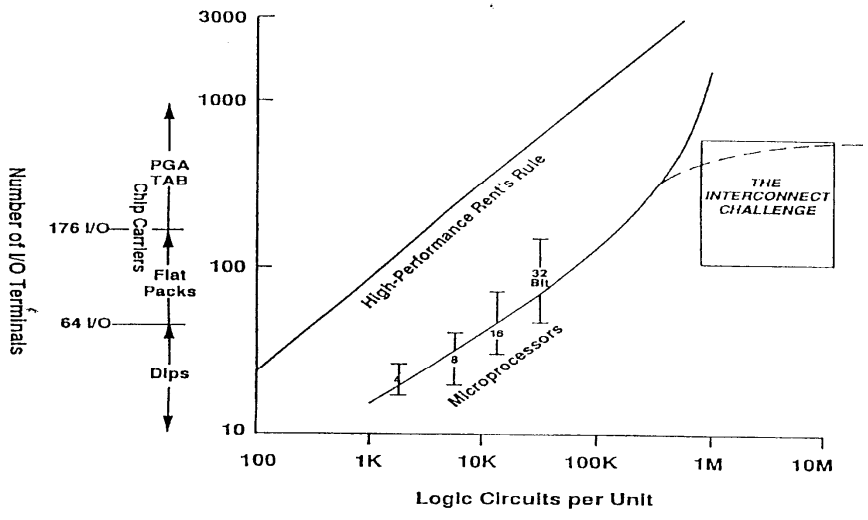



**Figure 1.4.** High-performance Rent's Rule.[4]

# Example I/O

| Package | 1980 | | 1990 |
|---|---|---|---|
| | 64-pin DIL | | 1500-pin QFP |
| | 0.1in pitch | | 0.01in pitch |
| | $3.3 \times 1.0 in^2$ | | $3.75 \times 3.75 in^2$ |
| Pkg I/O | 64 pins | Rent's rule→ | 1500 pins |
| Chip: | $0.6 \times 0.5 cm^2$ | | $1.25 \times 1.2 cm^2$ |
| I/O pitch | 344 μm | | 33 μm |



# Bare and packaged chip speeds

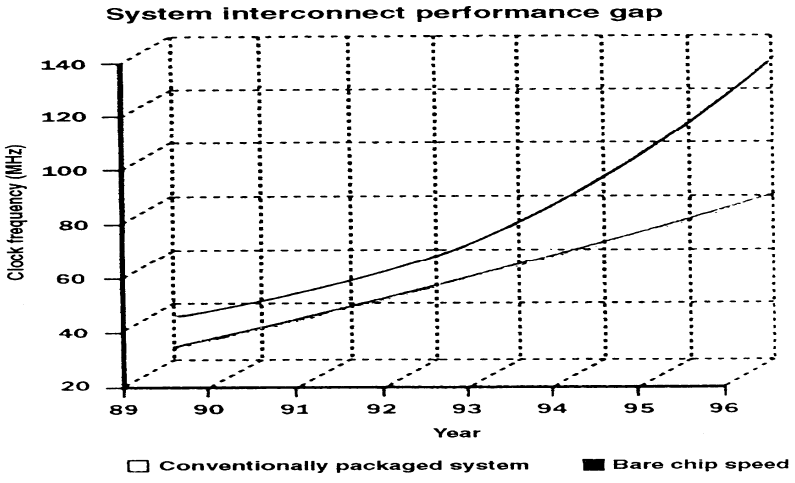



**Figure 1.3.** Bare-chip and conventional packaging speed trends.[2]

# Clock Frequency vs Time

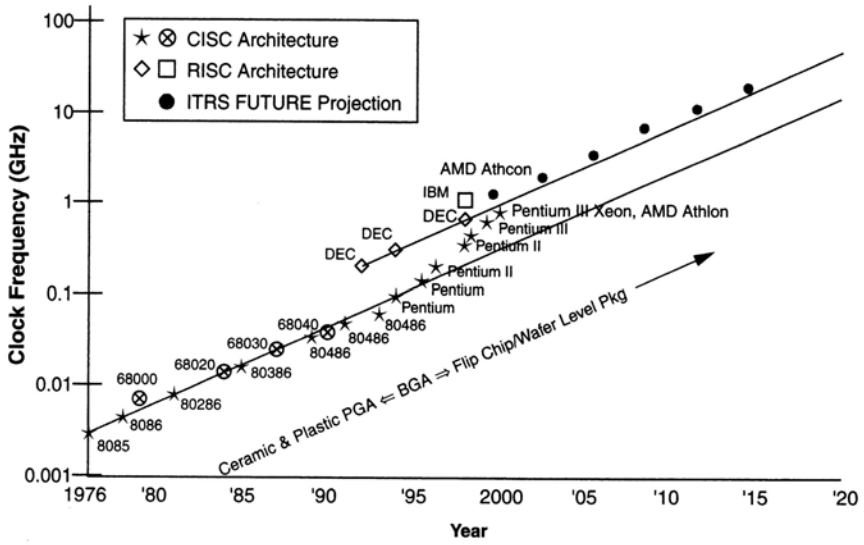



**FIGURE 7.5** Microprocessor and single chip packaging evolution.



# Power dissipation follows clock frequency

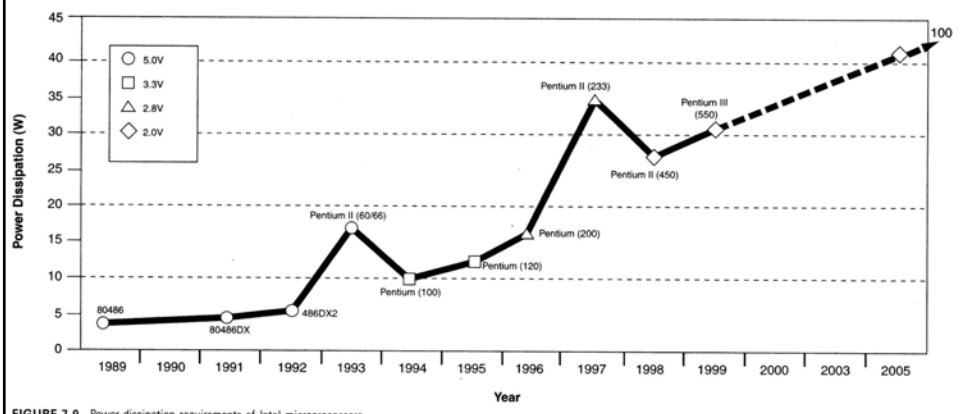



**FIGURE 7.9** Power dissipation requirements of Intel microprocessors.

# Increasing prices

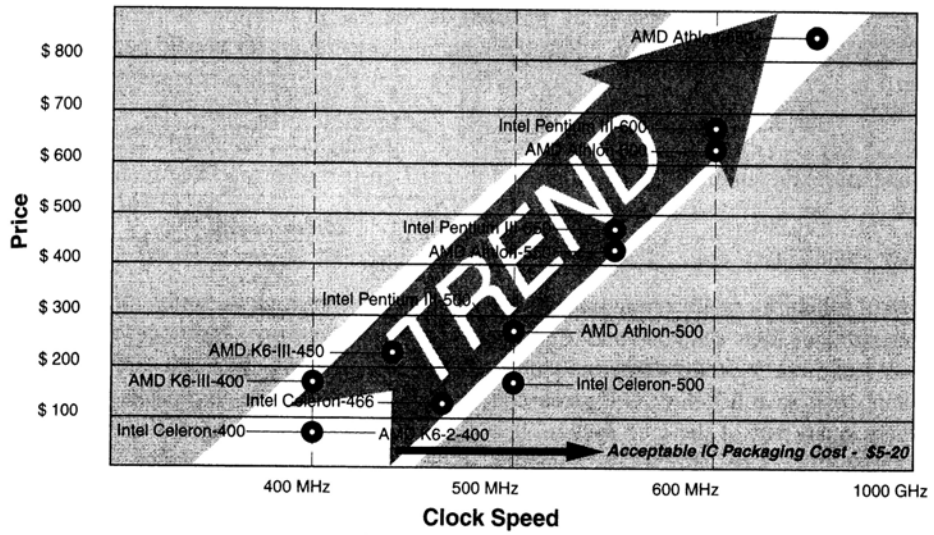



**FIGURE 7.23** Price of IC vs. IC package.



# Technology trend: Japanese consumer electronics

**TABLE 7.3** Single chip package trend for consumer products in Japan.

| Product | Year | | | |
|---|---|---|---|---|
| | 1998 | 2000 | 2005 | 2010 |
| Notebook PC | TCP (0.25)<br>BGA (1.0)<br>CSP (0.8) | CSP (0.75–0.8)<br>FBGA (0.8)<br>Flip Chip (0.2) | CSP (0.5)<br>FBGA (0.5)<br>Flip Chip/WLP (0.15) | CSP (0.5)<br>FBGA (0.5)<br>Flip Chip/WLP (0.1)<br>WLP |
| Hand-held PCs | FBGA (0.8) | FBGA (0.5–0.75) | CSP (0.5)<br>Flip Chip/WLP (0.15) | C4FC (0.5)<br>Flip Chip/WLP (0.1) |
| PDA | FBGA (0.8)<br>FBGA(0.5) | FBGA (0.5) | FBGA (0.5)<br>Flip Chip/WLP (0.15) | FBGA (0.3)<br>Flip Chip/WLP (0.1) |
| Cellular Phones | CSP | CSP | Flip Chip/WLP (0.15) | Flip Chip/WLP (0.1) |
| Audiovisual Equipment | FBGA (0.5–0.8) | FBGA (0.5–0.8) | FBGA (0.4–0.5)<br>Flip Chip/WLP (0.3) | FBGA (0.3–0.5)<br>Flip Chip/WLP (0.2) |

# Trend to CSP

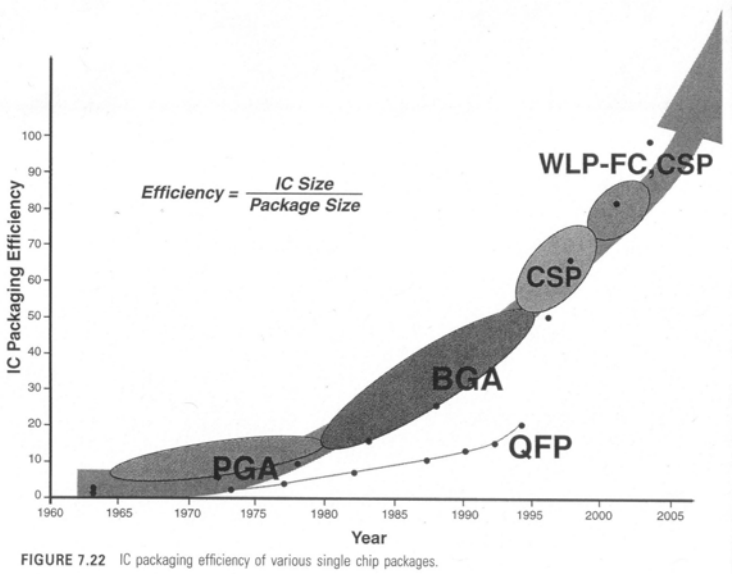



FIGURE 7.22 IC packaging efficiency of various single chip packages.



# Package functions

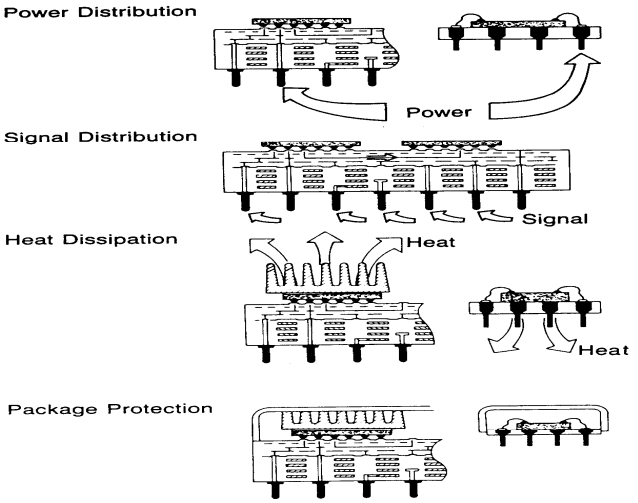


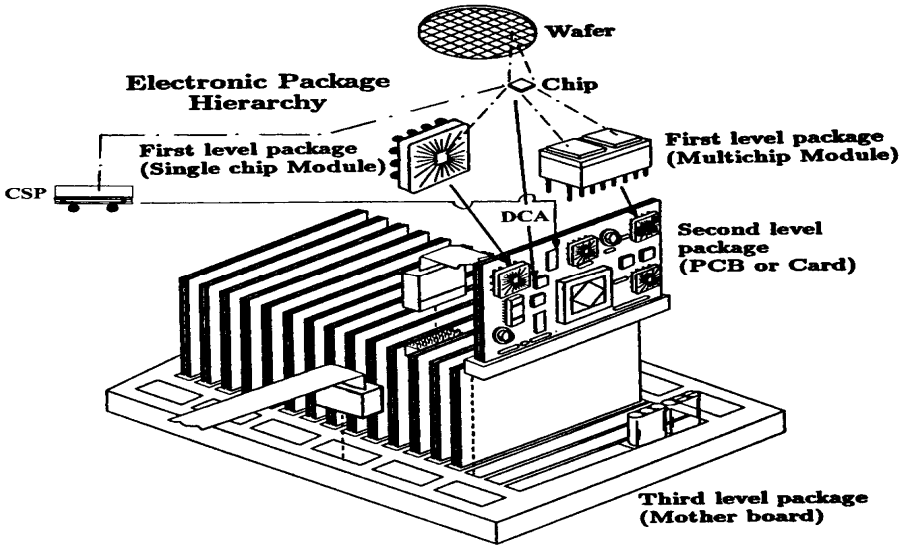

**Figure 1-1. Four Major Functions of the Package.** + Mechanical support.

## Electronics Packaging is Multi-disciplinary!

- Electrical
  - Architectures
  - Power distribution
  - EMI/EMC, crosstalk, ΔI & switching noise
- Mechanical
  - Vibrations
  - Stress
- Thermal
  - Conduction cooling
  - Convection cooling
- Materials
  - Metallurgy
  - Ceramics
  - Polymers
  - Surface science
  - Interfaces/diffusion
- Manufacturing
  - Instrumentation
  - Process control
  - Manufacturability/ Test



## Packaging Levels



# Lead Pitch/Density: peripheral leads, area array, 3D

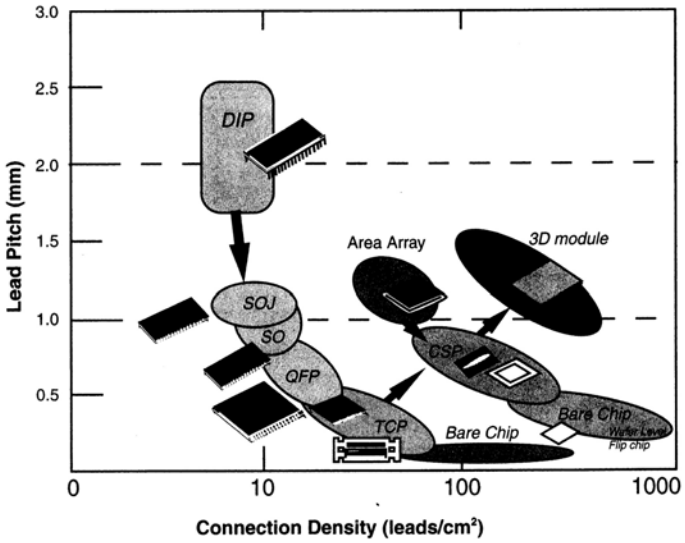



**FIGURE 7.25** Summary of single chip package evolution.



# PWB Density

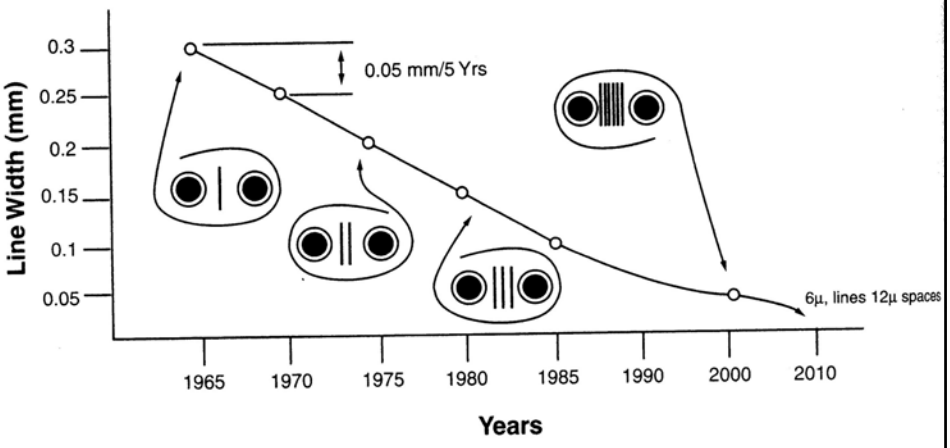



**FIGURE 16.32** PWB roadmap.

# PWB line width, pitch, & pin count

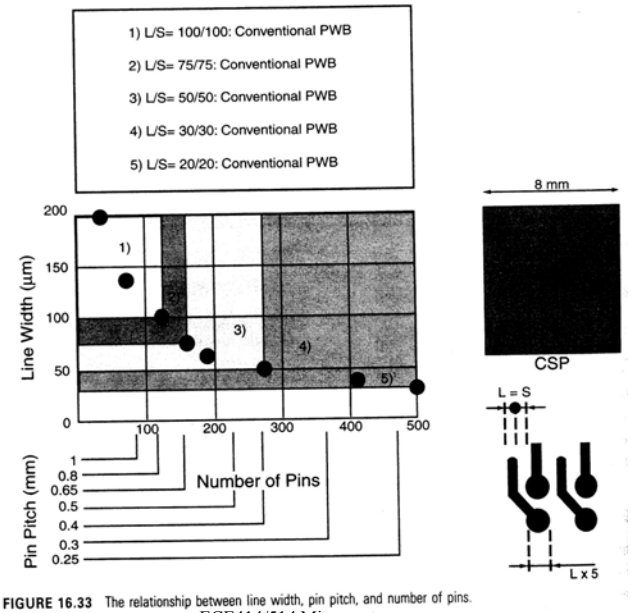



**FIGURE 16.33** The relationship between line width, pin pitch, and number of pins.



# Summary

- Course overview (MS Word doc.)
  - Topic-by-topic & lecture-by-lecture
  - Evaluation; academic honesty policy
- Significance of electronics packaging
  - Technology trends: device shrink
- Packaging functions; packaging levels
  - PWB trends