mounted to a circuit board using through-hole technology the same way that an axial lead resistor is mounted to a board. The only difference is that the diode has a polarity and must be inserted in the correct direction for the circuit to function properly. The diodes housed in surface mounted packages are also fastened to the board using the same solder reflow operations as other leaded chip carriers.

Diodes used in power supplies to rectify ac voltages are packaged in a wide assortment of housings. As the lead count is very low, the emphasis in packaging the diode is on dissipating large amounts of heat from the device to the heat sink with a small thermal penalty. Most of these power diode packages have a base or a flange which can be fastened directly to a heat sink to minimize the thermal resistance of the diode package.

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EXERCISES

4.1 What is a chip carrier and what purposes does it serve?

4.2 What are the two main approaches in the design of chip carriers?

4.3 Describe the three different types of surface mount chip carriers.

4.4 Prepare a sketch showing the arrangement of components in a DIP type chip carrier.

4.5 Prepare a sketch showing the arrangement of components in a ball-grid-array. What assumption did you make in preparing this sketch?

4.6 Ceramic chip carriers are very expensive. Why are they used when plastic chip carriers are much less costly?

4.7 Describe the general features of through-hole technology.

4.8 Describe the general features of surface mount technology with leaded chip carriers.

4.9 Describe the general features of surface mount technology with leadless chip carriers.

4.10 Describe the general features of surface mount technology with ball-grid-array packaging.

4.11 Describe the general features of direct chip attachment considering both wire bonding and flip chip connections.

4.12 What are the advantages and disadvantages of the DIP family of chip carriers?

4.13 Determine the area efficiency of a DIP which is used to house a chip which is 4 by 6 mm in size. Consider the number of pins on the DIP to be an open variable and graph the area efficiency as a function of I/O count.

4.14 What are some variants in the design of DIPs?

4.15 What is a SIP and what devices are housed in this package?

4.16 What is a ZIP? How does it differ from a SIP?

4.17 How is the pin-grid-array related to the DIP? Why do some designers specify the pin-grid-array in the design of new product?

4.18 Develop an equation showing the area of a pin-grid-array as a function of pin count. Assume the chip size is 12 × 12 mm and that pins are not placed under the chip cavity. Consider a square array on 100 mil (2.54 mm) centers. Also consider as a second case a staggered pin arrangement with the same pitch. Prepare a graph showing this relation.

4.19 What are some variants in the design of pin-grid-arrays?

4.20 Describe the two materials used to fabricate the substrates for pin-grid-arrays.

4.21 Describe the two techniques used with pin-grid-arrays for enhancing it heat dissipation capably.

4.22 What is a socket and why is it used to support pin-grid-arrays?

4.23 What is the oldest type of chip carrier and why is it still in use after more than 50 years?

4.24 Describe the advantages and disadvantages of surface mounted chip carriers relative to the DIP.

4.25 Prepare a list of the various types of surface mounted chip carriers.

4.26 Describe the purpose of the solder balls located at the center of the BGA illustrated in Fig. 4.19.

4.27 Describe the general characteristics of discrete device packages.

4.28 Go to the Internet and find a supplier of plastic quad flat packs (PQFP). Describe their product line. Are drawings of the package footprint available to aid you in the subsequent design of the printed circuit board?

4.29 Describe the general features of a SOIC type chip carrier

4.30 Describe the general features of a J leaded chip carrier. Why is this package limited to a lead pitch of 50 mil (1.27 mm)?

4.31 Write an equation describing the area of a J leaded chip carrier as a function of I/O count and prepare a graph showing this relation.

4.32 Describe the general features of a leadless chip carrier. What are the two most important disadvantages of this type of chip carrier?

4.33 Describe the general features of a thin-small-outline-package (TSOP). What type of devices is it used to house? In what type of product is it found?

4.34 The ball-grid-array is a relatively new chip carrier design. Describe its general features.

4.35 What are the principle advantages of the ball-grid-array? What are its disadvantages?

4.36 Write an equation describing the area of a ball-grid-array as a function of I/O count and prepare a graph showing this relation.

4.37 Sketch the features on a ball-grid-array that enhances its heat transfer capability.

4.38 What is the purpose of the column grid array illustrated in Fig. 4.33? Explain why the columns are more resistant to thermal fatigue that the typical solder ball found on a BGA.

4.39 Describe the difference between chip scale packaging and ball-grid-arrays.

4.40 Cite the primary applications of CSP.

4.41 Prepare a sketch of a CSP using flip-chip connections. Include in the sketch the connections to the PCB.

4.42 What is a multi-chip module? What are its advantages? When is it used?

4.43 Describe the features of the IBM's TCMCM.

4.44 Why are multi-chip modules still in use today when chips can be design with a complete system on a single chip?

4.45 What is meant by die stacking and why is this practice employed?

4.46 Cite the advantages and disadvantageous of ceramic chip carriers.

4.47 Describe the method of producing multi-layer ceramic substrates using the co-fired process.

4.48 Describe the process of solder bumping on a chip so that it may be bonded directly to a printed circuit board.

4.49 How is the mismatch between the temperature coefficient of expansion of the chip and the printed circuit board managed for wire bonding applications?

4.50 How is the mismatch between the temperature coefficient of expansion of the chip and the printed circuit board managed for flip-chip applications?

4.51 Describe the process for bonding the chip to a ceramic substrate.

4.52 What is eutectic solder? Why is it important to consider eutectic solder in many manufacturing processes?

4.53 Would you consider the gold-tin eutectic as a replacement solder for the gold-silicon eutectic? Why?

4.54 Describe the process of bonding the chip to the frame of a leaded chip carrier.

4.55 Discuss the engineering trade-off between using an epoxy adhesive and a thermoplastic for bonding a chip to a lead frame.

4.56 In what applications is polyimide used as an adhesive for bonding chips to lead frames?

4.57 Why are the thermosetting adhesives filled when used in chip bonding processes? What is a common filler material?

4.58 Describe the physical properties of materials used to fabricate lead frames.

4.59 The physical properties of three alloys used for lead frames are given in Table 4.1. Copper alloy MF 202 is less expensive and has better heat transfer characteristics than the other two alloys (Alloy 42 and Kovar). Why are the other alloys used in some designs?

4.60 Describe the automated wire bonding process for gold wire.

4.61 Write an equation for the number of wire bonding pads which can be placed about the perimeter of a chip. Prepare a graph of the I/O count as a function of perimeter length for three different pad sizes and spacings.

4.62 How does the automated wire bonding process change when aluminum wire is used to replace gold wire.

4.63 Is it possible to use copper instead of gold or aluminum in wire bonding? Cite the advantages and disadvantage of wire bond with copper.

4.64 Calculate the cost of the gold used in the bonding wires for a 100 pin chip carrier. Take the cost of gold wire at $500 per troy ounce. Consider at least two common wire diameters. Comment on the cost trade-off between gold and aluminum bonding wires.

4.65 Describe the tape automated wire process for making connections between the chip and the chip carrier.

4.66 Cite the advantages and disadvantages of the TAB process.

4.67 Describe the process for producing solder bumps on chips that are to be connected using flip-chip technology.

4.68 Cite the advantages and disadvantages of the flip-chip process process.

4.69 How is it possible to use flip chip technology with organic substrates which exhibit a much higher temperature coefficient of expansion than a silicon chip?

4.70 What is the purpose of an interposer?

4.71 Sketch the design of a chip carrier with a rigid interposer using flip-chip connections. Include the PCB in this sketch.

4.72 Sketch the design of a chip carrier with a flexible interposer that uses a flexible circuit for making the required connections between the chip and the PCB.

4.73 Sketch the features of a interposer manufactured at the wafer. Cite the advantages of this process and indicate why it may become the dominate process for producing CSP in the future.

4.74 Describe the process and the materials used to encapsulate chips and their connections with plastic.

4.75 Why is important to carefully package bare dies for shipment from one facility to another? Describe three of the methods for shipping individual dies.

4.76 Describe two methods for shipping wafers after they have been processes but before the chips have been cut from the wafer.

4.77 Examine a circuit board from an available PC and identify the passive components such as the capacitors and resistors. Describe some features of the board and the first level packages worth noting as design techniques.

4.78 Describe at least four through-hole packages for resistors.

4.79 Why would a design use a zero ohm resistor?

4.80 Resistors can be housed in leadless carriers without concern for solder joint failures due to cyclic thermal fatigue. Why?

4.81 Reference the power resistor shown in Fig. 4.65j. Where will this resistor be mounted. Cite the reasons for your answer.

4.82 Is it necessary to derate resistors when they are required to operate at elevated temperatures? Why?

4.83 Is self heating a consideration in derating a resistor? Why?

4.84 Explain why it was not necessary to consider self heating in the discussion pertaining to the packaging of capacitors. Consider capacitors in both ac and dc circuits in the explanation.

4.85 There are four types of capacitors. Describe the criteria for selection of the type used in a specific design.

4.86 What are the characteristics of a diode that is important in the selection of a first level package?

4.87 Prepare a caption for the figure shown in Fig. Ex4.87.

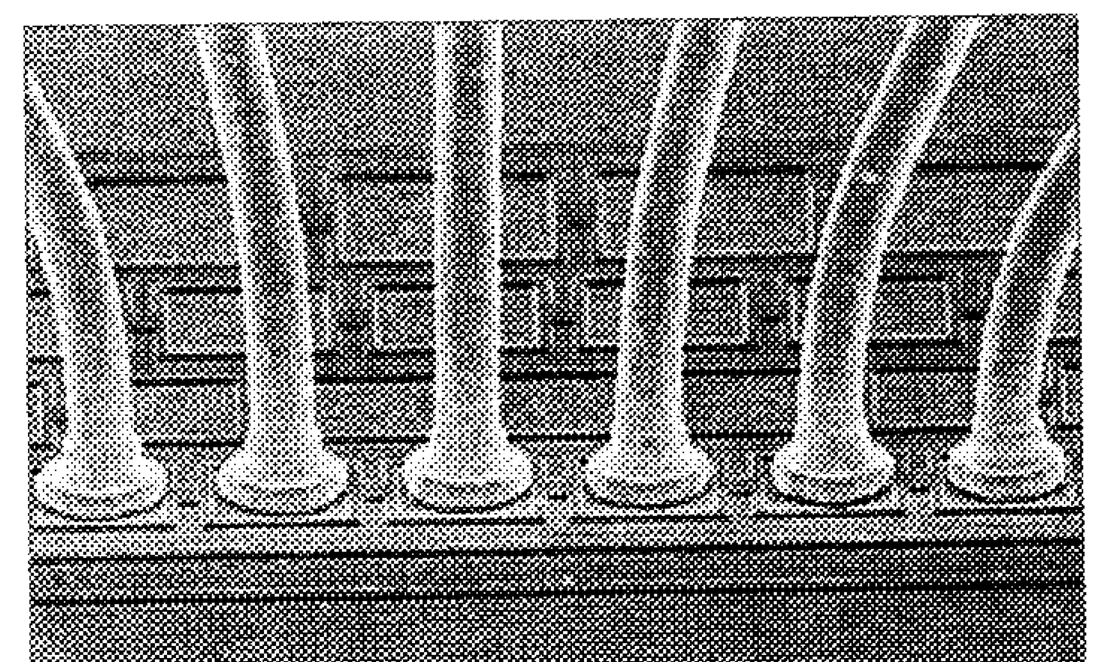

Fig. Ex4.87