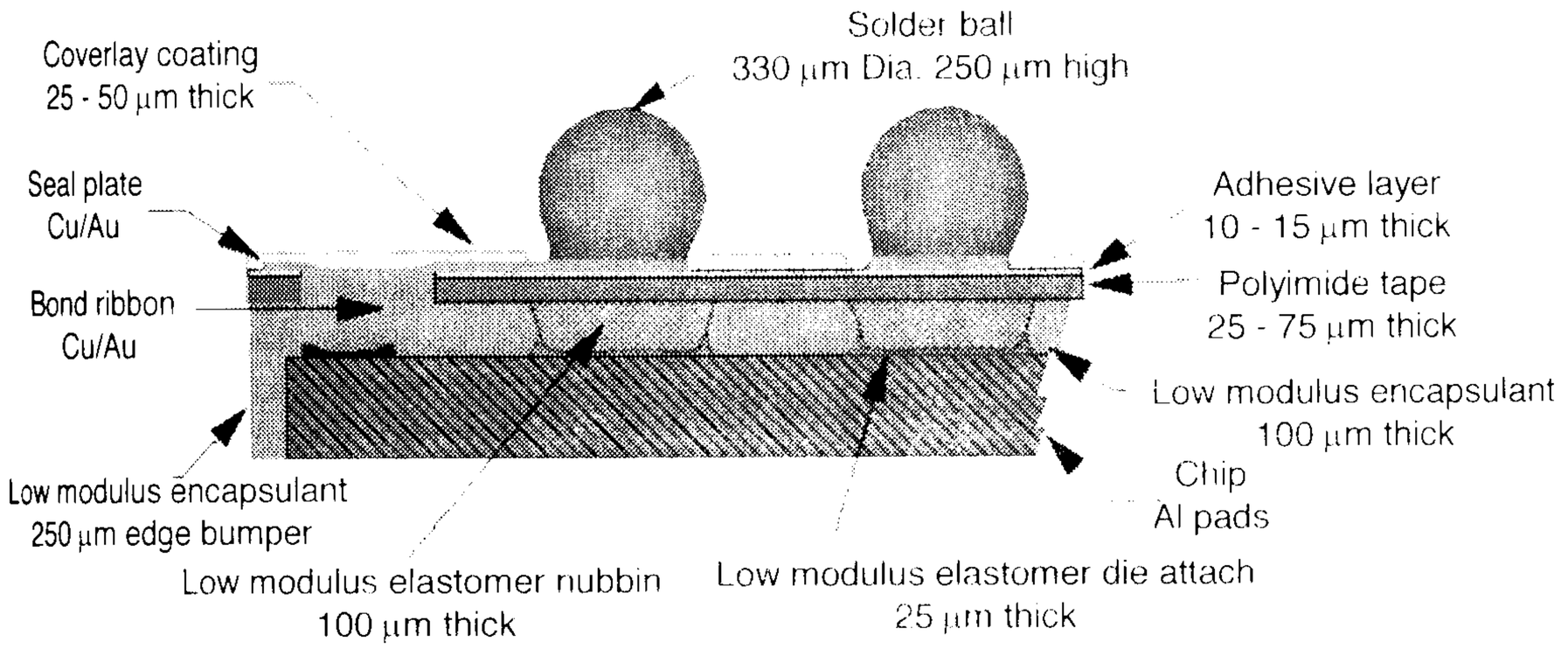


Fig. 4.58. Construction details of a molded flexible interposer.

Wafer Level Assembly

Some manufacturers are producing CSP using a process known as wafer level assembly. In this type of CSP, a chip is processed and assembled on the wafer before it is diced to form a single chip. A thin-film metallization process is used to place conducting lines that extended into the normal wafer scribe areas to redistribute the chip bond pads to a standard grid array footprint. The redistribution of IC interconnections to create other pad configurations allows the integrated circuit to be converted to a CSP. A diagram showing the detail of the transformation from an IC pad to a solder bump on a CSP is presented in Fig. 4.59. Note that polyimide dielectric polymer layers are used to isolate redistribution routings and to cover the entire area of the chip face in redistributing the I/O.

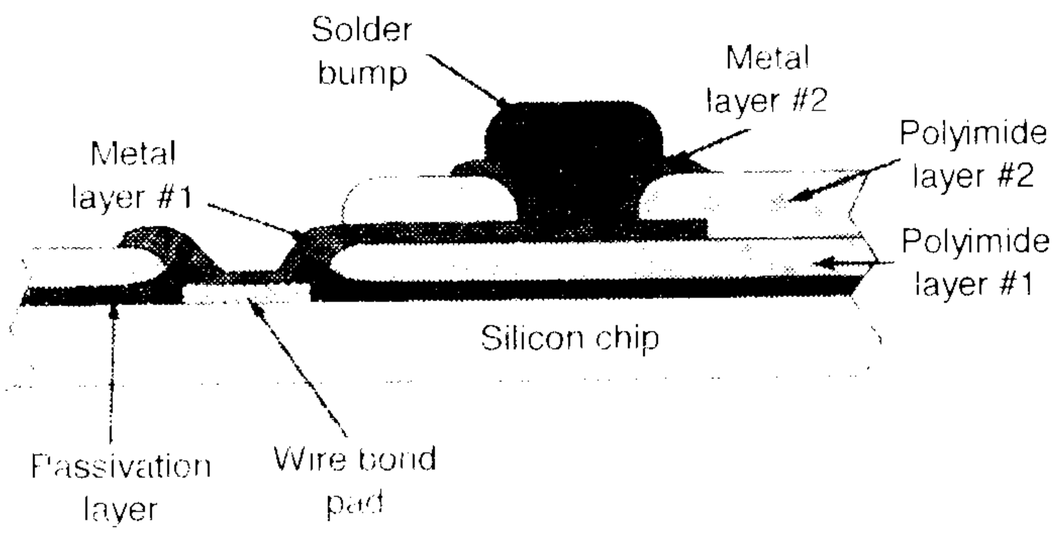


Fig. 4.59 Section view of a CSP solder bump produced on the wafer before dicing.

4.3.4 Molding

Plastic encapsulation of microelectronic devices is preferred because of costs. Plastic compounds are used to encapsulate chip on board, first level packages and as underfill and encapsulation of flip-chip assemblies. In this discussion, we will deal with those plastic materials used to encapsulation first level chip carriers. The primary purpose of the plastic chip carrier is the same as with the ceramic packages—to provide environmental and mechanical protection of the microelectronic device.

Environmental protection has been a concern because of the ability of water to diffuse through the plastic and causing corrosion of the aluminum pads and chip metals. This problem has been mitigated by formulating relatively pure encapsulating polymers with low ionic content. The mechanical protection is provided by employing polymers with a relatively high modulus of elasticity (rigid).

Thermo-mechanical stresses arise because of the mismatch in the coefficient of thermal expansion between the silicon chip and the polymeric encapsulant. Temperature changes that occur during start-up and shut-down cause thermal stresses that can result in chip cracking, encapsulant cracking, wire bond failures, passivation cracking, etc. The polymers are filled with silica to reduce the coefficient of thermal expansion from about 60 to 80 $\times$ 10^{-6} /°C to 14 to 24 $\times$ 10^{-6}/°C alleviating many of these failure problems.

The earliest materials used for encapsulation were silicones because of their high-temperature performance and high purity. However, silicones are costly and bisphenol-A (BPA) epoxies were introduced to lower costs. The BPA epoxies were replaced with phenolic novolac epoxies because of their higher functionality, higher cross-linking and increased glass transition temperature T_g. However, epoxies can have high ionic impurity levels because their reaction chemistry uses an excess of halogen-containing epichlorohydrin. In recent years, polymer suppliers have developed high-purity phenolic novolac epoxies that contain less than 25 ppm of hydrolyzeable chlorine.

The hardener that is added to the base epoxy contains the functional groups that chemically react with the epoxy molecule to produce the highly cross-linked molecules that form the polymeric encapsulants. The epoxy resin and hardeners are mixed with fillers and other additives then the composition is partially cured (B staged). This B staged compound is solid and can be ground into powder, formed into pellets and stored until it is ready to use. Because the epoxy resin and its hardener are reactive, the pellets are stored at low temperatures to prolong their shelf life.

The filler material, usually fused silica, serves to reinforce the epoxy enhancing its strength. To improve bonding between epoxy and silica, epoxy silanes and amino silanes are used as coupling agents. The addition of the silica (65 to 70% by weight) reduces the coefficient of thermal expansion and increases its resistance to thermal stresses. The added silica also increases the thermal conductivity of the polymer to 0.6 – 2.0 W/(m-°C) thereby improving the ability to dissipate heat through the encapsulant. Other additives include elastomeric modifiers to improve the epoxy's toughness and carbon black for its coloring. The filler also increases the modulus of elasticity of the encapsulant that is a disadvantage. A higher modulus for the encapsulant increases its ability to transfer stresses to the chip, passivation layer and the wire bonds.

The chips are encapsulated using injection molding. A controlled quantity of B-staged pellets is heated until the polymer becomes fluid. A hydraulic ram then drives the resin into a split mold as shown in Fig. 4.60. The lead frame, chip and bonding wires are in place before the mold is closed. Heaters are provided in both sides of the mold to maintain the temperature of the compound as it fills the cavities. The encapsulant is held at temperature in the molds until it is cured (C staged).

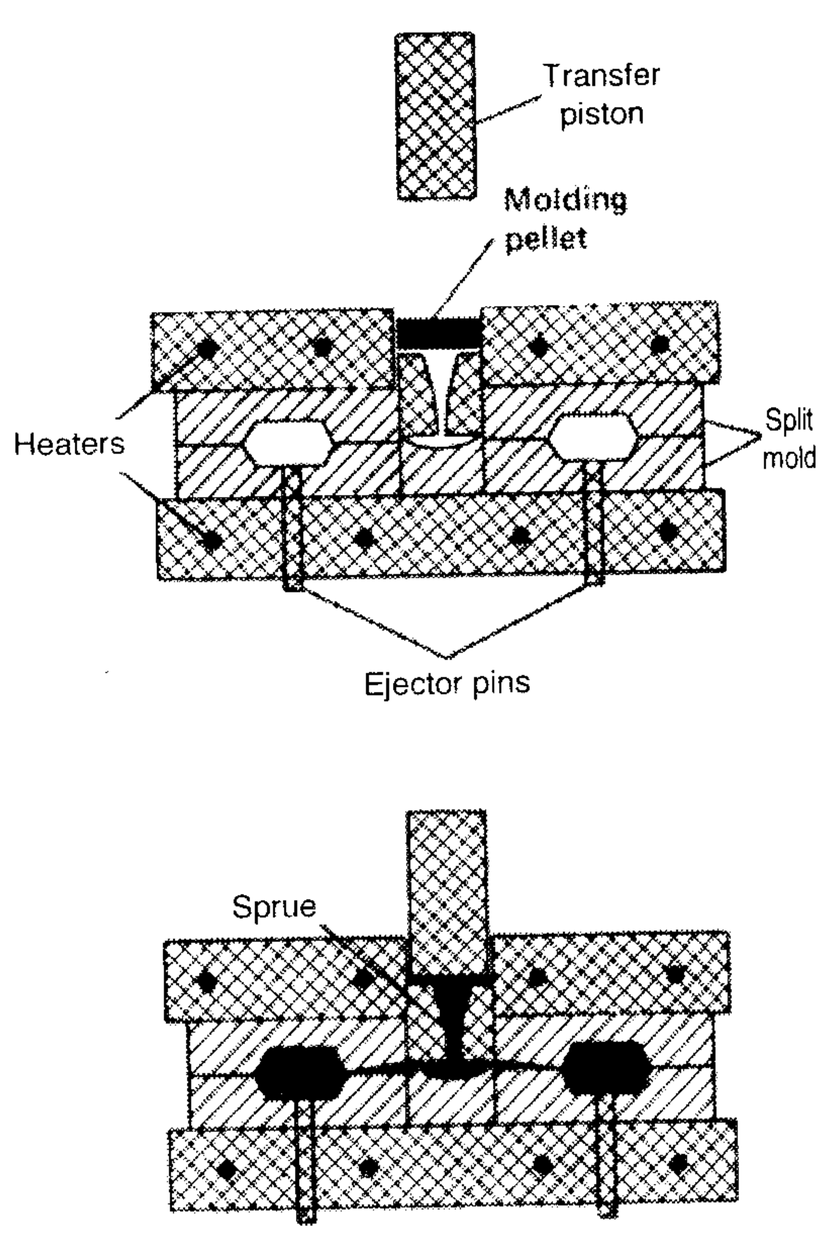


Fig. 4.60 Injection molding plastic encapsulated chips.

After the curing process is complete, cold water is circulated in the mold to cool the encapsulated chips. The die is opened and ejector pins are engaged to push the product from the lower mold. The flashing and sprue are cut from the molded chip carriers to complete the injection molding process.

The properties of molding compound used for encapsulating chips are presented in Table 4.2.

Table 4.2
Properties of an encapsulating molding compound

Property	Units	Molding Compound
Density	g/cm^3	1.9
Modulus of Elasticity	GPa	15-20
Tensile Strength	MPa	95-150
Thermal Conductivity	W/(m-°C)	0.7-0.9
Glass Transition Temperature	°C	180-225
Coefficient of Thermal Expansion	ppm/°C	α_1 = 12-18
		α_2 = 41-65
Volume Resistivity	Ω-cm	$>10^{16}$

4.3.5 Transport Packing

Safe transportation of the bare die is important to maintain overall quality and ensure higher yields when they are assembled into a product. It is essential to select the appropriate transport carrier for the bare dies. There are a number of different methods used for transporting chips from one location to another prior to their encapsulation (and protection) in a first level package. These include Waffle Pack, Gel-Pak, Tape and Reel, Wafer Jar or Vial, Wafer Cassette. The transport carrier is designed to move individual dies or complete wafers from one location to another without incurring damage, maintaining clean room cleanliness levels and retaining position and orientation so that the dies can be acquired with pick and place robots. Also important is prevention of damage due to electro static discharge (ESD) during transport and subsequent storage. Finally, protection must be provided to prevent corrosion of the sub micron size features on the chip during extended storage periods. Illustrations showing the essential features of each of these transport methods will be presented below:

Waffle Pack

Waffle packs have been the traditional carrier for dies that have been cut from their wafer, especially those that has not been functionally tested. The waffle pack, shown in Fig. 4.61, is made of conductive polypropylene that provides the grounding needed to avoid electrostatic discharge. It is available in either 2 × 2 or 4 × 4 inch sizes. Indented pockets are formed in an array across the tray for housing each chip. The number of pockets per waffle pack varies depending on the die size. A chip is placed in each pocket with its orientated consistent with all other chips in the tray. A sheet of lint-free glassine paper is placed over the array of chips, and then another waffle tray is stacked on top. Several waffle packs are uniformly stacked and locked in place. Several of these stacks of waffle packs are sealed in a dry pack bag for extra cushioning protection during shipment. A humidity indicator card and a desiccant are included in the bag when it is packed under vacuum.

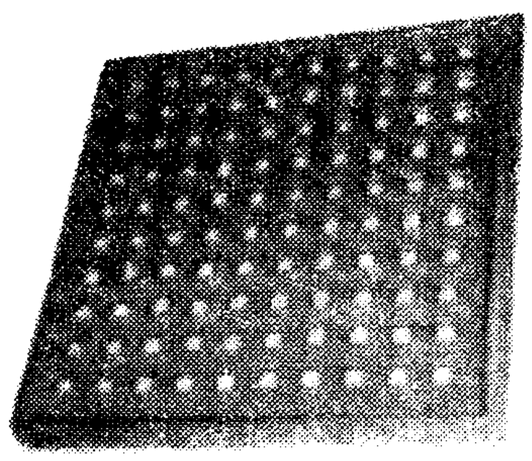


Fig. 4.61 A waffle pack holds an array of chips in a rectangular array of pockets formed in a conducting polymer tray.

Gel-Pak

In a Gel-Pak, the chips are arranged in a rectangular array in a manner similar to that used for the waffle pack except for the absence of pockets. The Gel-Pak is essentially a flat tray that has a non-adhesive but tacky membrane over which the chips are arranged. This tacky membrane minimizes movement of the chips in transport. The trays are available in 2 × 2 and 4 × 4 inch sizes. They are vacuum packed in a foil bag that provides protection from ESD and from the corrosive effects of the environment. A photograph of a Gel Pak holding a large number of small chips is presented in Fig. 4.62.

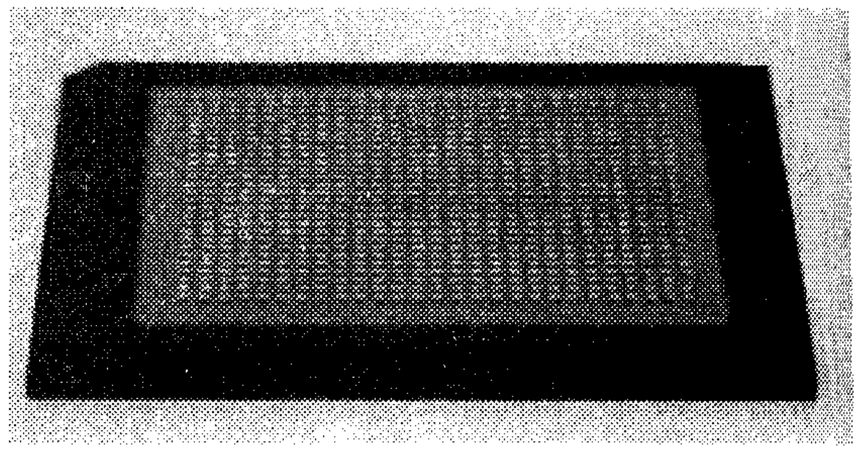


Fig. 4.62 A Gel-Pak supports a large number of chips on a tacky membrane during transport.

Surf Tape and Reel

The surf tape and reel carrier[9], shown in Fig. 4.63, is designed for shipping large numbers of chips in a format compatible with a high-volume, automated board assembly operation. The tape and reel is preferred over waffle packs because it eliminates movement of the die during shipment, reducing the risk of damage. In addition, many different chip sizes can be accommodated with only a few standard tape sizes.

The design for surf tape and reel is similar to the standard tape and reel carriers that are commonly employed for conventional surface-mount packages. The system consists of a surf tape wrapped on a standard 7 in. (178 mm) diameter reel. Two sizes of surf tape, which fit on the same standard reel, are available to accommodate a wide range of chip sizes.

The surf tape, shown in Fig. 4.63, consists of a conductive, polystyrene tape with rectangular depressions formed in the tape to provide a slightly recessed pocket for each chip. Two strips of sticky tape are applied along the edges of the window. This tape has a pressure-sensitive adhesive coating that holds each chip in place eliminating the risk of damage to the chips due to movement during transit. The sticky tape allows for easy and safe removal of each chip by the pick-and-place robot. Each chip is loaded into the surf tape with its topside exposed and chip orientation is consistent throughout the tape. Because the pockets are recessed, each chip is protected from exposure by the next layer of surf tape. The tape is indexed into the pick and place robot using the sprocket holes to advance the tape for each placement cycle.

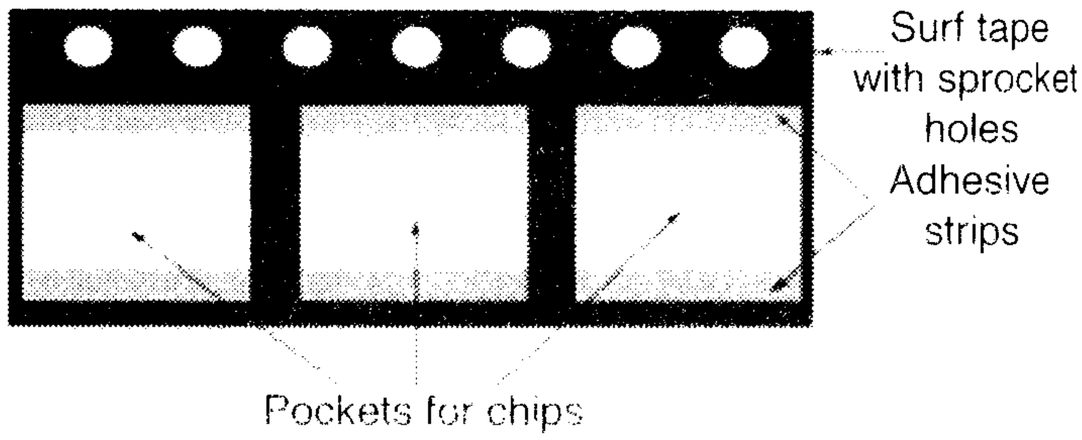


Fig. 4.63 Surf tape used to transport chips in a format suitable for high speed assembly operations.

[9] The surf tape and reel system and the tape and reel system are so similar that only the surf tape and reel system is described here.

Wafer Jar or Vial

Wafer jars are the standard carrier for fabricated wafers that have not been functionally tested. The wafers are packed in a wafer jar that is made of conductive polypropylene. A piece of antistatic, polyurethane foam is placed on the bottom of the jar to cushion any impact that might occur during transit. The wafers are stacked in the jar with a piece of lint-free filter paper between each wafer. Another layer of foam is used to fill the jar. The jar lid is also fabricated conductive polypropylene.

Wafer Cassette

The wafer cassette is used to transport complete wafers in a boat-like-box. The boat is fitted with slots that accommodate the wafers as shown in Fig. 4.64. The slots are arranged to provide spaces between adjacent wafers. Both the top and the bottom of the boat are fabricated from conductive polypropylene to provide protection from ESD. The cassettes can hold up to 25 wafers with diameters of 200 and 300 mm. The boats are filled with an inert gas before they are sealed to protect the wafers from the environment.

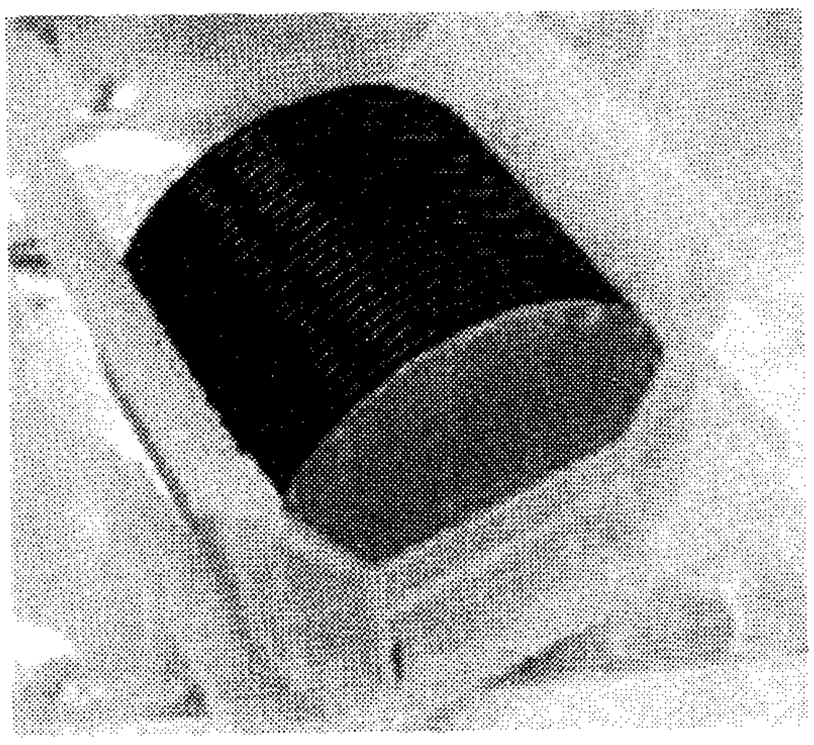


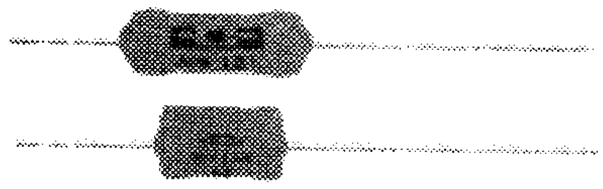
Fig. 4.64 Wafer cassette for transporting and storing wafers prior to dicing testing and assembly in chip carriers.

4.4 FIRST LEVEL PACKAGING FOR DISCRETE COMPONENTS

While the emphasis in this chapter has been on chip carriers, it should be recognized that first level packages are also important in protecting passive devices like resistors, capacitors and diodes. The packaging of these passive devices involves both through hole and surface mount. Because each of these components different to some degree with regard to their packaging, they will be covered individually.

4.4.1 Resistors

Resistors are available in a very wide assortment of package types as illustrated in Fig. 4.65. There are several reasons for the lack of standardization in the types of packages employed. Firstly, the range of product where resistors are employed is quite large and the amount of power dissipated varies considerably. Secondly, the importance of circuit density changes significantly with the type of product. Next, the importance of resistor temperature differs markedly with the application. Finally, the assembly process used for the board may influence the choice of package. To avoid having to pass the board through another line to assemble the resistors, the package for the resistors often is selected to match the carrier for the chips.



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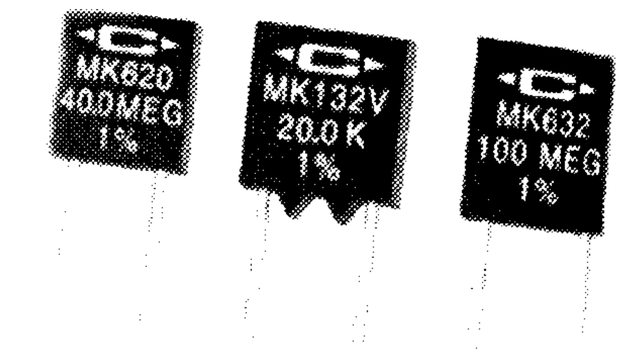

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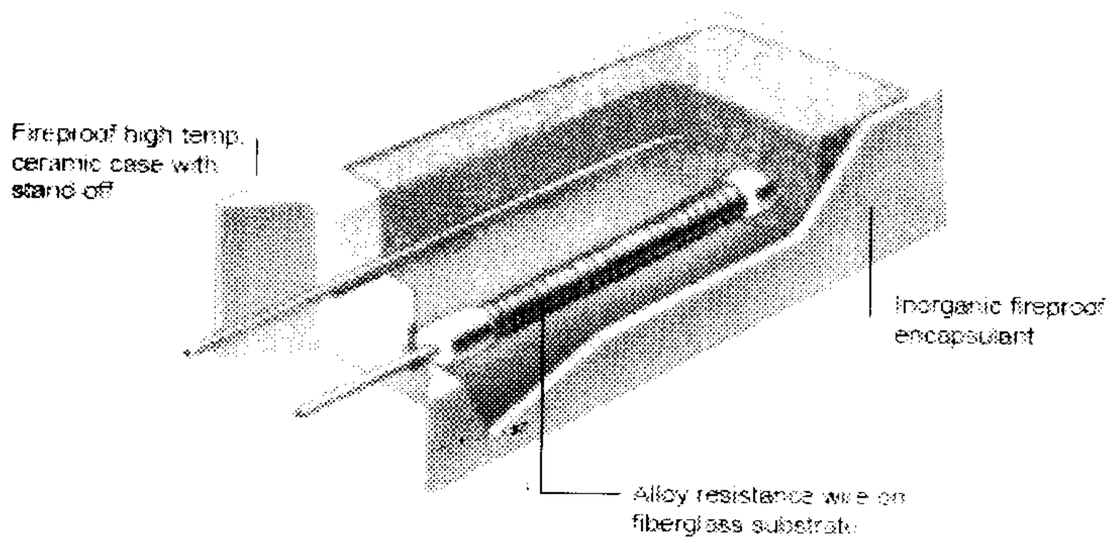

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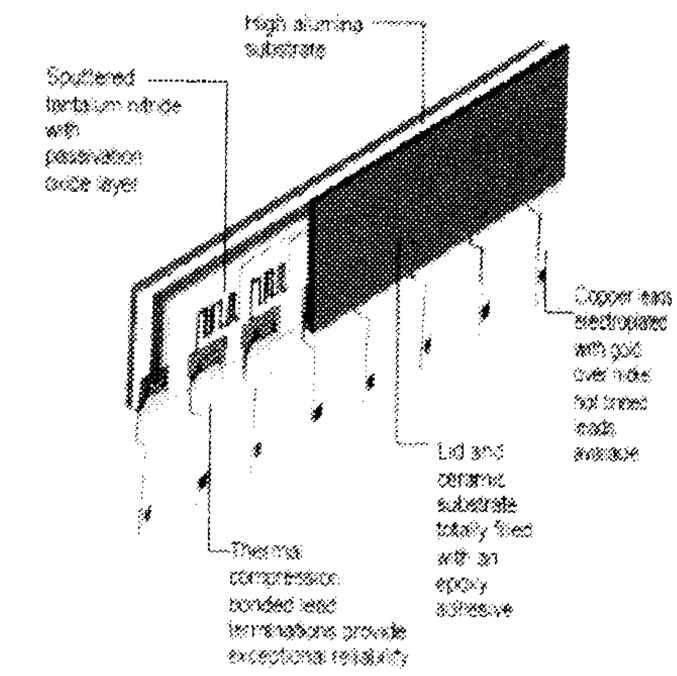

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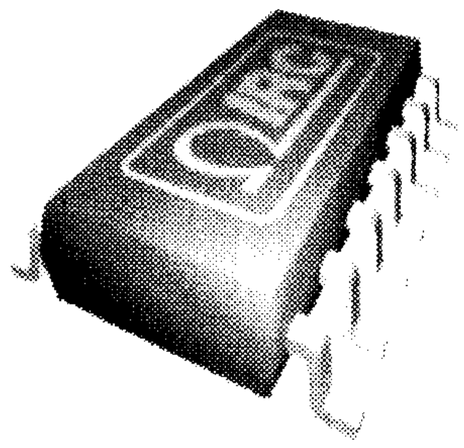

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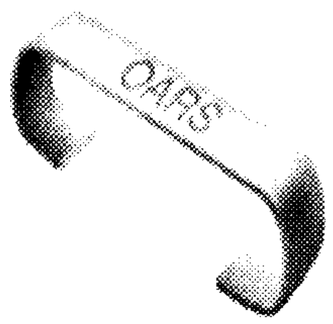

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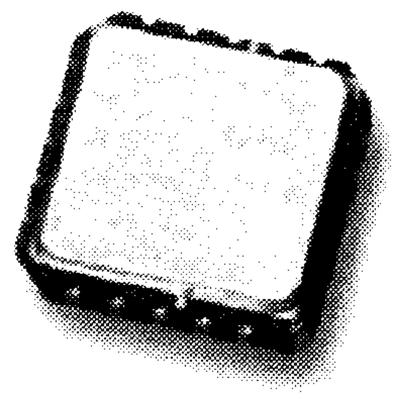

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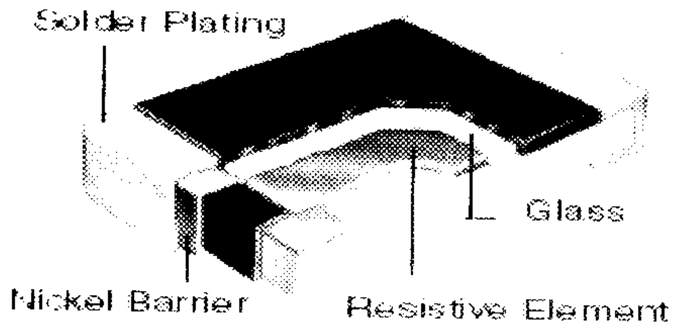

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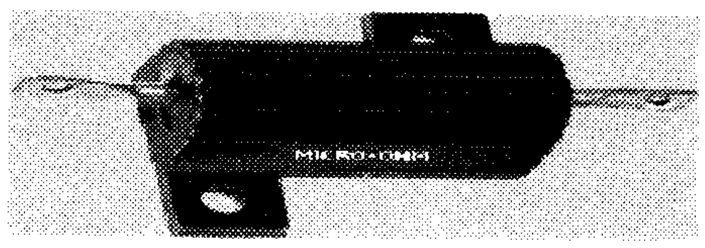

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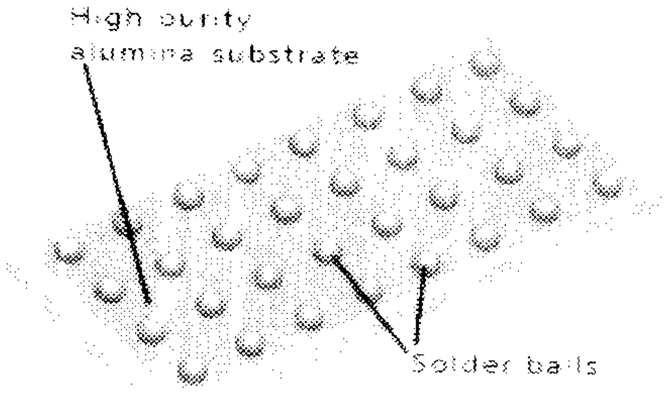

(i)

Fig. 4.65 Resistors are available in many different types of carriers. The examples shown in this figure represent some of the different carriers available.

A common resistor package is the axial lead type (See Fig. 4.65a) because it is easy to assemble into through-hole type circuit boards. The radial lead package shown in Fig. 4.65b utilizes less board space and dissipates heat better than the cylindrical axial leaded package. A power resistor with radial leads, shown in Fig. 4.65c, is encased in a ceramic case to withstand high temperatures. The SIP, shown in Fig. 4.65d, houses a resistor network. SIPs save board space and conform to assembly procedures involving boards containing only through-hole components. All of these resistor packages are the through-hole type and can be assembled with DIPs connected to the PCB's with a wave soldering process.

The SOIC carrier and the leadless packages, shown in Fig. 4.65e, f, g and h, are surface mounted carriers that are used to conform to the surface mount chip carriers, which house the IC's placed on the circuit board. The component, illustrated in Fig. 4.65f, is a zero ohm resistor that provides a method to connect one circuit to another. The leadless resistor shown in Fig. 4.65g is one of the most common surface mounted resistors in use today. It comes in a wide variety of sizes with all of the standard resistance values in use today. A network of resistors is housed in the leadless quad pack shown in Fig. 4.65h. Networks of resistors are also housed in ball-grid-array carriers as illustrated in Fig. 4.65i. The power resistor shown in Fig. 4.65j incorporates an aluminum heat sink. This heat sink is fabricated with fins to improve the amount of heat dissipation from the resistor.

Temperature plays an important role in the life and performance of resistors. The resistors are rated for specific power dissipation, and this rating is based on an ambient temperature T_a of 25 °C. If the resistors are used at a temperature higher than T_a, they must be derated (used at a power level lower than the rated value) to avoid early failures or a change in the value of their resistance with time. Typical derating curves for two types of resistors are shown in Fig. 4.66a and Fig. 4.66b.

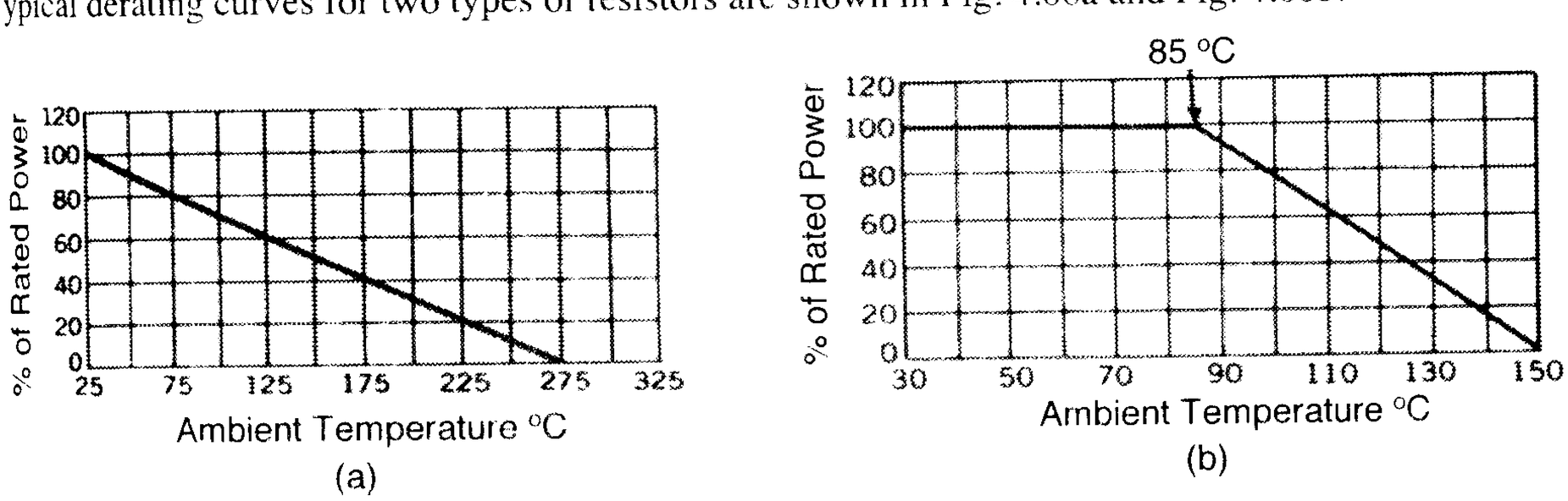

Fig. 4.66 Derating curves for two types of resistors. (a) Wire wound power resistor. (b) Precision thin film resistor.

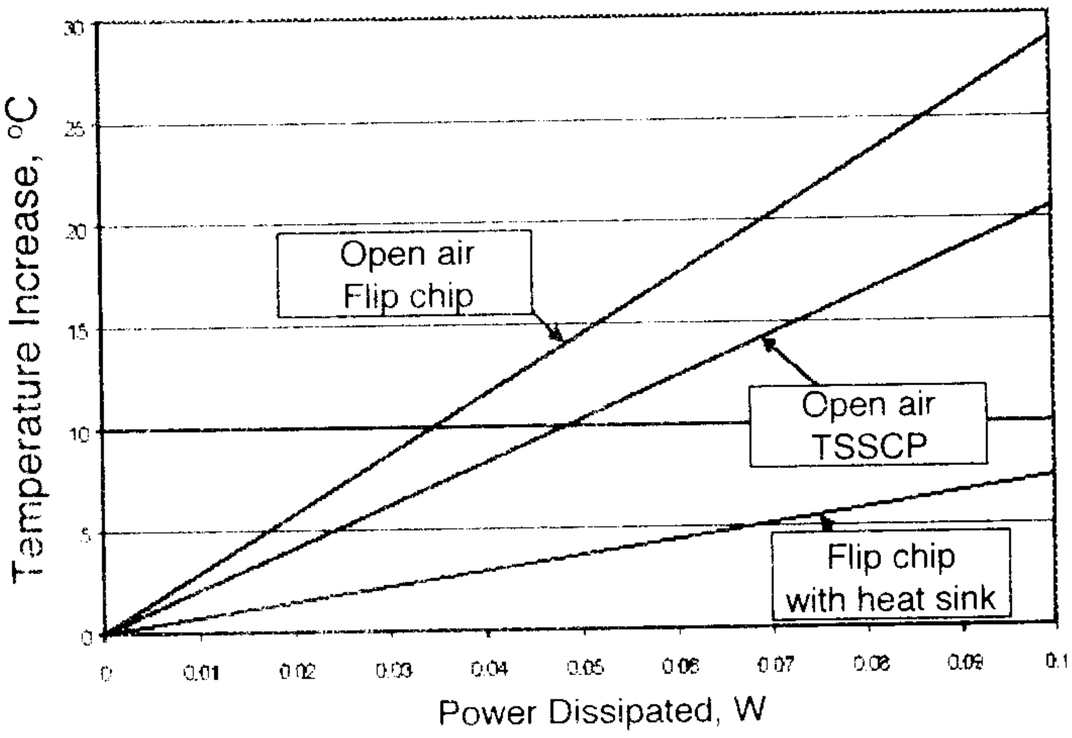

Fig. 4.67 Temperature increase due to self heating of resistors housed in flip chip packages.

Self heating must also be considered in determining the temperature of a resistor. As the power dissipated by a resistor increases, its temperature increases relative to the ambient temperature. The thermal resistance which controls the slope of the temperature-power relation is a function of the size of the resistor and the materials used in its construction. In this case, the resistors were packaged using flip chip technology with and without a heat sink. Significant temperature increases were noted with in the flip-chip package without the heat sink. Cylindrical resistors with axial leads also undergo appreciable increases in temperature in order to dissipate power. Often resistors are packaged in an epoxy case that is molded about the core to provide protection against moisture. It should be noted that the thermal resistance penalty associated with this type of encapsulation is quite high with values ranging from 135 to 95 °C/W. A more detailed description of thermal resistance and its effect on component temperature is presented in Chapter 9.

4.4.2 Capacitors

Capacitors like resistors are packaged in a wide variety of carriers that are usually selected to be consistent with the packaging of the other devices on the circuit board. The PCB usually provides support and wiring for the capacitor; however, in some instances the capacitor is too large and it must be mounted on the chassis. Capacitors are generally divided into four categories, namely aluminum electrolytic, tantalum, film and ceramic. The aluminum electrolytic utilizes aluminum foil as the conductor and aluminum oxide as the dielectric. Electrolytes used in aluminum electrolytic capacitors have near-neutral pH and no aggressive species that might attack aluminum or its oxide. Typical solvents include ethylene glycol, dimethylformamide and g-butyrolactone. Mixtures of these are often used. Common solutes include ammonium, quaternary ammonium, and tertiary amine for cations, and borate or dicarboxylate for anions. Some water is usually present in the electrolyte (1 to 3%) to support formation of the anodic aluminum oxide dielectric after capacitor assembly. Because the electrolyte is liquid, the capacitor is usually packaged in a sealed can as shown in Fig. 4.68a. Circuit board mounting, with the capacitor leads being inserted into plated through holes, is illustrated in Fig. 4.68b. Aluminum electrolytic capacitors are also available for surface mounting with pads at their base instead of pins.

The aluminum can is usually insulated by a vinyl chloride sleeve which also serves for marking the part number, capacitance, working voltage and polarity. The lead wires emerging from the can are a copper based alloy providing a material which can be soldered with conventional methods. An aluminum to copper weld is made inside the can because the lead emerging from the foil is aluminum. In connecting electrolytic capacitors to the PCB, it is important that polarity be established and confirmed. If the capacitor is used in reverse polarity, its life is reduced in the best of circumstances or the capacitor is destroyed in a worst case.

Tantalum capacitors are also of the electrolytic type and if the electrolyte is a liquid, the tantalum capacitor is sealed in a manner similar to that shown in Fig. 4.68. The advantage of using tantalum in place of aluminum is due to the dielectric constant of tantalum oxide ($\varepsilon = 11.6$) as compared to aluminum oxide ($\varepsilon = 4.5$). This property gives the tantalum capacitor a much higher capacitance at a given working voltage for a specified volume. Because capacitor size is extremely important, the tantalum capacitor has gained a large share of the capacitor market.

Film capacitors are fabricated from polymeric films either metallized directly or between layers of metallic foils. These capacitors utilize several different film materials including polyester, polycarbonate, polystyrene, polypropylene and paper. These capacitors have the advantage of very high reliability and an extended temperature range of operation -55 to 125 °C. However, for a specified capacitance, they are relative large in volume when compared to the electrolytic type capacitors describe previously.

Ceramic capacitors are available in single or multiple layers using materials such as titanium acid barium for the dielectric. Manufacturers of multilayer ceramic capacitors (MLCC) have increased the capacitance per unit volume of the ceramic carrier. In a multilayer capacitor, increased capacity is accomplished by increasing the number of electrodes, and by using thinner ceramic dielectric and electrode layers. The multilayer construction of a ceramic capacitor, presented in Fig. 4.69, shows the internal electrodes which are typically made from palladium or silver palladium alloys. One factor that complicates the effort to produce thinner electrodes is the trade off between metal electrode thickness and electrical performance. Thicker electrodes provide more continuous, higher conductivity paths for capacitor charging and discharging, but thicker electrodes also increase the cost of manufacturing due to the use of additional quantities of costly metals (silver/palladium).

Capacitors like resistors are affected detrimentally by increasing temperature. Increasing the operational temperature decreases life and decreases the maximum allowable working voltage.

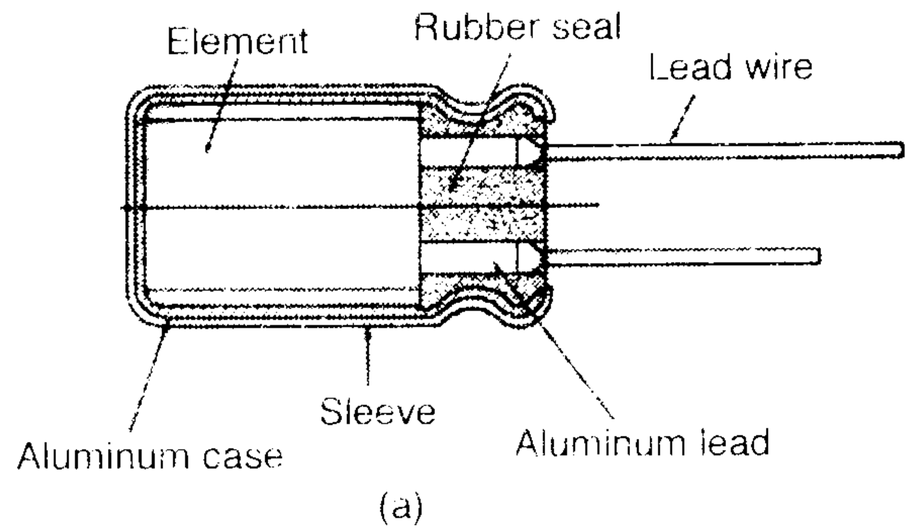

Fig. 4.68 (a) Construction details for an aluminum electrolytic capacitor. (b) Mounting methods for axial and radial leaded capacitors.

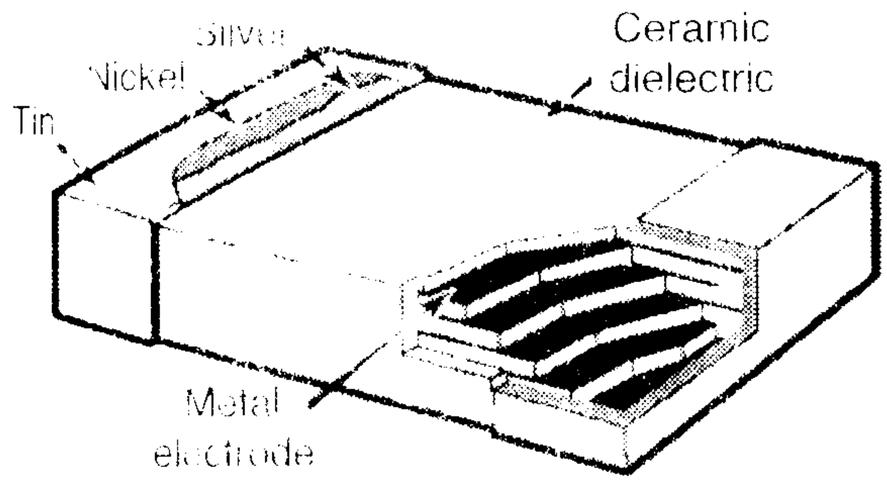

Fig. 4.69 A small high-capacity ceramic capacitor that is surface mounted on a printed circuit board.

4.4.3 Diodes

Packaging for diodes depends largely on their purpose. Signal diodes either pass or block signals representing low voltages and low currents. These diodes are housed either in small diameter glass or plastic cylinders with axial leads for through hole PCBs or in a variety of surface mounted packages. Surface mounted packages include two terminal leadless carriers, SOICs for diode arrays, two leaded L plastic encased carriers and even CSP with solder ball connections. The diodes with axial leads are