high joint strength, excellent resistance to corrosion and high thermal conductivity. Its reliability has been proven in for die-attach and for solder lid sealing in applications for over 30 years.

The bonding of the chip to plastic carriers is entirely different because hermeticity usually is not a major concern. Instead, the problem encountered is with the difference in the thermal coefficient of expansion (TCE) of the silicon chip and the plastic housing. The TCE of silicon is 4 PPM/°C and that of plastic about 80 PPM/°C. Bonding the chip directly to a plastic substrate would result in large thermal stresses induced in the chip due to temperature changes. This problem is circumvented by introducing a lead frame into the housing. The lead frame serves several purposes. Firstly, it is fabricated from an alloy which has a thermal coefficient of expansion much more closely matched to silicon. Second, it serves as a bonding surface. Third, it provides the I/O leads that fan-out from the package. Finally, the lead frame provides a surface to which the small bonding wires from the chip can be welded. A typical lead wire frame for a 40 lead DIP is shown in Fig. 4.48.

Properties of lead frame materials that are important include: density, modulus of elasticity, tensile strength, thermal conductivity and thermal coefficient of expansion (TCE). Physical properties of three common lead frame materials are presented in Table 4.1.

Adhesive die attach materials are suspensions of metal particles in a polymeric carrier. The particles are several μm in size, usually in the form of thin flakes of silver. The polymer provides adhesion and cohesion to make a bond with the adequate mechanical strength, while the metal particles provide electrical and thermal conductivity. Note that conductive resins are often used even though an electrical connection is not required, in order to enhance thermal performance. The polymer most commonly used is a solvent-free, high purity epoxy resin. Epoxy adhesives reduce costs, shorten cure cycle time and produce stress-free bonds. When selecting a particle filled epoxy it is important to specify a solvent-free product to reduce the formation of voids in the adhesive joint and to improve heat transfer across the bond line. Purity of the adhesive is also an important consideration. Aluminum corrosion failures of the bonds occur when hydrolysable ions react with water vapor to form organic acids. In more recent years, adhesives that contain lower and lower levels of hydrolysable ions, in particular chlorine, sodium and ammonium are specified for this application.

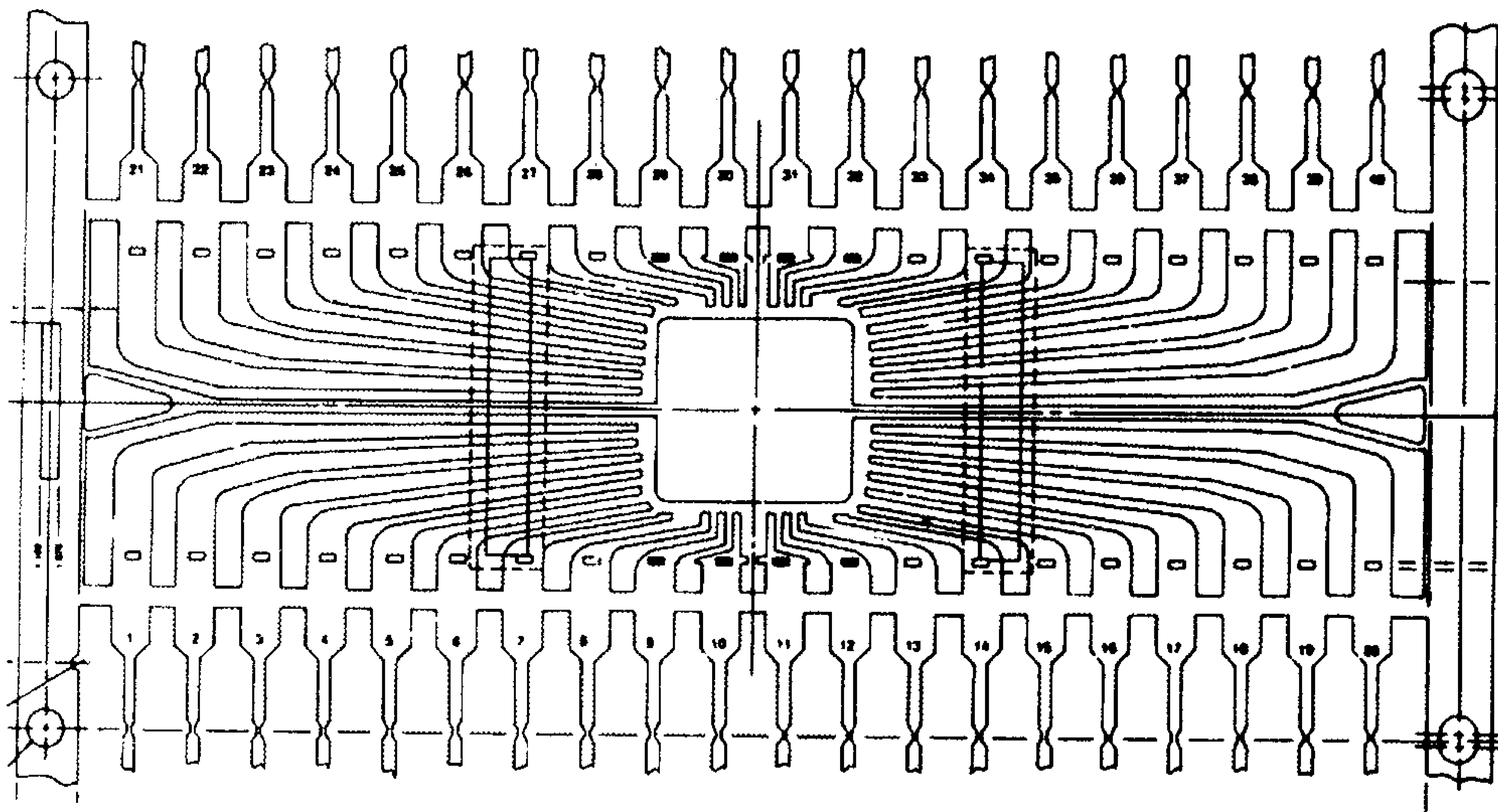

Fig. 4.48 A typical lead frame used for chip bonding in a 40 lead DIP.

Table 4.1
Physical properties of common lead frame materials

Properties	Units	Copper Alloy MF 202	Alloy 42	Kovar
Density	kg/m^3 (g/cc)	8880 (8.8)	8100 (8.1)	8400 (8.4)
Modulus of Elasticity	GPa	113	145	138
Tensile Strength	MPa	540	615	627
Thermal Conductivity	W/m°K	160	15.7	17.5
Coefficient of Thermal Expansion	ppm/°K	17.0	4.5	5.3

Polyimide die attach resins are specified when higher temperatures are involved in subsequent processes because they withstand higher temperatures than epoxies. Polyimide adhesives are thixotropic pastes containing approximately 70% silver powder in a polyimide resin that has been dissolved in a solvent with a high boiling point. To minimize the quantities of solvents and other vapors released during cure, the base polyimide used is a low molecular weight resin which is cure by an addition reaction. Although in use since the mid-1980s, the main objection to polyimide is the difficulty in removing all the organics that may outgas later in service, causing premature failure of the device.

Epoxies have extremely large molecules which are cross-linked in three dimensions to give relatively high-modulus polymers with good adhesion, low shrinkage and high-strength. This strength and rigidity, which was ideal when chips were much smaller, can cause problems when bonding large dies. The requirement for the adhesive to bond these large chips involves mechanically decoupling the larger die with a low TCE from a substrate with a higher TCE. To accomplish this decoupling requires a more flexible, lower-modulus adhesive. Thermoplastics are inherently lower-modulus adhesives because they are made from linear molecules that do not cross link. There are a number of commercially available filled thermoplastic adhesives suitable for die bonding that can be processed in the range from 200°C to 400°C.

The advantages of thermoplastic adhesives are presented below:

- They are supplied fully polymerized, which implies that their properties are determined by the manufacturer; hence, they are more consistent than thermoset polymers.
- Their shelf life is virtually unlimited even without refrigeration.
- The bonding process is simple, because it involves only heating and cooling the polymer after it is placed in contact with the surfaces to be bonded.
- The bonding time is extremely short (seconds), and the process is clean.
- The die can be reworked, disassembled or repositioned by reheating allowing defective chips to be removed and replaced.
- The polymer is used in a dry state, which significantly reduces the possibility of voids as compared with those thermoset adhesives that contain solvents.

The bonding mechanism for thermoplastic adhesives is primarily by mechanical interlocking and is more dependent on surface roughness than on material composition. At its glass transition temperature, the polymer changes to a rubbery state. Increasing the temperature further causes it to become semi-fluid. Bonding is achieved by applying pressure to force the semi-fluid polymer into the scratches and pits on the surface of the lead frame. Sufficient time under pressure is permitted for heat

to distribute at the bond line and for the polymer to penetrate the surface roughness. Cooling the assembly causes the polymer to solidify making a mechanical bond.

4.3.2 Chip to Chip Carrier Connections

The I/O from the chip consists of a number of bonding pads usually arranged in a straight line around the four edges edge of the chip. The bonding pads are very small, usually 40 to 50 μm square on 60 μm centers. On very dense chips, two staggered rows of bonding pads are placed around the chip's perimeter. When flip chip bonding is employed solder bumps are deployed over the area of the chip. In this case, the solder bumps are placed on pitches of about 150 μm. Connections are made between these bonding pads on the chip and the metal fingers on the lead frame for leaded chip carriers. For flip chip, the solder bumps are aligned with the pads on the chip carrier and connections are made by reflowing the solder bumps. Three different methods are used in making these connections which include: automatic wire bonding, tape automated bonding and flip-chip with solder bump reflow. Each of these methods will be described in the following subsections.

Automated Wire Bonding

Wire bonding is performed using either a thermo-compression or an ultrasonic bonding process. The wire materials are gold, aluminum and more recently copper. With thermo-compression bonding*, a gold ball is first formed by melting the end of the wire, which is held by a capillary bonding tool, with an electronic flame-off (EFO) procedure. The free-air ball, shown in Fig. 4.49a, has a diameter that is about twice the size of the wire diameter. The size of the free air ball size is controlled by the current employed in the EFO procedure and the tail length of the wire extending from the capillary tool.

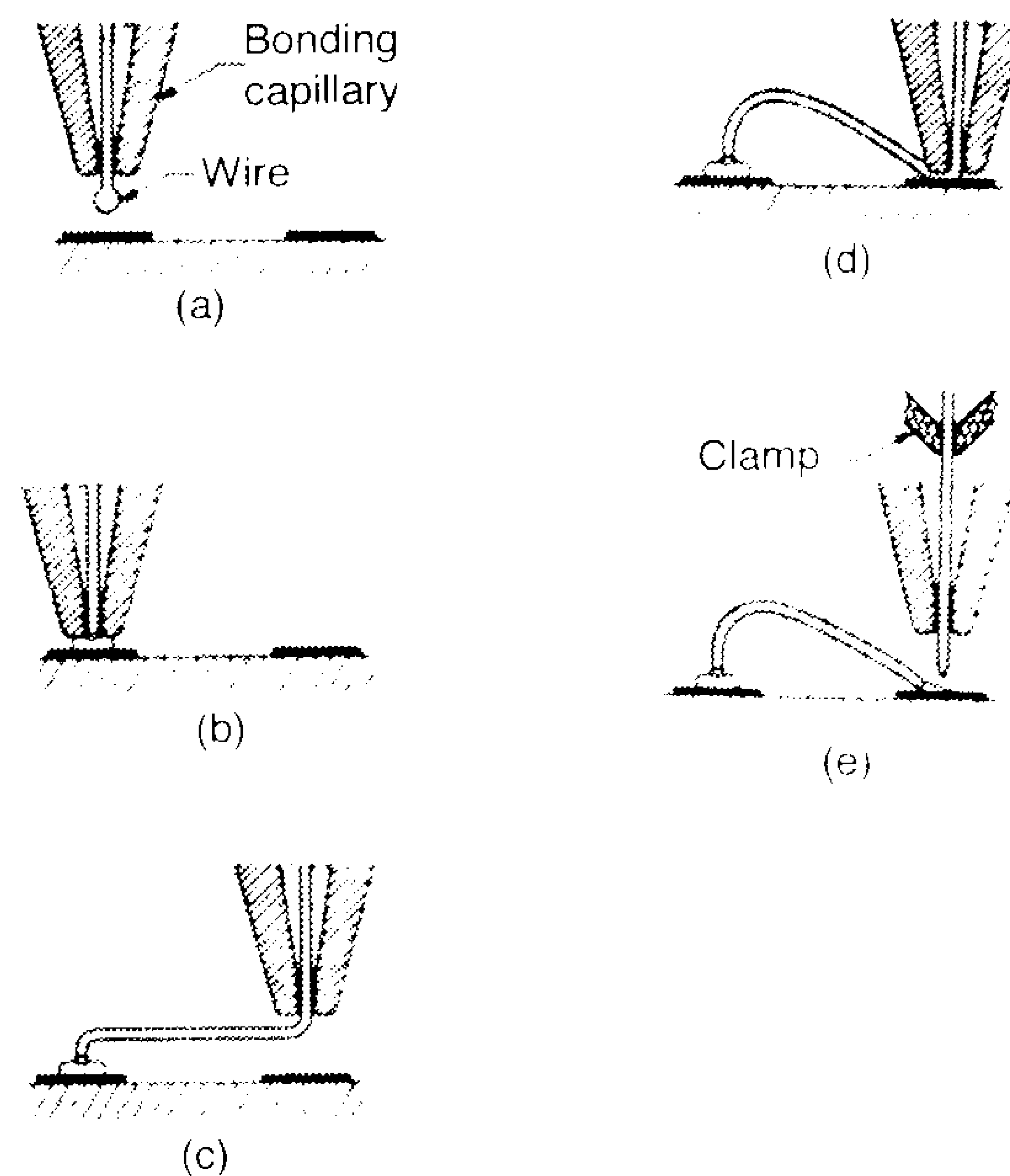

Fig. 4.49 Processing steps involved in producing ball-wedge joints with a thermal compression welding process.

*The thermal ultrasonic process is also employed where the metallurgical bond is made using heat, pressure and ultrasonic forces. In ultrasonic bonding, the wire is forced against the bonding pad with a head that is vibrated with a shearing motion at a frequency of about 60 kHz. The local slip of the wire produces intimate contact of the two materials and friction welding occurs producing the joint.

The free-air ball is then brought into contact with the bond pad. Pressure and heat are applied to the ball with the capillary tool for less than 0.1 second, as indicated in Fig. 4.49b, to form the metallurgical weld between the ball and the bond pad. The weld is formed by the diffusion of the atoms from the wire and pad materials into each other. The combination of temperature and pressure promotes diffusion producing a strong welded joint between the bonding wire and the pad. The shape of the end of the gold wire after attachment is illustrated in Fig. 4.50.

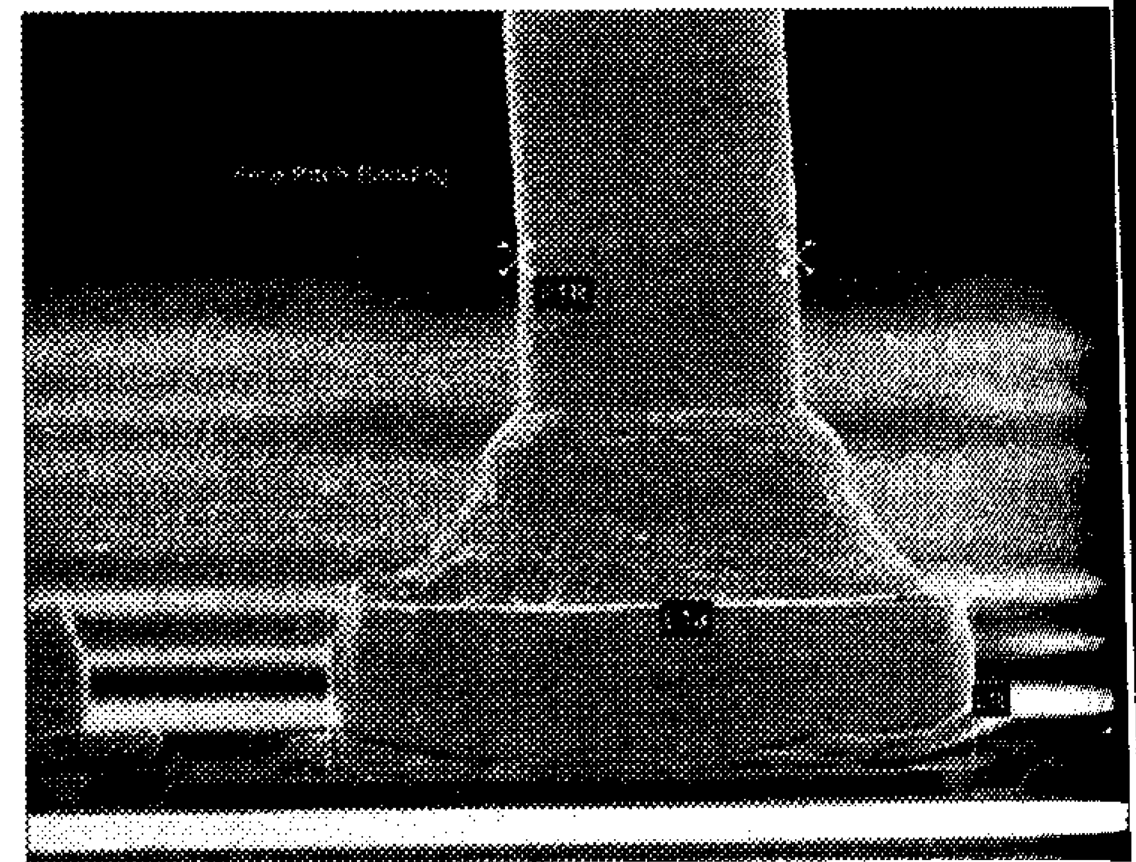

Fig. 4.50 Photomicrograph of a 20 μm diameter gold wire bonded to a chip pad.

After the ball is bonded to the die, the capillary pulls wire from the supply spool to free a sufficient length to make a connection to the lead frame of the chip carrier (see Fig. 4.49c). Then the capillary lays the wire down in a parabolic or elliptical curvature to form a loop between the chip and lead frame pads as shown in Fig. 4.49d. The looping profile is controlled by the wire bonder's software. Achieving low-loop, long lead bonding is not difficult because a programmable looping algorithm optimizes its formation for the different connection lengths. When the capillary reaches the second bond position, a wedge shaped bond is formed on the lead frame by applying heat and pressure with the capillary tube as shown in Fig. 4.49d.

A second wire-bonding process is aluminum wedge bonding. During this process, a clamped wire is brought in contact with the bond pad on the chip. Ultrasonic forces are applied to the wire for a less than 0.1 seconds while the capillary tool applies a compression force. A friction weld is produced between the wire and the bond pad. The wire is then extended to the specified bonding location on the lead frame, where the friction welding process is repeated. The wire is then broken off by clamping and pulling the wire until it fractures as illustrated in Fig. 4.49e. The result is a wedge weld that is illustrated in Fig. 4.51.

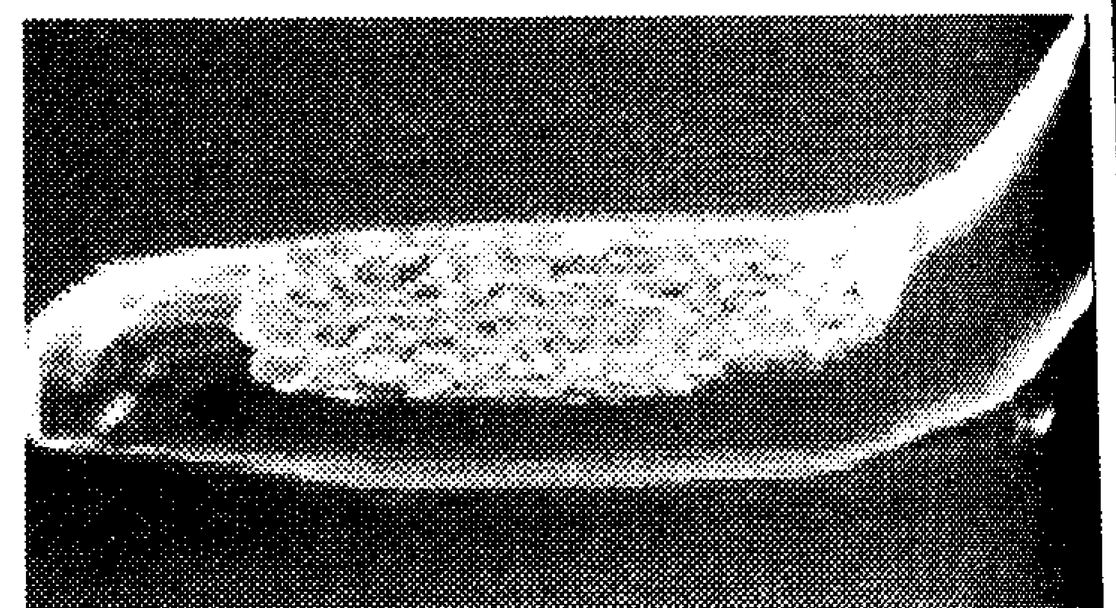

Fig. 4.51 A wedge weld with aluminum wire produced with an ultrasonic bonding process.

Gold ball bonding is faster than wedge bonding with about 18,000 welds per hour. The speed of the gold ball bonding is faster than the wedge bonding because the second bond can be formed about an angle about the arc of the ball bond. Rotation of the capillary tool is not necessary to form the second bond. In wedge bonding, the wire is fed under the bottom of the capillary tool. The second bond must therefore be in line with the first bond. To achieve alignment the capillary tool must be rotated. This added motion slows the process and as a consequence wedge bonding often takes longer to form the second weld than gold ball bonding.

Aluminum wedge bonding can be used with slightly smaller pitches than gold ball bonding because the size of bonding pad on the chip is only 25 to 30% larger than the diameter of the bonding wire. Because the deformation of the gold ball is larger, the bonding pad size must be 60 to 80% larger than the diameter of the gold wire. Aluminum wire is also used when higher temperatures are

required in subsequent manufacturing processes, because higher temperatures degrade the gold wire weld by producing intermetallics at the gold/aluminum joint.

The two most common metals used for the bonding wire are gold or aluminum with wire diameters varying from about 20 to 50 μm depending on the pitch of the bonding pads on the chip. Aluminum is used primarily in making wedge type joints with ultrasonic bonding on chips with very small bonding pad pitch (< 45 μm). Gold is easily bonded, using the ball-wedge method illustrated in Fig. 4.49. The ductile properties of gold aid in the welding process and high production rates can be achieved. Also, the gold is a noble metal and resists corrosion that can occur with plastic chip carriers.

Copper has been introduced as a bonding wire in recent years. Copper is more economical than gold, has superior electrical properties and is more compatible with copper metallization on chips. Because copper metallization results in significant reductions in the power dissipated by logic chips, its usage has grown in the past decade. When making wire bonds with copper, a nitrogen blanket is used to prevent the formation of copper oxide during the bonding process. It is also necessary to maintain tight control of processing parameters on the wire bonding machines because copper is harder than gold, and higher forces are required to effect the weld. These high forces if not closely controlled may damage the die.

Tape Automated Bonding (TAB)

In tape automated bonding (TAB), the small diameter wires described previously are replaced with a precisely etch series of foil leads supported on a plastic carrier. An example of typical TAB tape is shown in Fig. 4.52. The plastic carrier is in the form of a roll of film with sprocket holes so that the TAB lead pattern can be automatically positioned over a chip. The lead pattern is etched in very thin copper foil and then plated with gold to protect the foil from oxidation during storage and to facilitate welding to the chip bonding pads. The pattern is positioned over the chip bonding pads and a heated pressure head is lowered over the assembly to form a thermo compression bond to all of the chip pads. After this inner lead bond is complete, the chip may be tested to insure that it is totally functional before completing the assembly of the chip carrier. The final step in the TAB process is making the connections to the pads on the chip carrier. This series of bonds is made in the same way, with a larger pressure head designed to conform to the pad array on the chip carrier.

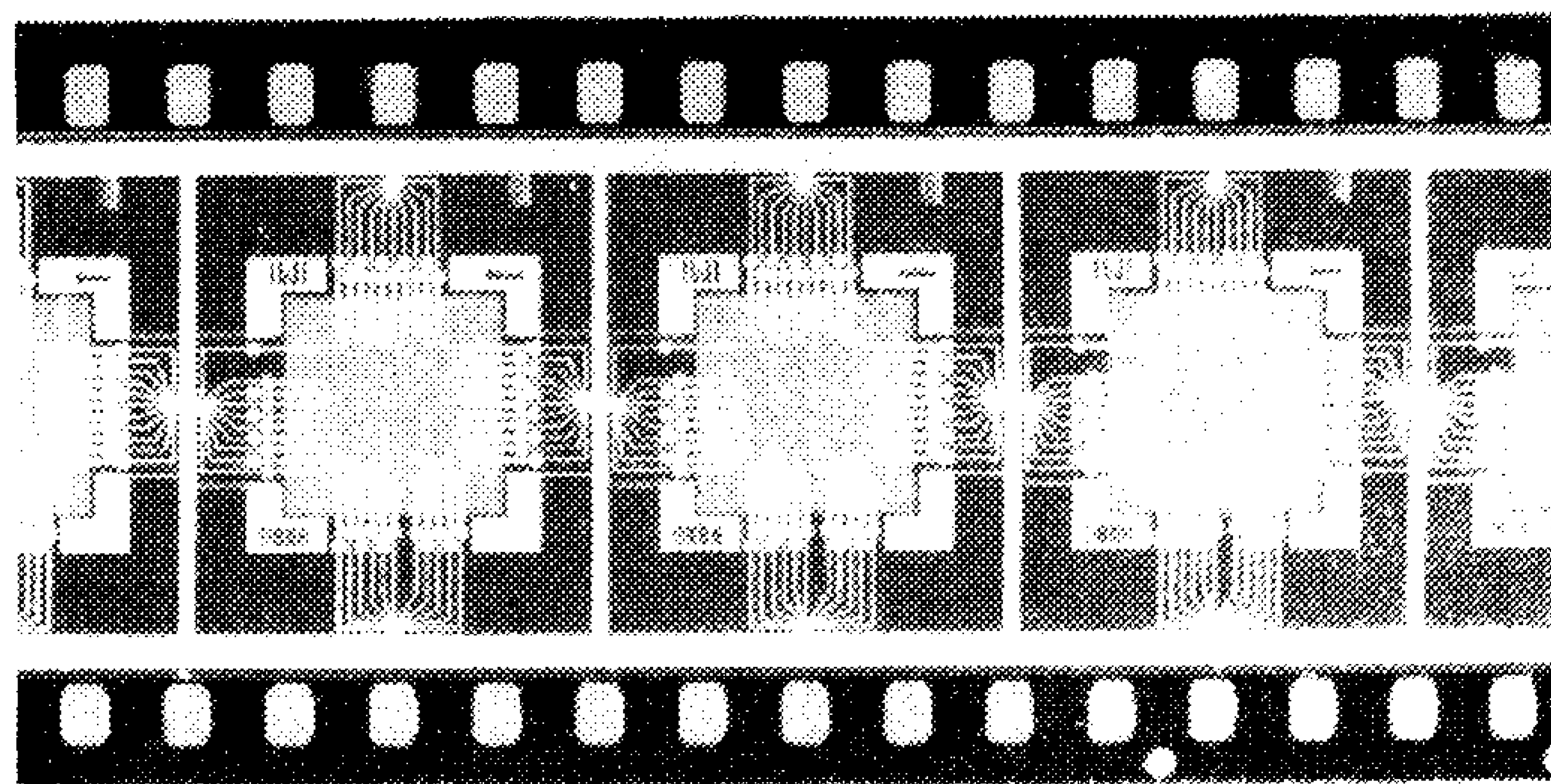

Fig. 4.52 Sprocket holes in the polyimide tape are used to position the tape over the die.

TAB is typically a single sided polyimide based circuit, although tape with metal on both of its sides is available. Copper is either electro-deposited to the tape or rolled copper is attached to the tape using an adhesive. The circuit traces are then produced using a photolithography process that will be described in Chapter 5. The main advantage of TAB is the small pitch of the bonding pads that can be accommodated. Currently, line pitches of 45 μm can be achieved (22.5 micron lines/spaces), which enables the used of TAB with high-density circuits that require a high pin count. The polyimide film is available in three widths, 35 mm, 48 mm and 70 mm, allowing the process to accommodate different size chips. The other critical dimension is length of the part, which is typically measured in sprocket pitches (see Fig. 4.52). Each sprocket pitch is equal to 4.75 mm, and most lithographic systems are

capable of an image length of 16 pitches (76 mm). The base polyimide film is typically between
100 microns thick.

The critical feature for TAB processing is cutting holes in the tape to expose the circuit
that are to be bonded to the chip. The leads on the tape are cantilevered over the position of each
bump on the die. Similarly, other holes are cut in the tape to allow for connections to the lead fram
directly to the PCB.

There are two common methods of welding the gold bump on a die to the lead on a
trace—a single-point process with heat and ultrasonic forces applied to the bonding pad on the chip
gang thermal compression process. In single-point bonding, the weld is made to each of the die's
sites individually. This single-point process is more time-consuming than the gang bonding.
bonding employs a specially designed bonding head to apply pressure and temperature
simultaneously make thermal compression (diffusion) welds between the TAB leads and gold bumps
the die. The gang bonding process has a high throughput rate, and is preferred to the single-
bonding process.

TAB has several advantages over wire bonding which include:

- TAB permits use of smaller bond pads and smaller bonding pitch
- Bonding pads can be deployed over the entire area of the chip to increase the I/O count
- The quantity of gold required for bonding is decreased.
- Less time is required in production if gang bonding is employed.
- TAB connections provide better electrical performance (reduced noise and higher frequency
- TAB connections can be made on flexible circuit materials.
- TAB enables the chip to be tested after completing only the inner lead connections.

The disadvantages of TAB include:

- The additional time and cost due to fabricating and patterning the tape.
- The capital expense for TAB equipment that is needed in addition to the machines used for wire bonding.

TAB is a better alternative to conventional wire bonding if very fine bond pitch, reduced die size and
higher circuit density are required. It is also the only suitable manufacturing method when the circuits
must be flexible (i.e. printers, flex cables, folding components, etc.) TAB is usually more cost-effective
in high-volume production, because the time and cost of developing the tape become less important
when large quantities of a product are produced.

The welded joints formed with TAB require additional processing of the chip bonding pads.
This added processing is performed on the wafer before it is separated into chips. The aluminum
bonding pads are plated with chromium and copper to develop a bump which raises the pad well above
the surface of the chip as indicated in Fig. 4.53. The bumps are then gold plated to facilitate thermo-
compression welding. The chromium barrier layer serves to limit migration of the gold and aluminum
atoms and inhibits the formation of Al-Au intermetallics which can degrade the joint.

Flip Chip Connections to a Chip Carrier

In standard chip carriers, the chip is positioned on its back surface and electrical connections are made
to the bonding pads located about the perimeter on its top surface. In chip carriers using flip chip
technology, this standard orientation of the chip is reversed. The chip is placed face downward and the
back side of the chip faces upwards. This flip chip orientation has a significant advantage in that it
concentrates the electrical functions on the underside of the chip leaving the top side free for use in

developing a highly efficient method for heat dissipation. In addition, today's trend toward higher device clock speeds, smaller devices for mobile and portable applications and higher I/O count make flip-chip the technology of choice. Flip chip technology offers several other advantages including: superior electrical performance due to the shorter electrical connections between the chip and substrate that result in smaller package size. Also attachment of high I/O devices becomes very cost competitive in flip-chip, compared to wire bonding, because hundreds of I/Os can be connected in a single process step.

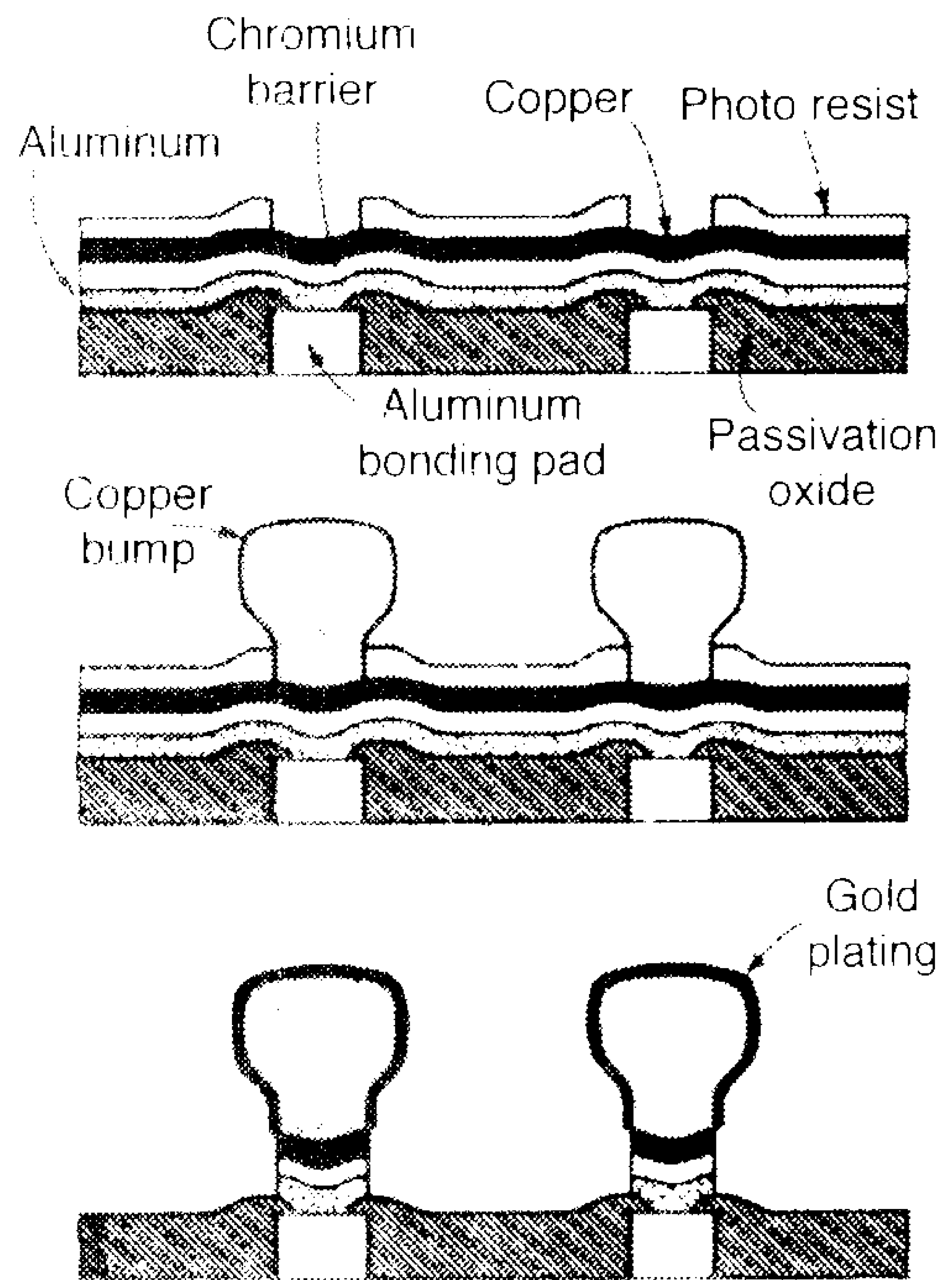

Fig. 4.53 Processing steps followed in placing gold plated solder bumps on a chip in preparation for TAB bonding.

The flip chip method of connecting the bonding pads to the chip carrier was originally developed by IBM in 1964 and was used exclusively by that company for many years in its high performance computers and signal processors. The original process was identified as C4 by IBM to identify a controlled collapsible chip connection. In this process, the chip bonding pads are deployed in an area array over the surface of chip in contrast to the deployment of these pads around its perimeter. By using these area arrays of bonding pads a higher I/O count is possible.

To insure a low and stable contact resistance at the bump-bond pad interface, the aluminum bond pads are metallized to eliminate non-conductive aluminum oxide. The under bump metallization involves evaporation of layers of chrome, copper and gold over the entire surface of the wafer. This layered structure acts as a hermetic seal, provides an electrically conductive diffusion barrier, and establishes a good mechanical base for the solder bump. Solder bumps are placed on these pads by either an evaporative process that is the preferred method for lead based solders, or by electroplating, which can be used for the application of any metal. After the deposition, a reflow process forms the spherical solder bumps as shown in Fig. 4.54.

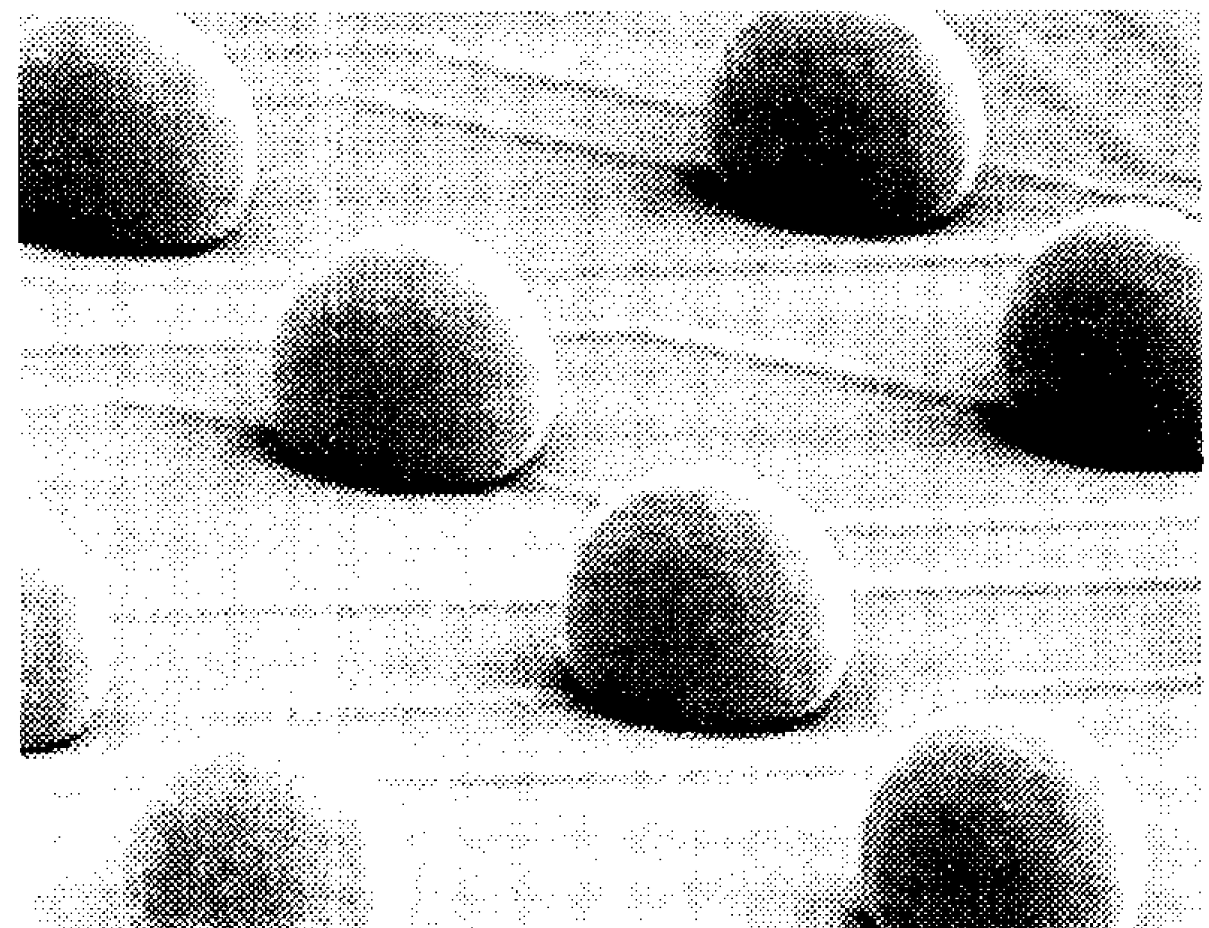

Fig. 4.54 Solder bumps deployed over the active area of the chip.

The spacing on the bonding pads vary with the application, but high performance processors employ pads on 200 μm centers that yields 2500 solder bumps per square centimeter. The solder bumps are 100 μm in diameter. The composition of the solder bumps is usually 97% lead and 3% tin. Matching bonding pads are produced on the substrate so that the pads on the chip and the ceramic coincide. The chip with its solder bumps is placed over the substrate with matching pads aligned. The assembly is heated until the solder spheres begin to soften and a controlled collapse of the sphere takes place as the solder simultaneously wets both pads. Surface tension of the solder controls the geometry of the solder joints until the solder solidifies. Solder flow from the joints along the circuit traces on either the chip or the substrate is prevented by plating these traces with metals like chromium which inhibit solder flow. This treatment controls the exact quantity of solder at the joint and provides for solder pillars about 75 to 100 μm high between the chip and the substrate. Precise control of the quantity of solder also prevents the formation of solder bridges between the closely spaced leads during the reflow process. After the completion of the reflow process, the space between the chip and the substrate is washed to remove any flux residues. When organic substrate materials are used, a significant mismatch exists in the thermal coefficient of expansion of the organic laminate and the silicon of the chip. In these cases, the gap between the chip and the substrate is filled with an adhesive. This adhesive, known as an underfill, serves to reduce the shear strains that result from temperature cycling that occurs in service.

4.3.3 Interposer Substrates

Designers of first, second and third level packaging have recognized for many decades that several layers of conductors are needed to make all of the interconnections necessary to wire a chip, PCB or mother board. However, there are several approaches to connecting the layers. The oldest method for connecting the conducting layers in organic boards was by plated-through-holes. Circuits boards are manufactured, bonded together, several boards are stacked and then drilled. The trough holes are plated with copper to form vertical conductors. With ceramic, multi-layer substrates are fabricated from green sheets that have printed circuits and filled via holes. These multi-layered substrates are co-fired to form in-plane circuits as well as conductors through the filled vias to provide z direction connections.

A circuit interposer is defined as either a material or construction that electrically and mechanically connects a pair of conducting layers in the z direction without interfering with x-y plane wiring. Perhaps the simplest interposer is an anisotropic conductive adhesive. In the 1980s, a process was introduced for making z direction connections using an adhesive that incorporated small solder balls in a B-staged epoxy film. The concept was to join pairs of double-sided circuit boards with this anisotropic adhesive film. The circuit boards were stacked and placed in a laminating press where heat cured the adhesive and pressure forced the solder powder to contact and connect the opposing pair of copper pads as shown in Fig. 4.55. The solder particles formed small but robust connections that remained intact during subsequent soldering operations.

One difficult with the anisotropic conductive adhesive was the random pattern of the small solder balls that limited its application to low density circuit boards. To extend the application to circuit boards with increased density it was necessary to develop a patterned anisotropic conductor. In the 1990s designers began to develop interposers using flexible circuits because of the thinness, compliancy, and ability to support high-density circuits on polyimide films. Microvias were laser drilled through the polyimide film with dry film adhesive on both sides. These microvias were filled with a conducting adhesive and B-staged. Double-sided circuit boards are then bonded together with these patterned interposer films to make high-density substrates.

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[8] Different substrate materials are employed depending on the application. Ceramic, glass-ceramic and organic laminates with BT epoxies are the most commonly used materials.

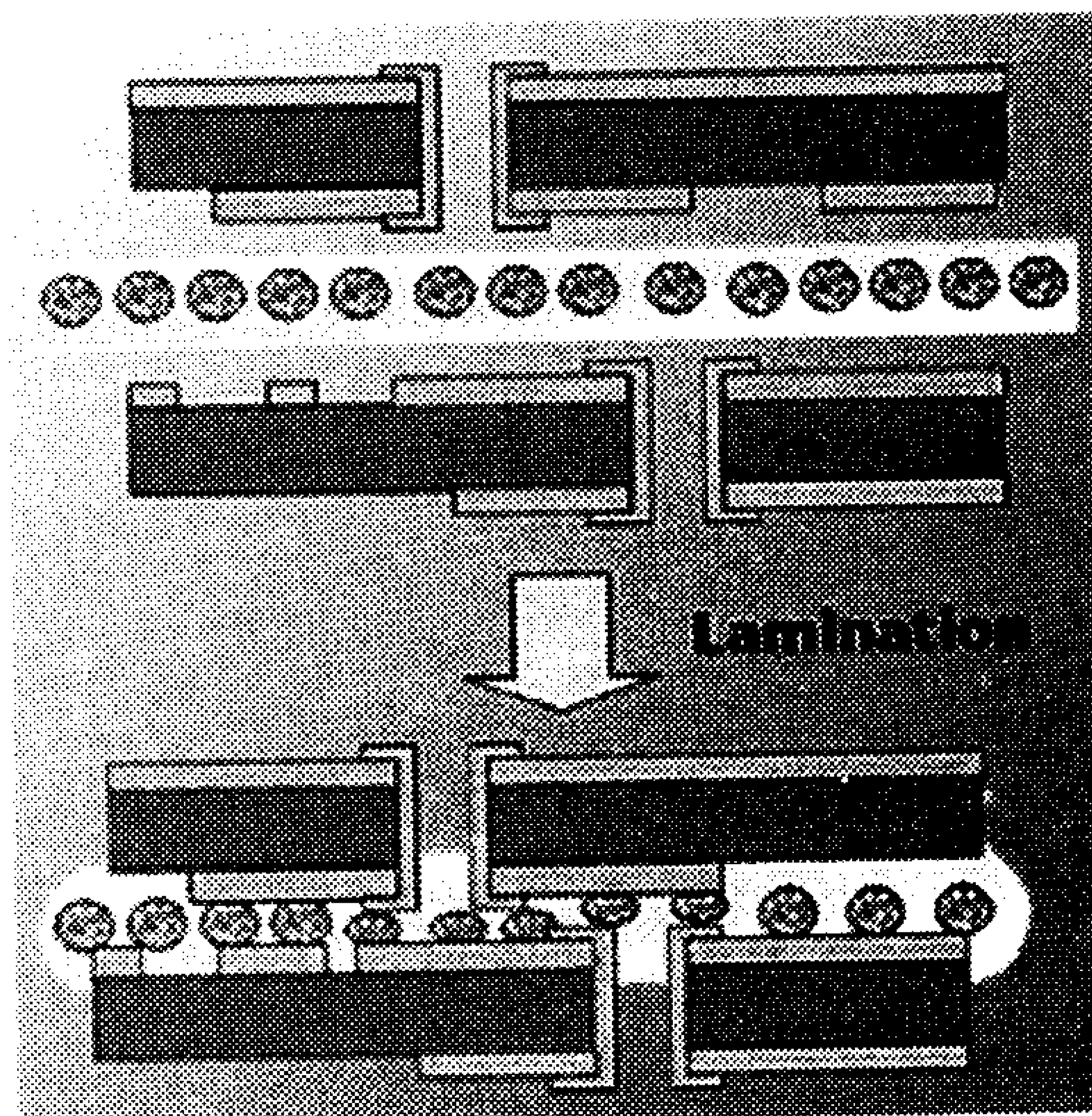

Fig. 4.55 An adhesive interposer to make connections between two double-sided circuit boards.

In both ball-grid-arrays and CSPs, the chips are bonded to a substrate that often serves as interposer because it is positioned between the chip and the I/O leads. The interposer has several functions in addition to supporting the chip and sometimes enclosing the package. The substrate contains the wiring pads for either wire bonding of flip chip connections. It may have vias and several layers of wiring to distribute the signals to the array of solder balls. The interposer provides a test bed for verifying the electrical integrity of the chip. Finally it provides a surface to support the solder mask required to prevent solder bridging during reflow operations. The coefficient of thermal expansion of the materials used in fabricating the interposer is very important because they markedly influence the thermal strains imposed on the chip or the C4 joints if the chip is bonded with flip-chip processes.

There are four general types of interposers—lead frame, rigid, flexible and wafer. We will describe each below:

Lead Frame Interposer

The lead frame interposer is employed on memory chips with a low I/O count. These chips have a small number of gull wing leads extending from two sides of the package. The construction is similar to that found in plastic encapsulated packages except the lead frame chip extends over the chip. Connections are made to lead wires along the length of the chip with wire bonding.

Rigid Interposer

Rigid interposers are made from either organic or ceramic substrates. As the name implies, they are rigid (high elastic modulus). The illustration, presented in Fig 4.38, shows a single layer laminate with wire bonding; however, rigid interposers often have several layers with microvias, blind vias and wiring planes with flip chip bonding. Materials for the ceramic interposers are usually mixtures of alumina and glass that are sintered together to form a material with a low coefficient of thermal expansion (4 to 6 × 10^{-6}/°C). Circuit traces and vias are formed from refractory metals. Matching the coefficient of thermal expansion of the interposer and the chip minimizes the thermal strains induced in the chip during operation.

Organic substrates are often employed with ball-grid-array assemblies as illustrated in Fig. 4.56. The BGA package is sometimes fabricated by wire-bonding a chip on a substrate made of a two-metal layer copper clad bismaleimide triazine (BT) laminate. The BT laminate is used in place of the standard and multi-functional FR4 laminates because of its high glass transition temperature of 170 – 215° C and

heat resistance (exposure to 230° C for 30 minutes with no degradation). The standard core thickness of this two-layer substrate is typically 0.2 mm. The copper cladding is typically ½ ounce (18 μm thick) with foils bonded on each side. Four-metal layer substrate designs are sometimes specified to provide additional power and/or ground planes that improve electrical and thermal performance.

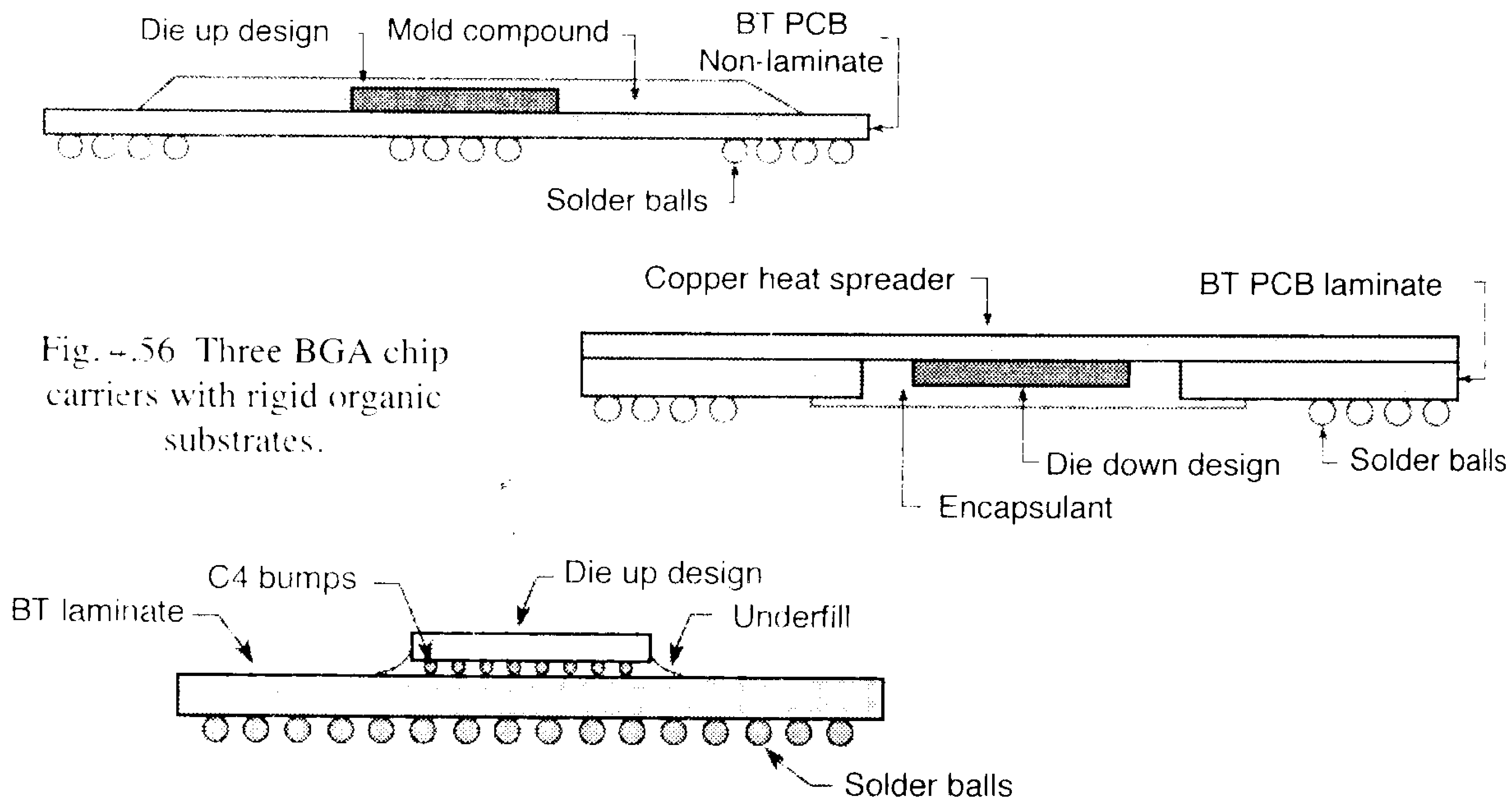

Fig. 4.56 Three BGA chip carriers with rigid organic substrates.

Flexible Interposer

Flexible interposers use a polyimide flexible circuit to connect the chip to the substrate similar to TAB tape interconnection. The most popular CSP of this type is the μBGA package. Interconnecting the chip to the interposer may include flip-chip bonding, wire bonding or TAB bonding. The concept of using flexible circuits as interposers is illustrated in Fig. 4.57. The flexible circuit, which may be multi-layered, contains the wiring and microvias needed to connect the chip I/O to the solder balls which serve as the package I/O. Connections from chip pads to the pads on the flexible circuit are wire bonded. Spacers are added to separate the chips and to provide the clearance required for the wire bonding. Solder balls are formed on the flexible circuit using procedures already described.

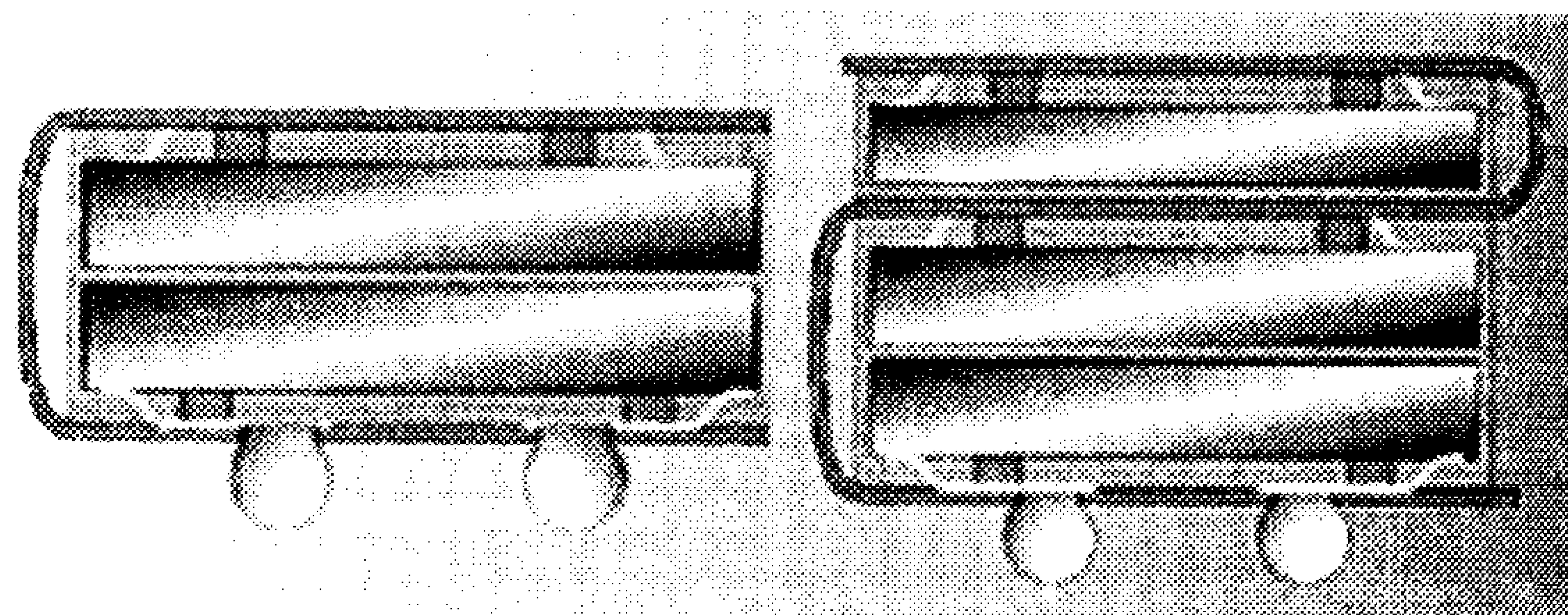

Fig. 4.57 Flexible circuits used as interposers for connecting chip I/O to package I/O.

Some molded interposers are considered flexible, because they also use a flexible circuit interconnection, as shown in Fig. 4.58. However, this type of package is encapsulated with conventional molded technology to protect the chip and its interconnections. Low modulus elastomers are employed in connecting the chip to the polyimide tape that serves as the flexible circuit. The ease of laser drilling microvias in thin film polyimide compared to laser drilling in glass reinforced epoxy is a major advantage in the growing use of flexible interposers.