Ball-grid-array packages are available in ceramic, plastic and organic laminate materials. The plastic ball-grid-array (PBGA) employs a wire bond to connect the bonding pads on the chip to the organic substrate as shown in Fig. 4.31. In this design, the solder balls are a lead free composition containing tin, silver and copper. The flip chip ball grid array (FCBGA), shown in of Fig. 4.32 utilizes and area array of C4 connections on the chip that are bonded to an organic substrate. Two other versions of ball-grid-arrays are available; both use flip chip connections to ceramic substrates. The first is the CBGA which is superior to the PBGA because it is hermetically sealed. A higher melting point solder (90% Pb and 10% Sn) is used in fabricating the solder ball[5]. Note that a lead free solder is used to bond the ball to both substrate and the PCB. A column version (CCGA) is also available where the solder balls have been replaced by short 20 mil (0.5 mm) diameter solder columns as shown in Fig. 4.33. The column heights vary from 50 to 87 mil (1.27 to 2.2 mm). These columns are used to space the ceramic chip carrier some distance away from the PCB. The increase in this dimension enables more effective cleaning and inspection. More importantly the added height of the solder joint decreases the shearing strains due to thermal cycling thereby increases its fatigue life.

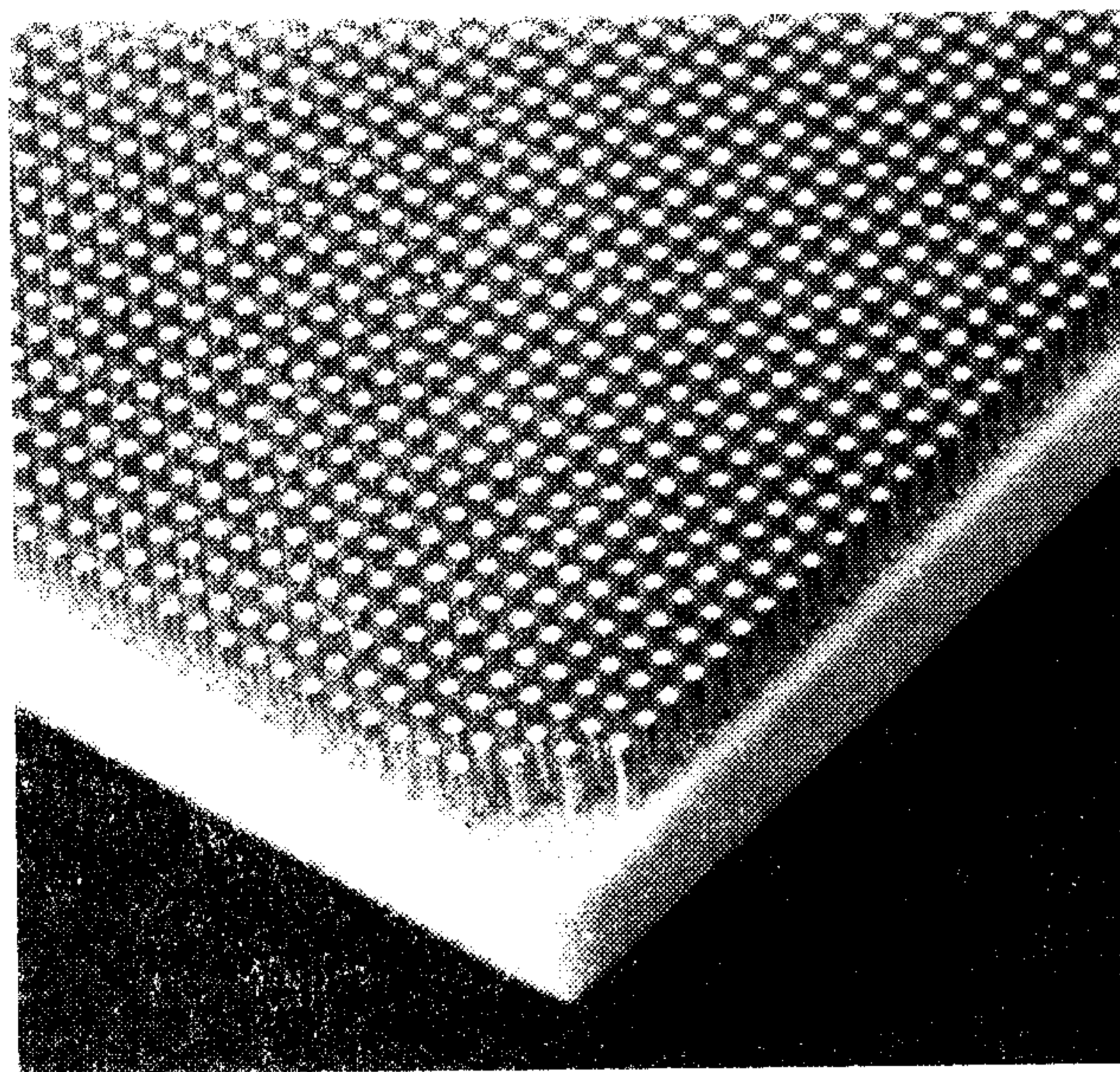

Fig. 4.33 Column grid array with columns replacing solder balls to improve solder joint fatigue life

The ball-grid-array with flip chip C4 connections lends itself to improved thermal design. As shown in Fig. 4.34, the narrow space, between the back of the die and the copper lid that serves as a heat spreader, is filled with thermal grease. This design reduces the thermal resistance between the chip and the cooling medium passing over the chip carrier. The flip chip with its C4 connections enhances heat flow downward through the substrate. The solder balls on close centers provide a low resistance path to the PCB.

Ball-grid-arrays exhibit several advantages when compared to leaded chip carriers, which include:

1. Higher I/O capability than surface mounted packages with either gull or J leads and indicated in Fig. 4.35.
2. Higher I/O for a specified footprint results in increased circuit density.
3. Reduced weight, size and cost because smaller packages enable more chips placed on a PCB.

[5] An exception is provided in the RoHS directive that allows solder with a high lead content (above 85%) in chip carriers.

4. The area array of the solder balls permit larger lead pitches for high I/O packages greatly reducing soldering problems.
5. Higher speed circuits because the connections are shorter with less resistance and inductance.
6. Improved heat dissipation (see Fig. 4.34).
7. BGA manufacturing methods are easy to extend to multi-chip modules.
8. Manufacturing processes are compatible with existing stencil printing and robotic mounting equipment.
9. Manufacturing advantages include:
   - Reduced coplanarity problems
   - Self centering during reflow reduces placement requirements
   - Larger pitch reduces solder bridging during paste printing
   - Elimination of fragile leads reduces handling problems
   - Higher yields achieved with BGAs during assembly

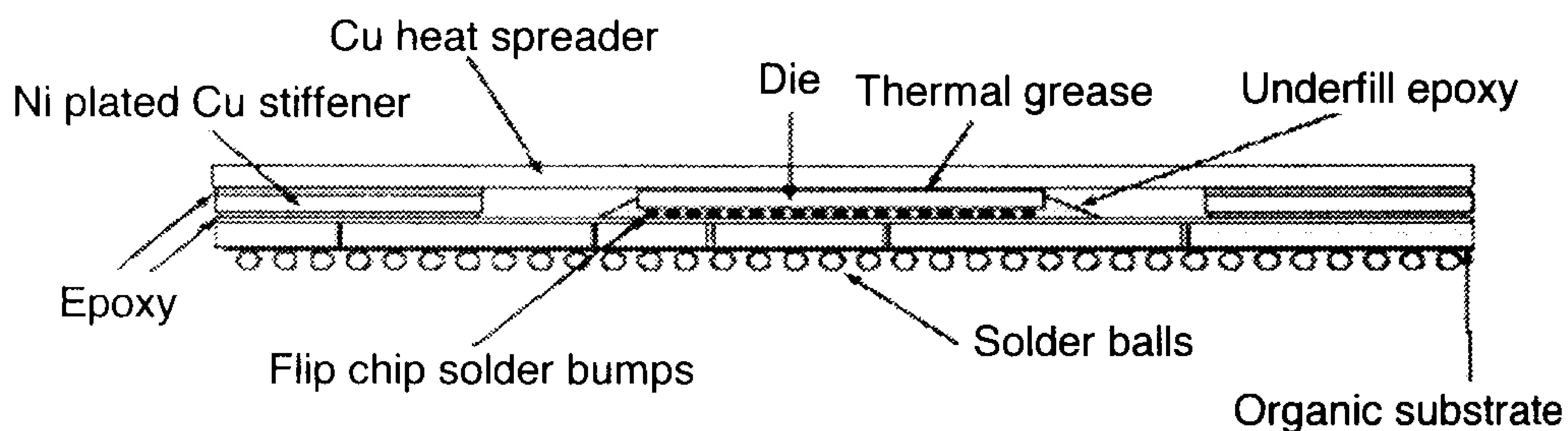

Fig. 4.34 A BGA with flip chip bonding designed to enhance heat transfer from the chip's back side.

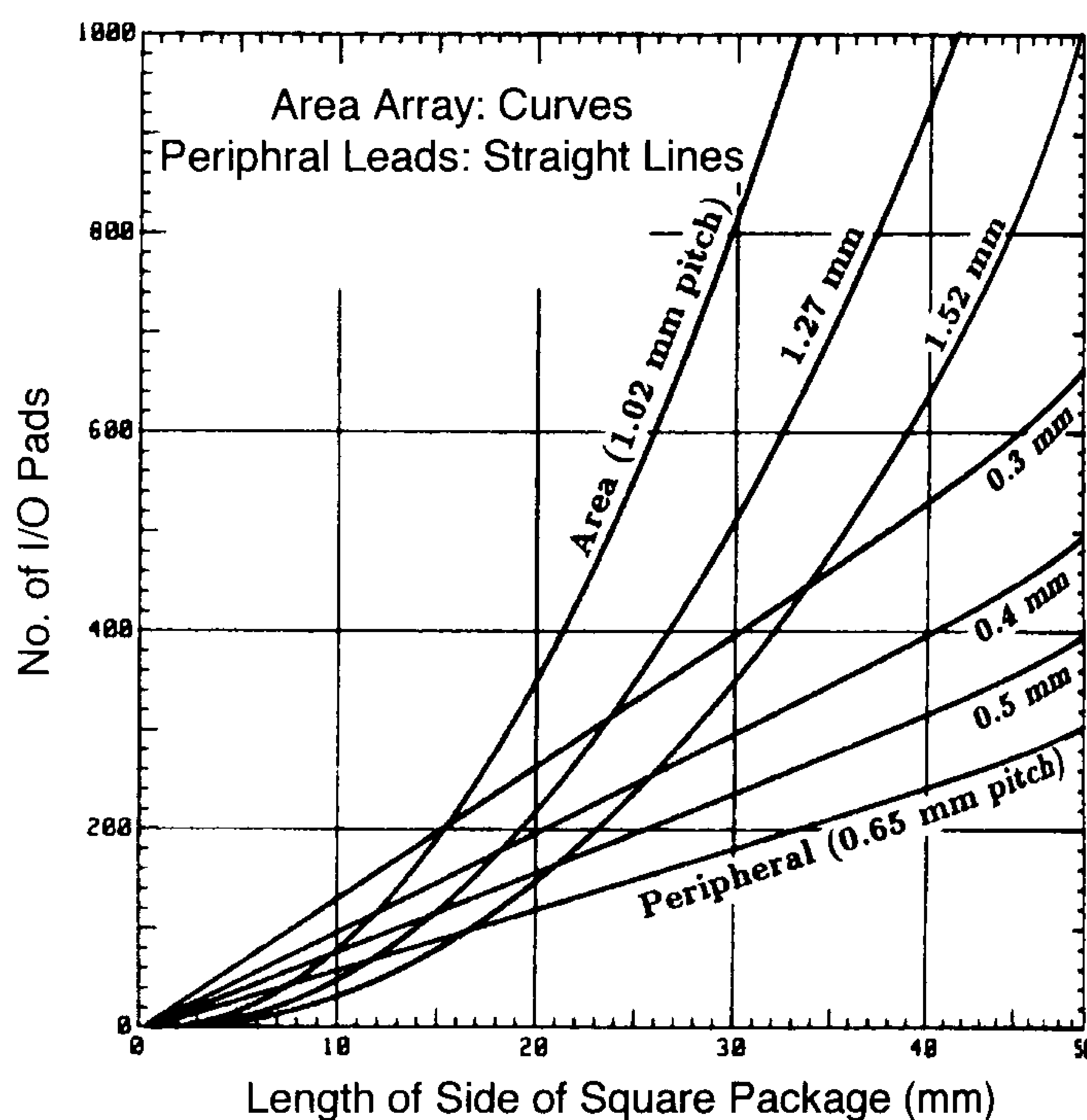

Fig. 4.35 I/O count as a function of package size for peripheral and area deployed bonding pads with different pitch.

There are some disadvantages associated with using BGA chip carriers that include

1. It is not possible to rework individual solder joints.
2. It is impossible to visually inspect the solder joints beneath to package except for CCGA column packages.
3. The rigidity of the chip carrier and the solder joints increases the possibility of solder joint failure by thermal cycling.

Chip Scale Packaging

Pressures continue to build for the chip manufactures to develop product that will enable designers to develop systems in smaller, thinner and lower weight envelops. Of particular importance is the market for portable products such as cell phones, laptop computers, music recorders and players and video cameras. Current packaging trends are illustrated in the block diagram presented in Fig. 4.36. This diagram begins with attempts to improve the packaging density of the quad flat pack with a lead pitch of 20 mil (0.5 mm). Attempts to move to 16 mil (0.4 mm) pitch have introduced soldering difficulties that have escalated assembly costs. Direct chip attachment with the flip chip process has been hampered by the technical challenges in testing, handling and placement of bare dies. Chip scale packaging (CSP) has developed as a suitable transition step between fine pitch leaded chip carriers and direct attachment of the chip to the circuit board with flip chip.

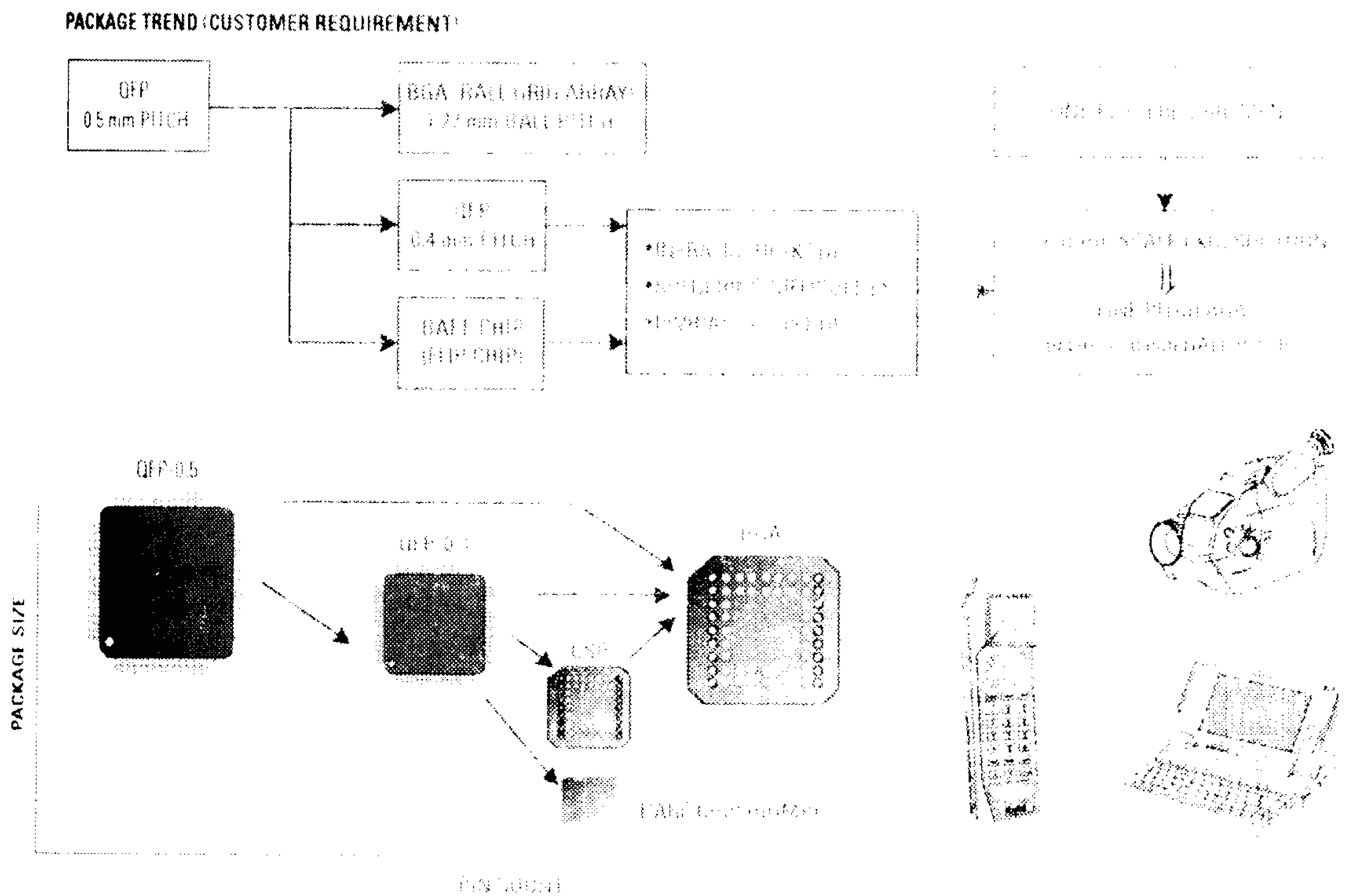

Fig. 4.36 Diagram showing trends to reduce the size and weight of chip carriers for portable electronics

The Chip Scale Package (CSP) has evolved from the ball grid array and is similar in many respects. One important distinction is the area of the chip relative to the area of the CSP. The package area of the CSP is limited to 1.2 times the chip area. This compares to a package area for either a BGA or a fine pitch quad flat pack that is four times the chip area. The photograph of a BGA presented in Fig

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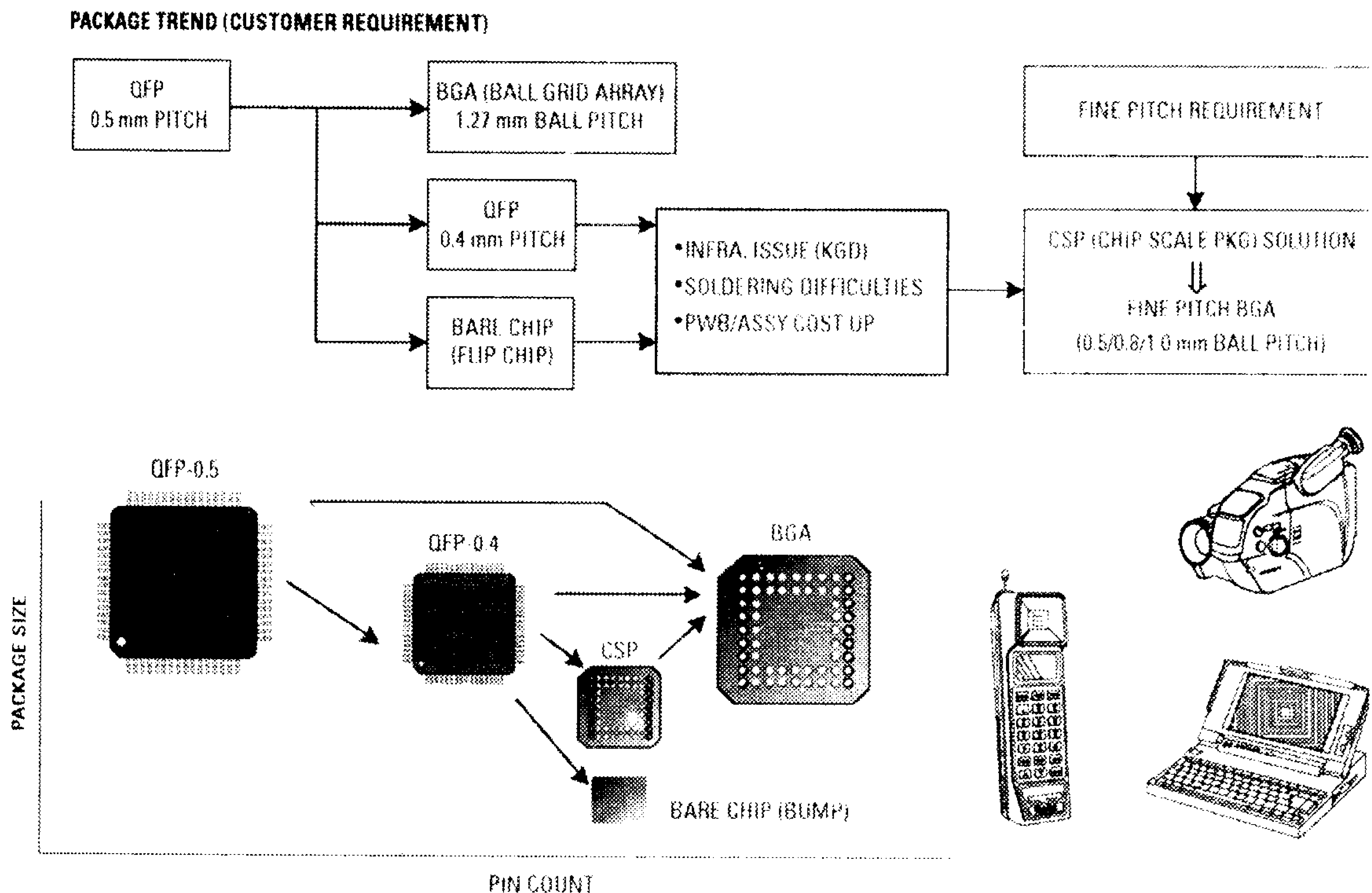

Fig. 4.36 Diagram showing trends to reduce the size and weight of chip carriers for portable electronics.

The Chip Scale Package (CSP) has evolved from the ball-grid-array, and is similar in many respects. One important distinction is the area of the chip relative to the area of the CSP. The package area of the CSP is limited to 1.2 times the chip area. This compares to a package area for either a BGA or a fine pitch quad flat pack that is four times the chip area. The photograph of a BGA presented in Fig.

4.37 shows the large area surrounding the chip that is reserved for the array of solder balls. It is clear that the development of the CSP chip carrier requires a marked reduction in the area of the chip carrier.

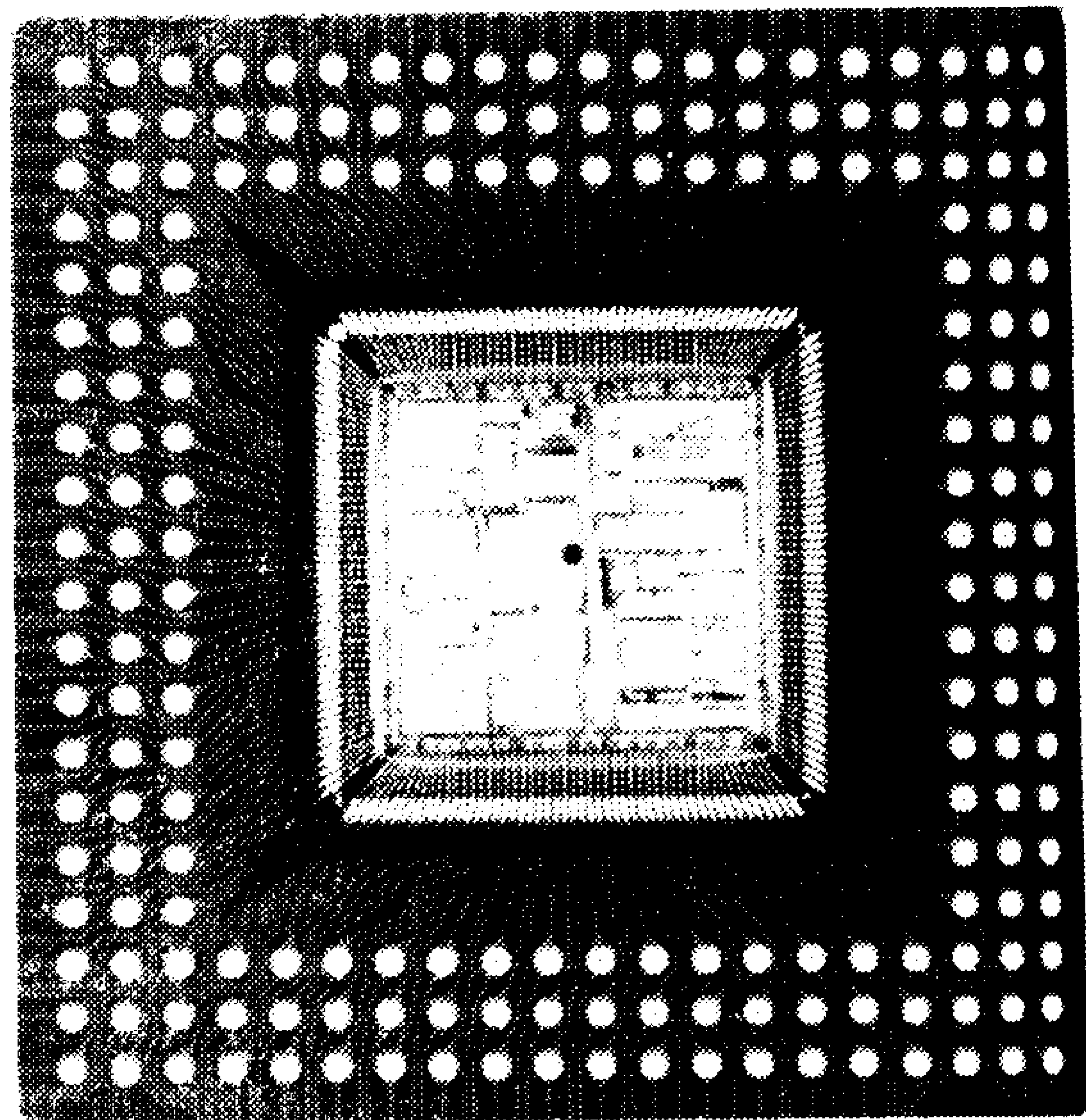

Fig. 4.37 The area of a BGA is about four times the area of the chip that it houses.

The CSP is a small package intended for chips with a lower I/O count. It employs solder balls deployed in an area array on its bottom surface for electrical and mechanical connections to a PCB. The definition of a CSP calls for packages with a lead pitch of 32 mil (0.8 mm) or less. Current CPS chip carriers are commercially available with lead pitches varying from 32 to 16 mil (0.8 to 0.4 mm). Bonding pad diameters range from 8 to 16 mil (0.20 to 0.40 mm). Both wire bonding and flip chip processes are employed with this package. However, flip chip is the preferred method because of the reduced size of the package that it affords. The very fine pitch CPS requires advanced manufacturing methods for the PCBs that involve microvias and very thin microstrip lines.

When wire bonding is employed in fabricating the CSP, connections are often made to a single row of pads deployed about the perimeter of a single layer laminate that forms the base of the package. A drawing showing this construction is presented in Fig. 4.38.

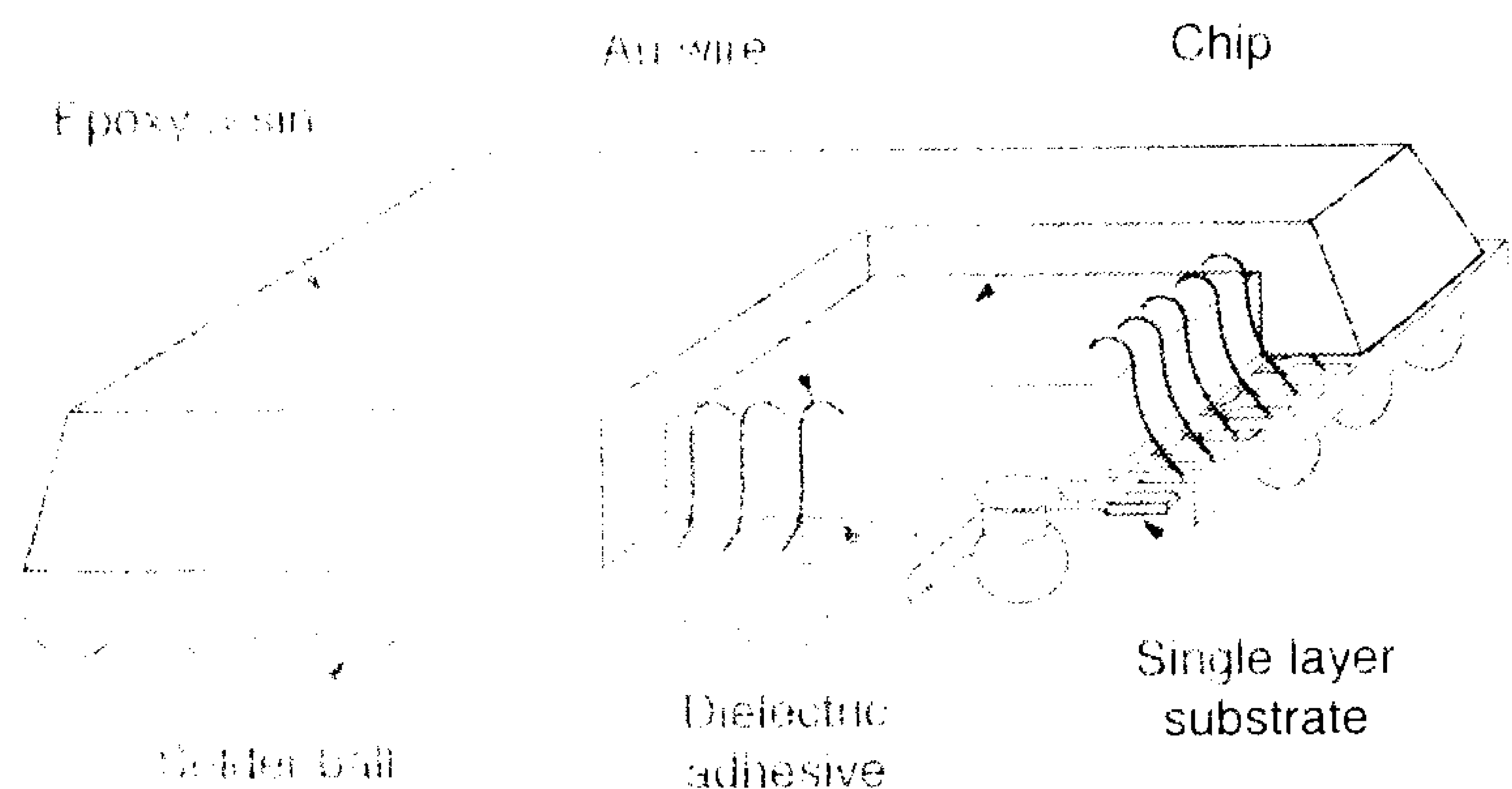

Fig. 4.38 Fabrication details for a CSP with wire bonded connections.

Fabrication details for a CSP with flip chip connections are presented in Fig. 4.39. This illustration shows that the back of the chip is exposed; however, the front of the chip with the circuits is protected by the substrate and the underfill adhesive. Flip chip bonding enables chips with higher I/O count to be placed in CSP and is superior to wire bonding for most applications.

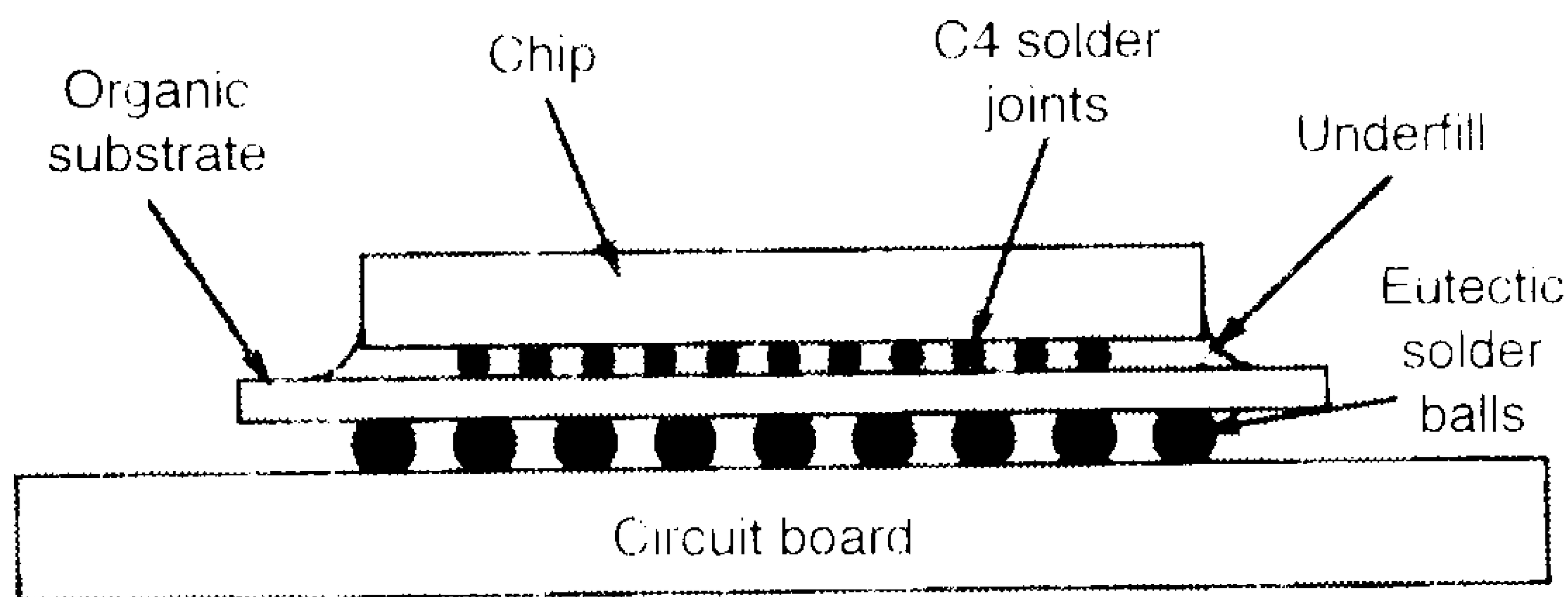

Fig. 4.39 Design of Motorola's slightly larger than IC chip package using flip chip bonding.

For chips with relatively low count I/O CSP offers several advantages when compared to direct chip attach, which include

- Speed of testing the chip.
- Superior die protection
- Better reliability without underfill
- Much easier to rework
- Superior yield due to easier handling and assembly

4.2.6 Multi-chip Modules

In most cases, electronic systems are assembled using a large number of components that are packaged as separate items. These individual components are mounted on a circuit card or cards and connected together with PCB wiring, connectors and cabling. In some cases, it is disadvantageous to package all of the components individually because of the need for added space for the connections and the loss of performance due to wiring length induced delays. It is often advantageous to house several devices which form a circuit function in a single multi-chip package.

Hybrid packages or multi-chip modules (MCM) are first level carriers which house several chips and other passive components together and provide the wiring necessary for circuit connections. Multi-chip modules are less important today than they were a decade ago, because modern chips have higher circuit density and systems on a chip have become more common. Nevertheless, MCM offer advantages when housing more complex products that perform more than one function. An example of a MCM is shown in Fig. 4.40. This module implements a 32-bit microprocessor, an ASIC co-processor with built-in set of interfaces, 6 Mbytes of protected instruction memory and 32 Mbytes of protected data memory. It is designed in a radiation tolerant technology qualified for space applications.

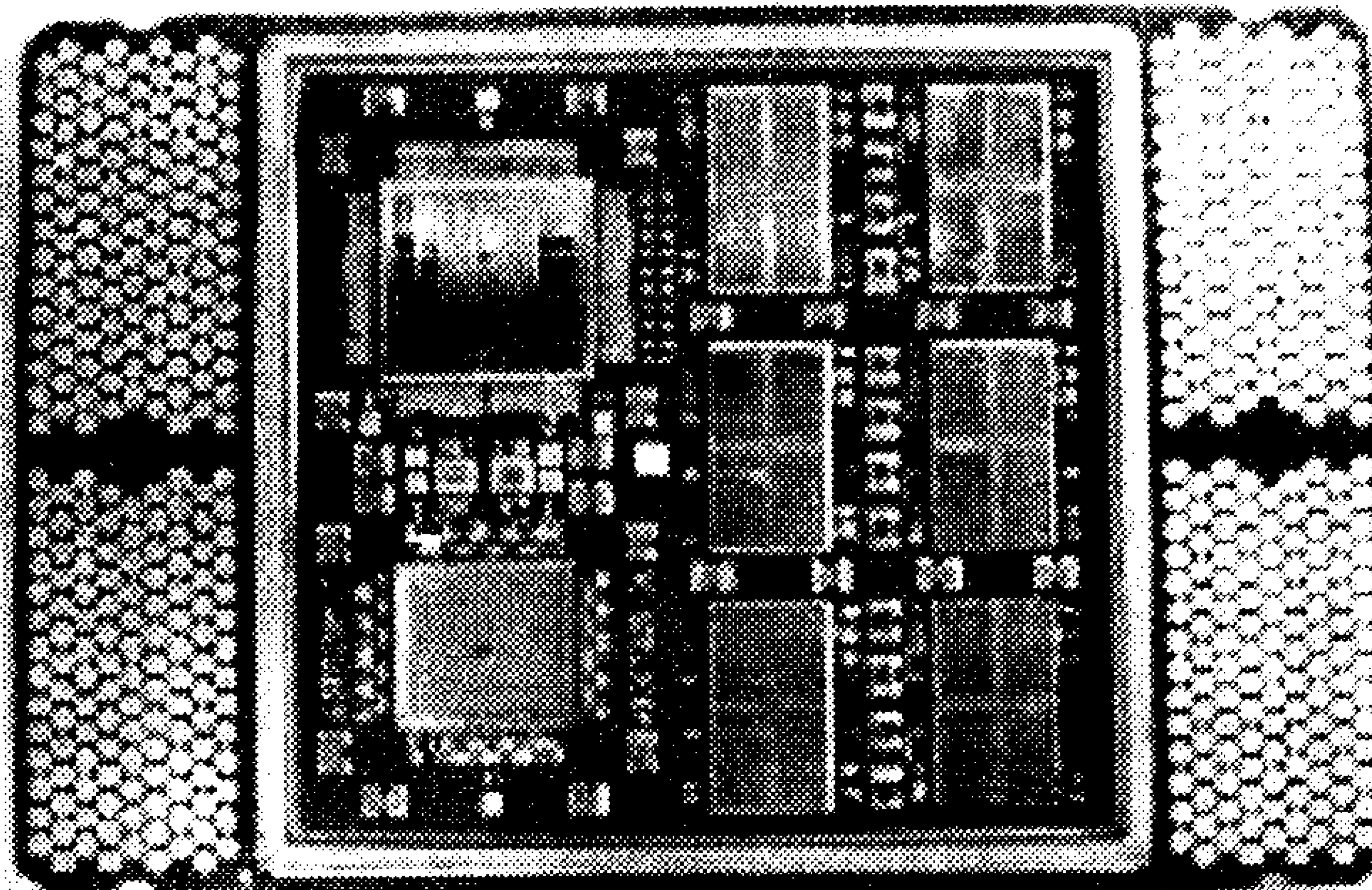

Fig. 4.40 Multi-chip module containing logic and memory chips as well as passive components.

In a sense the MCM is a combination of a first and second level package. It provides the protection function of a first level package and the wiring function of the second level package. The hybrids offer three advantages. In collecting together several relatively small chips, MCMs reduce the

area of the board required when compared to individual packages for each chip. Secondly, they reduce the complexity in wiring the circuit board, because the wiring between the chips is completed in the hybrid. Finally, the on board lead lengths are short and often with closely controlled impedance to facilitate timing in digital systems and/or circuit matching in analog systems.

Multi-chip carriers will continue to be an important first level packaging concept until custom design costs for special purpose chips are reduced sufficiently for the development of custom chips that economically replace the several of the smaller chips used in a MCM. Replacement of an MCM with a single customized chip housed in more standard chip carrier will provide a lower cost assembly, a more efficient design and a higher performance circuit.

The Thermal Conduction Multi-chip Module (TCMCM)

The thermal conduction module (TCM) was a multi-chip package designed and produced by IBM for use in its high performance computers in the early 1980s. The concept was adapted and modified by other firms for the design of the CPU for main frame and other large computers. The TCM has been replaced by a more modern multi-chip carrier that embodies the basic concepts introduced 25 years ago. In this text, we will discuss the newer design of the thermal conduction multi-chip module (TCMCM) in this chapter and in Chapter 9, because this method of packaging represents a major step forward in efficient design of electronic systems. The TCMCM is a very efficient (area and wiring length) chip carrier where the functions of the first and second level packages have been combined. In Chapter 9, we will consider the merits of this package in dissipating very large quantities of heat with a small thermal penalty.

The components involved in an assembly of a TCMCM that houses four chips for a high-performance IBM server, are shown in Fig. 4.41.

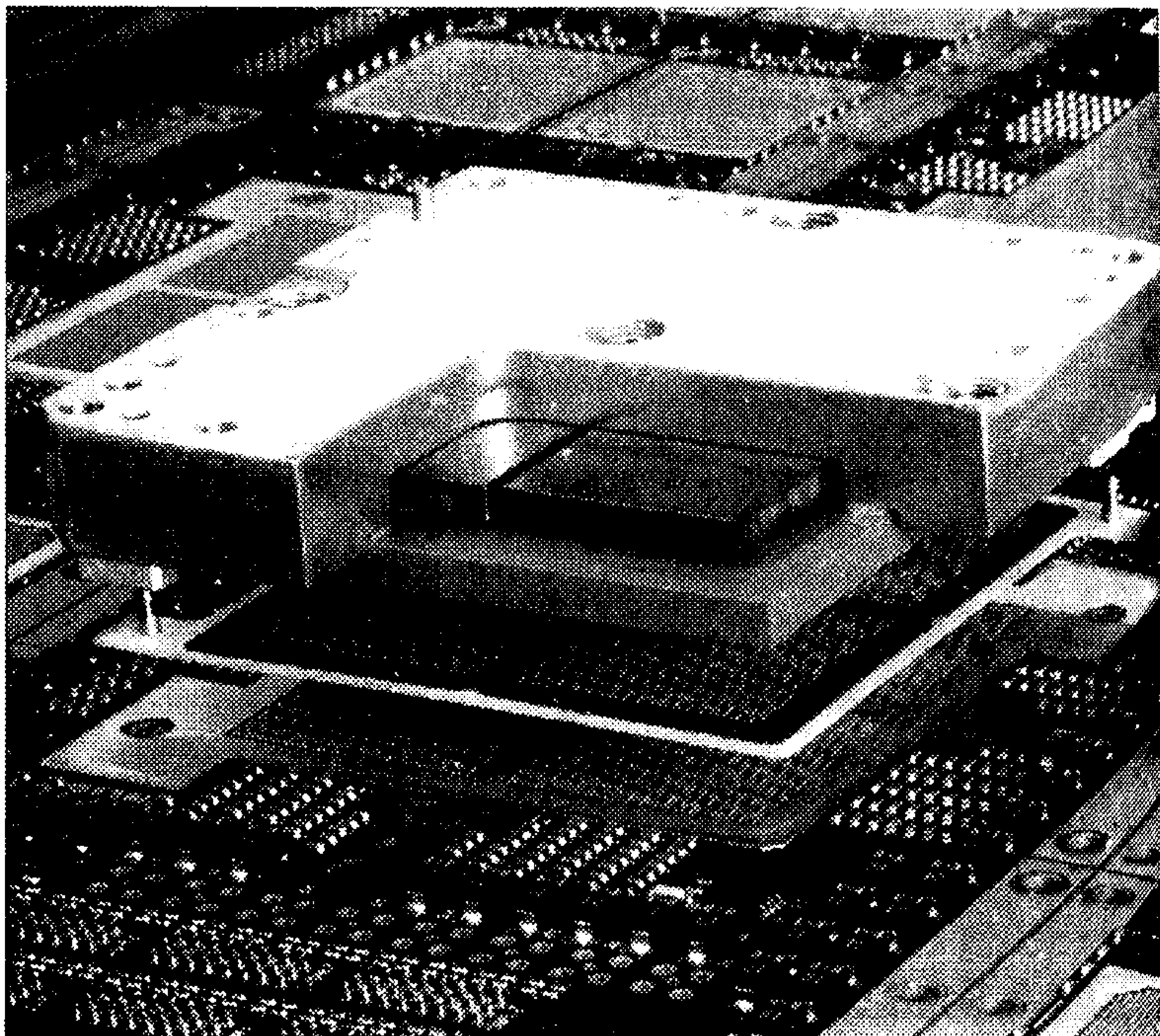

Fig. 4.41 A four chip multi-chip module used in an IBM high-performance server.

There are several layers in the stack making up this module. At the top, a heavy aluminum cover serves as a heat sink and a support for heat exchangers. Below the cover, two of the four SiC heat spreaders are visible. These heat spreaders are on top of the chips and serve to provide more effective heat conduction to the heat sink. The chips are not visible because they are covered by the heat spreaders that are much larger than the chips. The chips are bonded to a glass-ceramic substrate with

C4 connections. The next layer in the stack is a land grid array that contains an array of springs that connect the pads on the glass-ceramic substrate to the circuit board. The spring connections (fuzz buttons) are required because the coplanarity of the surfaces of the large glass-ceramic substrate and the circuit board is not sufficient for C4 connections. The spring connections also enable the module to be disconnected and reconnected to the printed circuit board.

This TCMCM house four high-performance chips each with [illegible] transistors. Connections on the chip are made with several layers of copper traces. Each chip is attached to the glass-ceramic substrate with 7018 C4 solder connections. The substrate, which is made from 84 layers, incorporates 1.7×10^6 internal copper vias and an area array of 100 μm contact pads placed on 200 μm centers on its top surface. The glass-ceramic substrate also contains 190 meters of co-sintered copper wiring. Off module pads (5,100) on a one millimeter pitch are located on the bottom surface of the substrate to provide connections to a unique land grid array. The package 85 by 85 mm in size contains up to 32 processors that operate at frequencies from 1.1 to 1.3 GHz. The module is capable of dissipating up to 624 W of heat.

Stacked Die Memory Packaging

In recent years, efforts to reduce area required on circuit board for memory chips have lead to the development of stacked dies in a single package or stacking of dies on separate CSP packages. An example of Amkor's stacked CSP is presented in Fig. 4.42. In this arrangement, a smaller memory die is adhesively bonded to a larger one. Bonding pads about the perimeter of both chips are available for wire bonding. When wire bonding is complete, the assembly is encapsulated and solder balls are plated and reflowed over the array of pads located on the bottom side of the package.

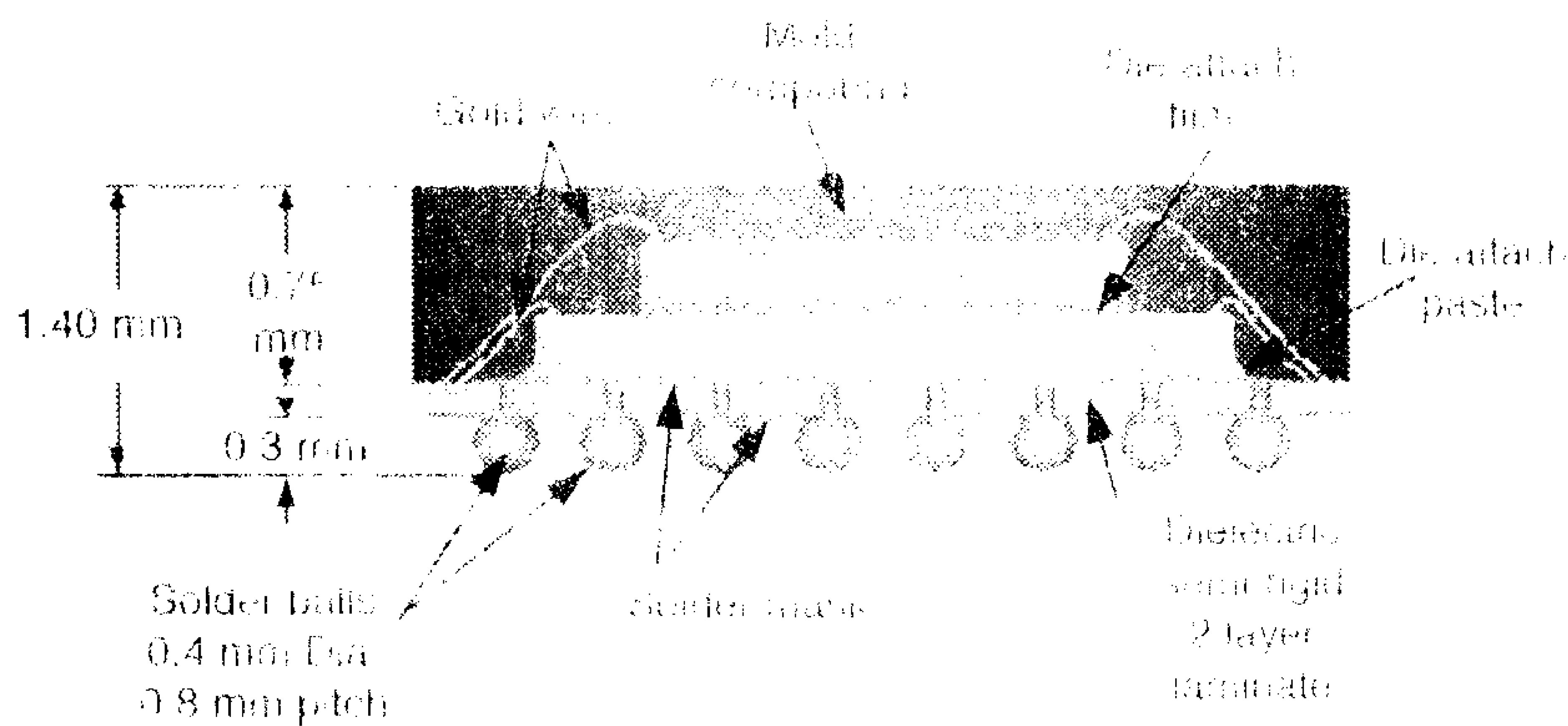

Fig. 4.42 Stacked memory dies in Amkor's CSP.

Another arrangement used to reduce circuit board area involves stacking CSP as indicated in Fig 4.43. In this photograph, three CSP are stacked to form a single package. The wiring in the substrates of the three packages must accommodate the combination of three memory chips and provide I/O on the bottom laminate, which enables connections that access to all three chips.

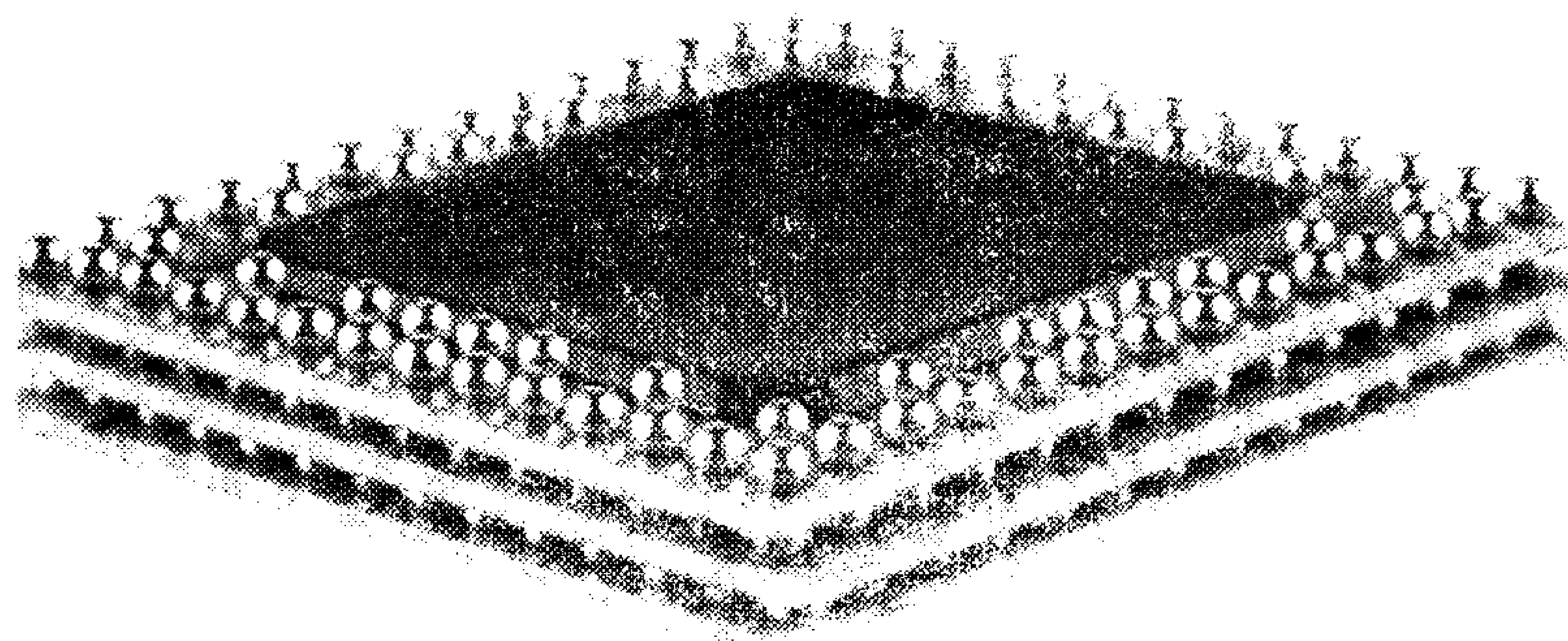

Fig. 4.43 Stacking of three CSP packages containing memory chips.

4.2.7 Ceramic Chip Carriers

The emphasis in this treatment has been on chip carriers encapsulated in plastic. Plastic chip carriers constitute by far the largest segment of the market[6]. Many of the first level packages described previously are available in ceramic versions; however, their significantly higher cost often prohibits wide spread usage. Ceramic chip carriers are usually specified for military and high performance applications where cost is less of a factor than performance. The most significant advantage that ceramic chip carriers have over plastic chip carriers is hermeticity. Moisture can in time diffuse through the plastic encapsulation and begin to corrode the circuit lines and bonding pads on the chip; thus, degrading the reliability of an electronic system. Ceramic is impervious. Moisture does not diffuse through the ceramic, glass or metal used in constructing the ceramic chip carriers.

There are two methods used in producing ceramic chip carriers—co-fired multi-layered construction and pressed two-layer construction. An example of a 14 pin DIP fabricated from ceramic is presented in Fig. 4.44. The body is made from three layers of ceramic green sheets. Circuit lines are printed onto the middle sheet with a glass-refractory metal mixture. The three sheets are stacked together in alignment and fired. During the firing process the ceramic green sheets are sintered and the volatiles are driven off the refractory metal ink forming a conducting line. The chip is brazed into the cavity of the ceramic body with gold silicon solder. The chip is wire bonded to the refractory metal pads deployed about the cavity. A metal lid is soldered in place under a vacuum to seal the chip within the ceramic package.

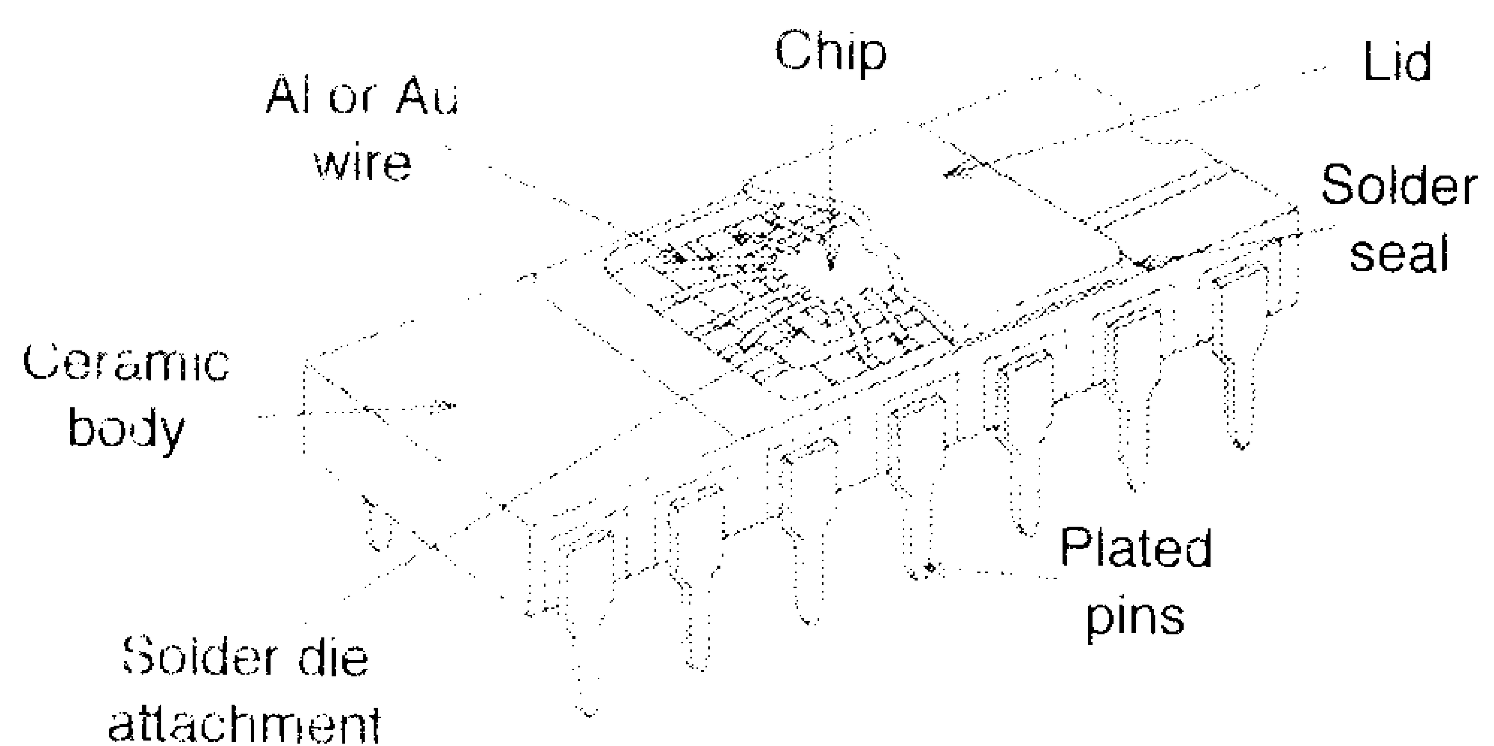

Fig. 4.44 Drawing of a co-fired ceramic DIP showing construction details

An example of pressed two layer construction of a ceramic surface mounted chip carrier is depicted in Fig. 4.45. In this approach, the base and the top layers are prepared by pressing a mixture of ceramic powder blended with a binder into molds. The two pieces are then sintered individually to form high density ceramic parts. A sandwich is then formed with the two ceramic layers, a lead frame and two layers of low melting point glass. The sandwich is then heated until the glass fuzes, welding all of the components together. The chip is brazed into the cavity of the package and connected with wire bonding. Finally a metal lid is solder to form a hermetically sealed package.

The pressed two-layer ceramic chip carriers are suitable for low pin count packages; however, for chips with higher I/O count two layers are not sufficient to accommodate all of the wiring that is required. In these cases, co-fired multilayer construction is employed where additional layers are added to accommodate vias and wiring in both the x and y directions. An example of a pin-grid-array with several layers of co-fired ceramics is presented in Fig. 4.46.

[6] When the market is measured in numbers of packages used plastic chip carriers are dominant; however, when measured in dollars, ceramic packages constitute about 2/3 of the market.

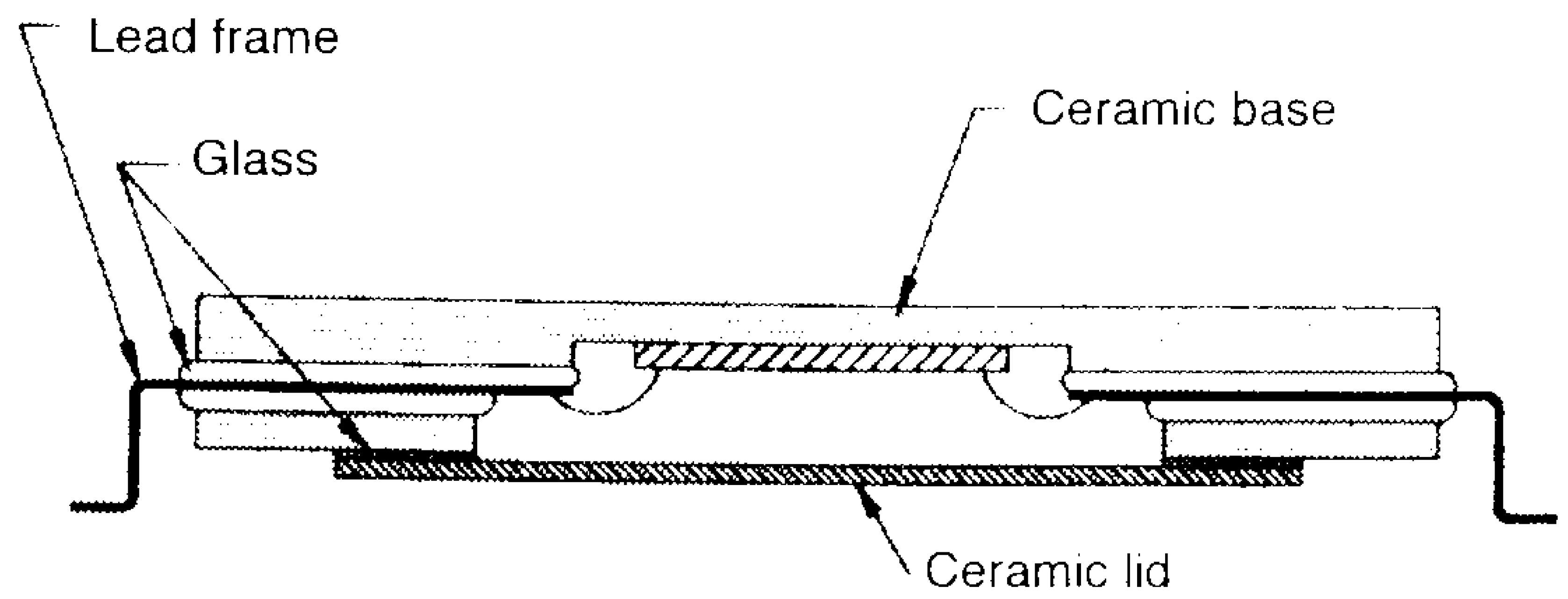

Fig. 4.45 Construction details of a surface mounted ceramic chip carrier with two-layers.

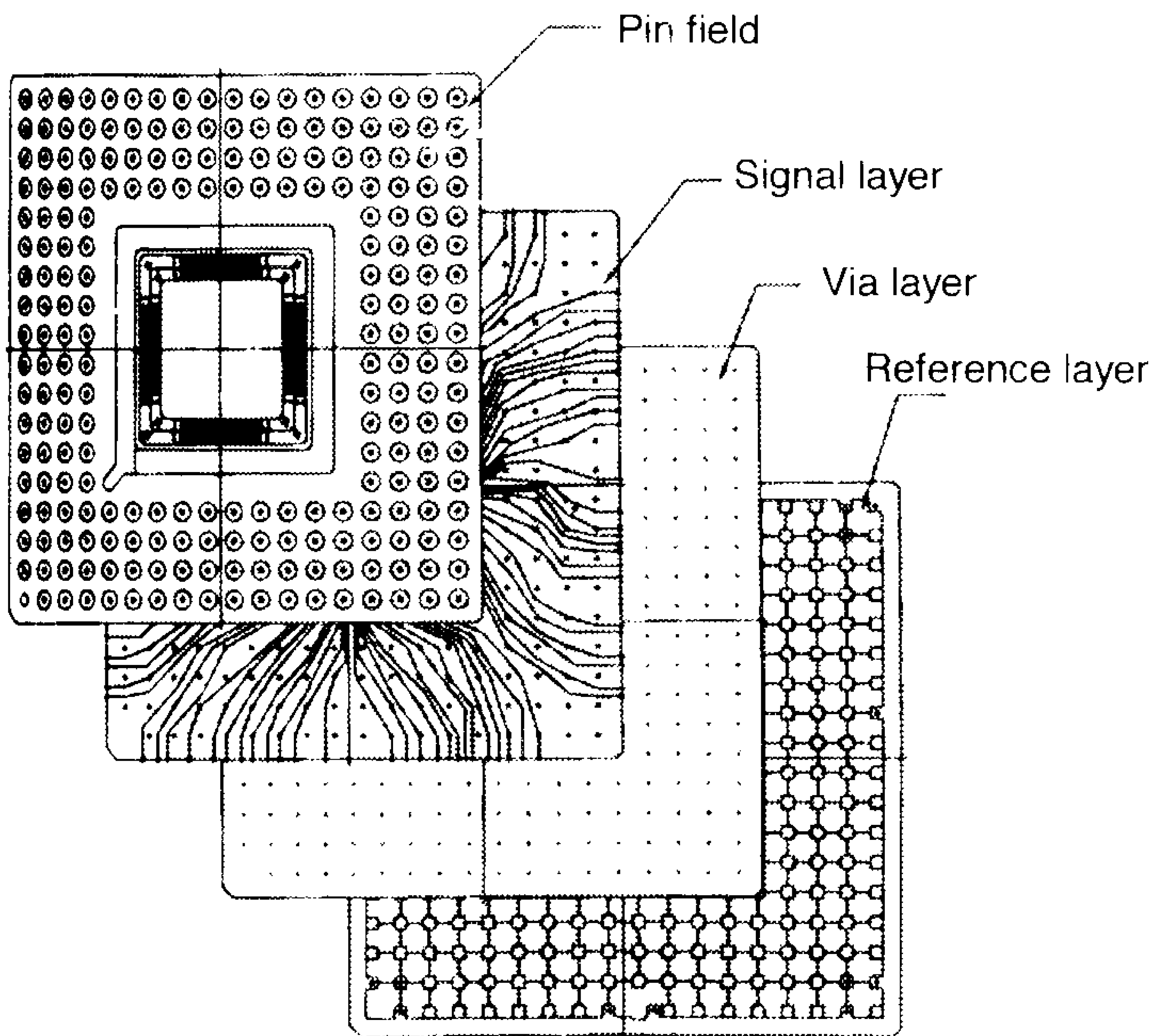

Fig. 4.46 Layers of co-fired green sheets form the substrate for a pin array chip carrier.

Co-fired green sheets are also used to form multi-layered substrates for multi-chip-modules, as illustrated in Fig. 4.47. These substrates are made up of tens of layers. The top layer has the metal pads to which the flip chips are bonded. Next several layers are devoted to redistribution where the wiring lines are fanned out to provide additional width and spacing. Many center layers are used in transmitting signal pulses between the chips and the I/O pads on the module. Finally the bottom layers are used to distribute power to the chips and to connect with the I/O pins or pads.

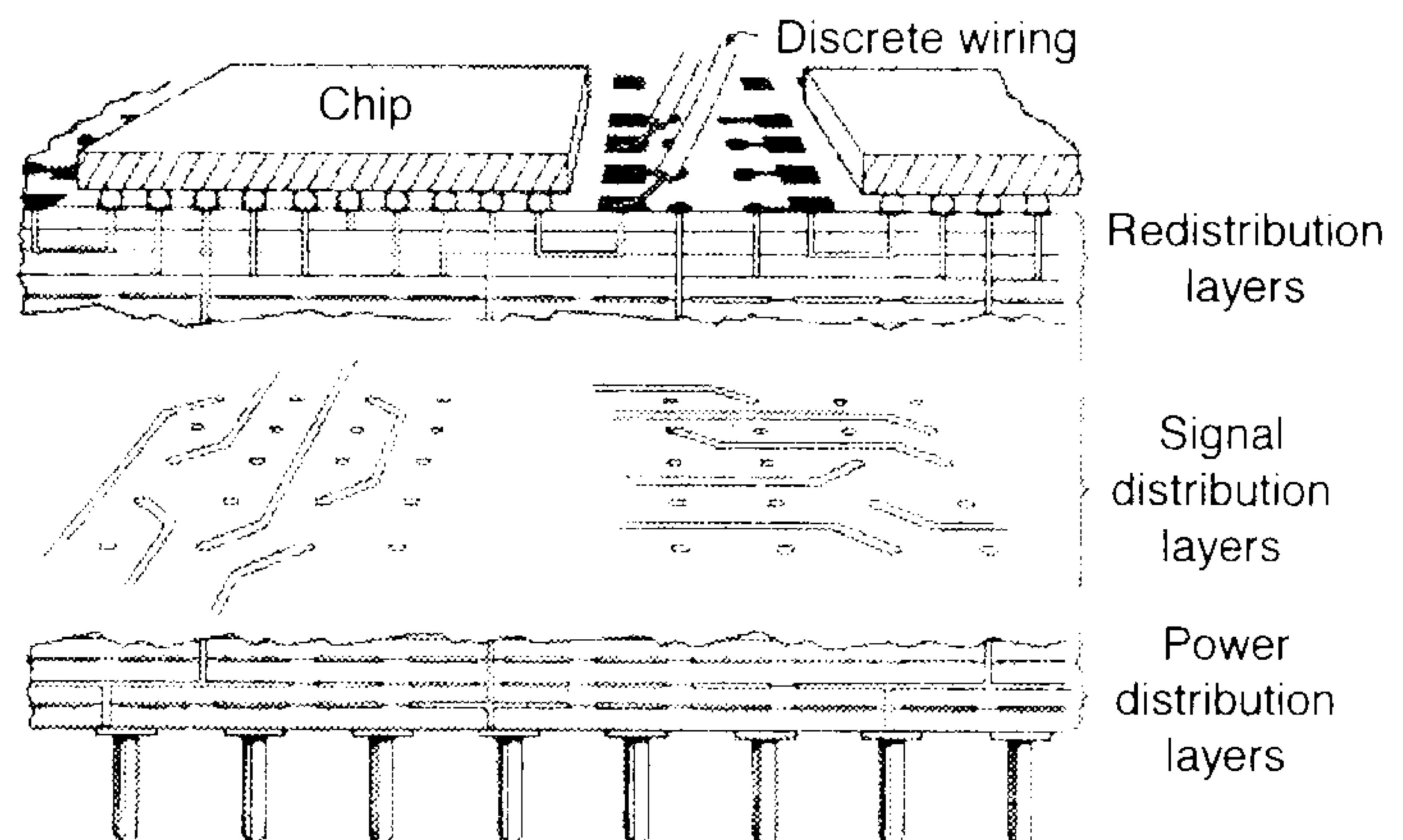

Fig. 4.47 Multi-layer co-fired ceramic substrate for a multi-chip module.

Most ceramic chip carriers are fabricated from alumina (Al_2O_3) with small amounts of additives such as glass, magnesium oxide and calcium oxide. The exact composition is considered proprietary information by the manufacturers. Other ceramic are often considered for applications in first level packaging including:

- Beryllium oxide (BeO) with its very high thermal conductivity; however, it is expensive and extremely toxic.
- Aluminum nitride exhibits better thermal conductivity than alumina, but it is brittle and fractures easily.
- Silicon carbide exhibits better thermal conductivity but is a conductor. It is used as a heat spreader in some IBM's multi-chip modules.
- Tungsten carbide is extremely hard and is used in fabricating cutting tools.
- Silicon nitride (Si_3N_4) is a high-temperature, high-toughness ceramic used in very high temperature applications.
- Boron nitride (BN), in its cubic crystal form, is used in substrates for high power components where its high thermal conductivity enables efficient heat dissipation.

4.3 CHIP CARRIER MANUFACTURING

Many manufacturing processes are employed in enclosing a chip in a first level package with its leads ready to be attached to a second level package. We will describe several of the processes in this section, and introduce some properties of the material employed.

4.3.1 Chip to Chip Carrier Mounting

The term 'die bonding' describes the operation of attaching the semiconductor die either to its chip carrier or to some substrate. The die is first picked from a separated wafer or waffle tray, aligned to a target pad on the carrier or substrate, and then permanently attached, usually by means of an inorganic solder or a particle filled epoxy adhesive. The requirements for the die bond include:

- It must not transmit significant stresses to the fragile chip during curing or during thermal cycling.
- It must provide excellent adhesion to both the chip and substrate materials without voids.
- It must withstand operational temperature without degrading or outgassing.
- It should exhibit good thermal conductivity to enhance heat transfer from the chip

The chip is bonded to the chip carrier to prevent any movement of the chip relative to its housing during the life of the product. Bonding methods vary considerably and depend on the type of chip carrier. Consider first a high-performance chip carrier fabricated from multi-layer ceramic. This carrier usually must meet stringent hermeticity requirements. Hence, it is essential that the bonding material used to attach the chip to the carrier maintain this hermeticity. In these ceramic housings, eutectic solder of gold and silicon (97.15% gold and 2.85% silicon) with a melting point of 363 °C or a silver filled glass are commonly as the bonding materials. Both the eutectic solder and the silver filled glass are inorganic and will not outgas making them ideal bonding agents in view of the hermeticity requirements. The eutectic solder of gold and silicon also exhibits a high thermal conductivity of 296 W/m-°C and aids in the transfer of heat from the chip to the case. The tensile strength of this solder is greater than 7,000 psi (48.3 MPa).

Other eutectic solders are also used for die attach to ceramic substrates such as a gold-tin alloy which is 80% gold and 20% tin with a melting point of 280°C (556°F). This alloy is lower in cost and its reflow temperature is also lower at 315-320°C. This alloy provides excellent wetting characteristics.