Sockets

Sockets are used to accommodate either chip carriers or cable connectors. Sockets are incorporated into a circuit design when chip replacement is probable. For example, a circuit being developed for a prototype system is likely to encounter several changes. In these cases, new chips housed in pin-grid-arrays can be substituted by inserting them into an appropriate socket. Sockets are also useful when chip replacement or repair is anticipated. High I/O count chips are difficult to remove from the circuit board because of the large number of leads that must be unsoldered simultaneously. Sockets can also be used to accommodate chip carriers with pins on circuit boards with surface mounted components. The socket illustrated in Fig. 4.16 shows receptacles on one side to accommodate pins and pads on the opposite side for surface mounting to a circuit board.

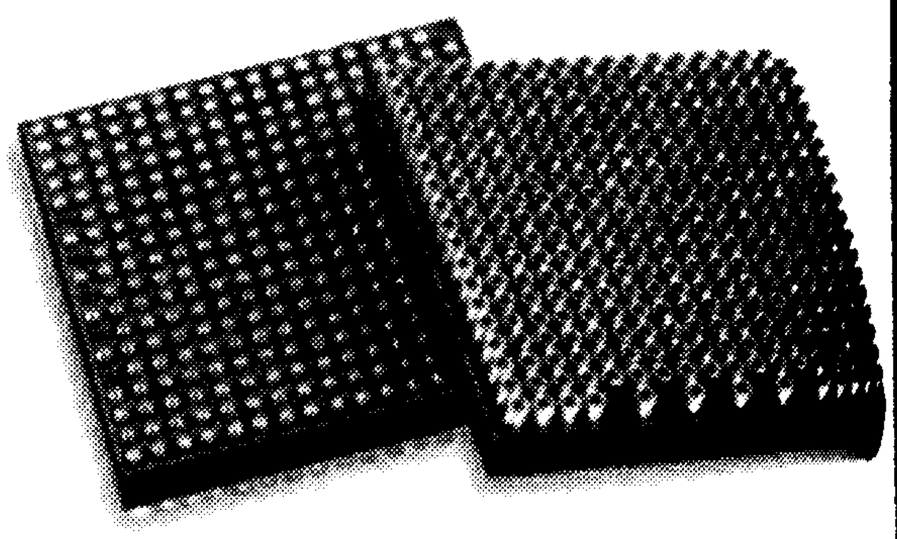

Fig. 4.16 Top and bottom views of a socket to accommodate pin-grid-arrays on a circuit board with only surface mounted components.

4.2.3 Surface Mounted Chip Carriers

A major distinction between types of chip carriers pertains to the type of leads used for the I/O emerging from the carrier. In addition to the pins used in through-hole mounting of chip carriers, three other types of leads are currently employed. The first is a J-lead intended for connection to the surface of the circuit board at a solder pad as shown in Fig 4.17.

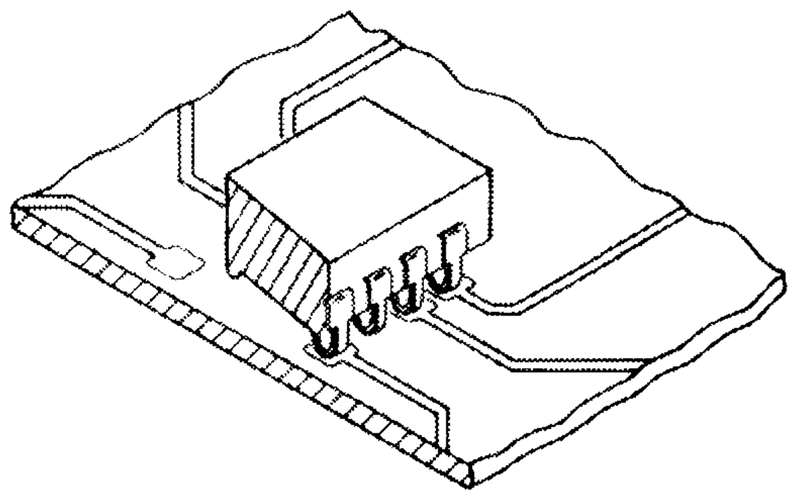

Fig. 4.17 Chip carrier with J-leads for surface mounting.

The second type is leadless, where metallized pads are provided on the chip carrier to provide soldering surfaces for connection to the circuit board. An illustration of this type of package is presented in Fig. 4.18.

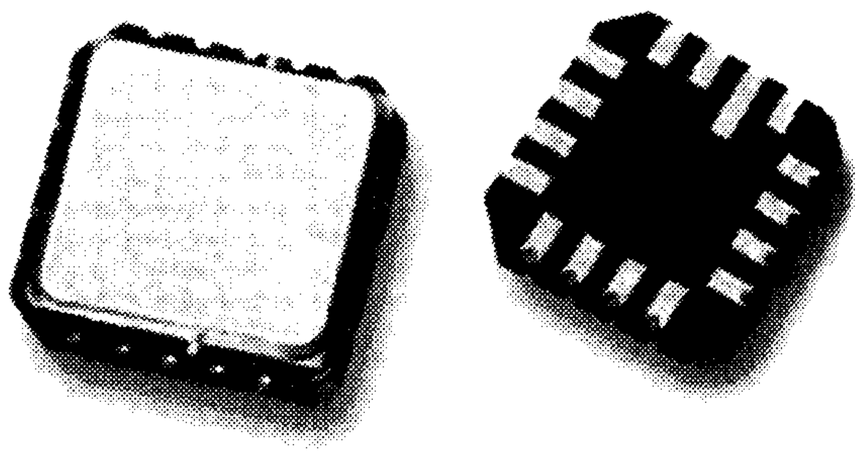

Fig. 4.18 Leadless chip carrier utilizes metallized pads for solder connections to the PCB.

The third type of chip carrier is the Ball-Grid-Array (BGA), where solder balls are deployed over the area of the bottom of the chip carrier to provide the connections to the PCB as indicated Fig. 4.19.

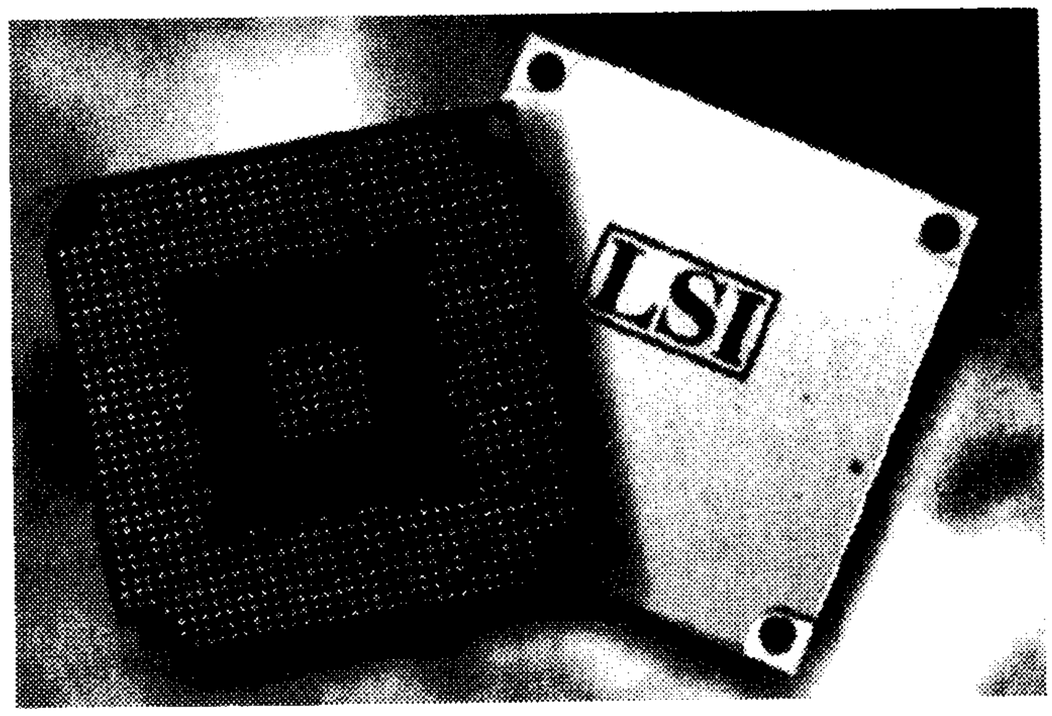

Fig. 4.19 A ball-grid array (BGA) chip carrier showing solder balls deployed on its bottom surface.

There are a very large number of surface mounted chip carriers in use today. They have been in use for several decades and the number and size of the packages have proliferated. We will describe many of these surface mounted packages in more detail in the following subsections.

Discrete Device Packages

There are still many products developed that require small chips or passive devices such as resistors. These devices typically have a very low I/O count and are housed in Small-Outline Transistor (SOT) packages. Usually only one transistor on a small (30 × 30 mil) chip is encapsulated in an SOT. The power to be dissipated is small—typically less than 0.5 W. An example of a three lead plastic encapsulated SOT is presented in Fig. 4.20. Note in this case the leads are the gull wing type.

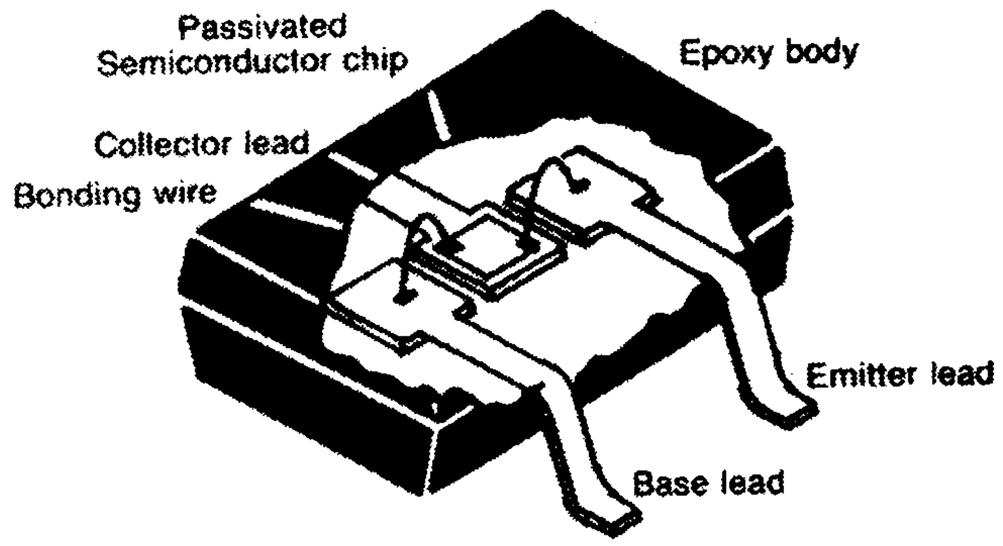

Fig. 4.20 Small outline transistor (SOT) package.

Discrete devices with higher power levels (greater than 1 W) are packaged in DPACKs. As shown in Fig. 4.21, the DPACK incorporates a heavy slug of copper that enhances the heat flow from the chip to the environment. Note a hole is provided in the copper slug so it can be bolted to a suitable heat sink. Silicon control rectifiers and power transistors, which require significant quantities of heat to be dissipated, are often housed in DPACKs.

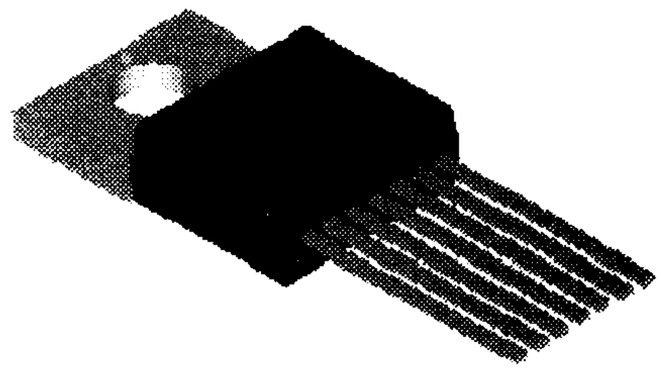

Fig. 4.21 DPACK package for discrete devices with high heat dissipation requirements.

Small Outline Packages

One version of the small outline integrated circuit (SOIC) chip carrier is shown in Fig. 4.22. This package is similar to the DIP in that it incorporates leads deployed along both sides of the package; however, it differs in that the leads centers vary from 20 to 50 mils (0.5 to 1.27 mm) rather than the 100 mil (2.54 mm) centers found on the standard DIP. For some designs, the leads are shaped like gull wings and soldered to the pads on the PCB as indicated in Fig. 4.23. When placed on the PCB, the SOICs are held in place by the adhesion of the solder paste on the bonding pads or by a drop of epoxy that is placed under the chip carrier. All of the connections are soldered simultaneously in a soldering process. Surface tension in the melted solder assisting in aligning the gull wing leads with the bonding pads on the PCB.

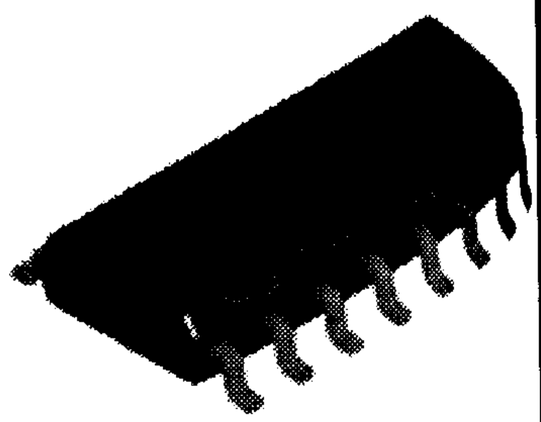

Fig. 4.22 Gull wing configuration on a SOIC chip carrier.

Another surface mounted chip carrier is available which incorporates a J lead on 50 mil (1.27 mm) centers. This chip carrier, known as the small outline J (SOJ), is illustrated in Fig. 4.24. The J lead configuration, which essentially folds the lead into a small pocket on the underside of the package, reduces lead deformations during shipping and handling. The J lead is fully configured for assembly. It is possible to position the packages on the board, bond them with solder paste and make all of the solder joints simultaneously by using either a vapor phase or IR reflow soldering process. The J lead with a pocket protecting the lead and the solder joint connecting the lead to the circuit board pad is shown in Fig. 4.25. Clearly the J leaded chip carrier is superior to the conventional DIP in designs involving high I/O count chips. One disadvantage of the J-lead new package is the difficulty in maintaining all of the curved leads in the same plane so that all of the leads are in contact with the pads on the PCB prior to soldering.

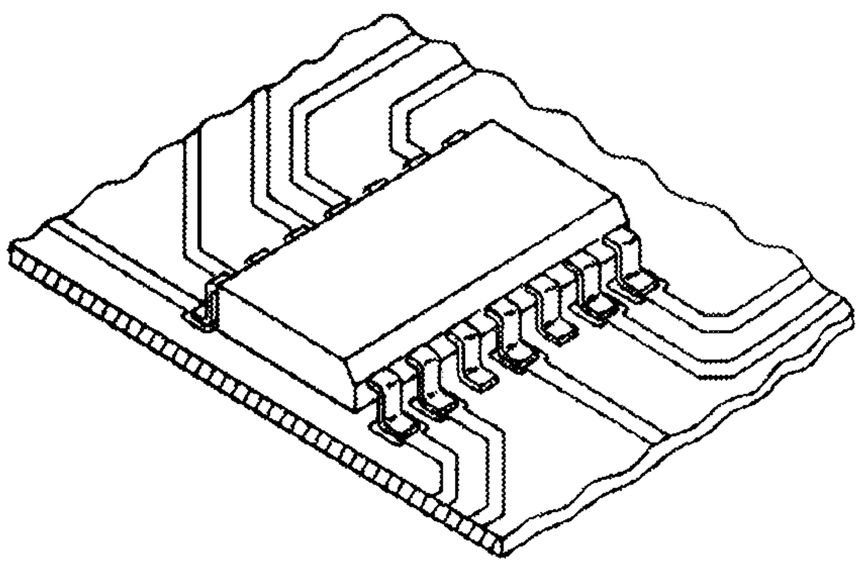

Fig. 4.23 Surface mounting of a SOIC package onto a PCB.

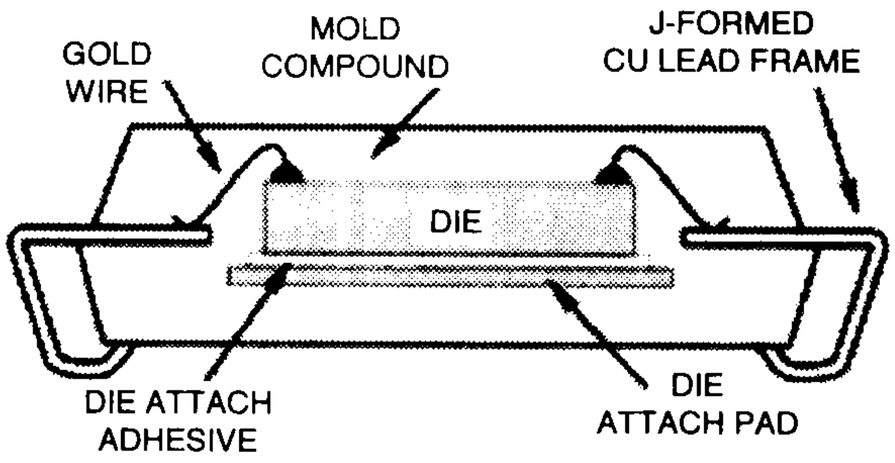

Fig. 4.24 Construction details of the SOJ—a J-leaded chip carrier.

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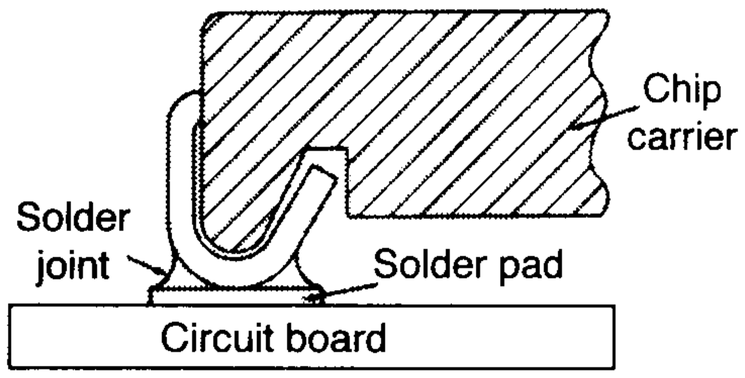

Fig. 4.25 Cross section of a J lead package showing the pocket protecting its lead, and the solder joint connecting the lead to the solder pad on the PCB.

Quad Flat Packs

With surface mounted chip carriers, the leads from the package are soldered to pads that are formed on the top surface of the circuit card as indicated in Fig. 4.17. The fact that a hole is not necessary to accommodate the mounting of the lead wire permits the leads to be placed on closer centers enabling the design of more area efficient chip carriers. With chip I/O count increasing and efficient use of circuit board area becoming more important, the advantages of surface mounting with its smaller package size has lead to many new developments in first level packaging.

The major advantage of the quad flatpack, shown in Fig. 4.26, is its relatively small size compared to DIP with the same I/O count. Because the leads are on closer centers and on all four sides, the quad flatpack is nearly four times as efficient as the DIP in utilization of circuit board real estate. Quad flatpacks have the advantage of reducing the size of second and third level packaging and improved electrical performance due to shorter lead length.

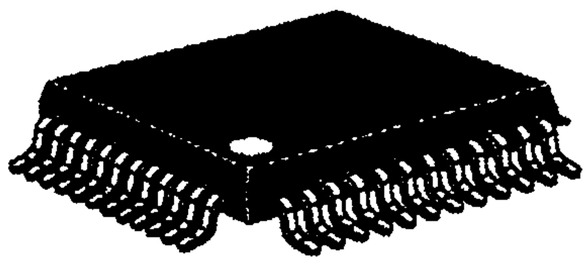

Fig. 4.26 A quad flatpack with gull wing leads on four sides.

The quad flatpack requires care in handling during the production process. Its leads are only 3 to 6 mils (0.076 to 0.15 mm) thick; hence, they are fragile and must be protected to prevent damage or misalignment during assembly. The plastic quad flatpack (PQFP) was developed to provide better protection for its leads. Its design incorporates corner bumpers that extend beyond the leads to provide some degree of protection. The PQFP is intended for low-cost, high-lead count applications. The small lead-pitch of a PQFP enables this design to accommodate higher lead count chips than possible in PDIP, PLCC, and SOIC packages. The lead pitch of the PQFP varies from 15 to 40 mil (0.4 to 1.0 mm) depending on lead count and package size. When the benefits of the PQFP package configuration were realized, the design was extended to lower lead counts. Lead counts ranging from 44 to 304 are now commercially available. In manufacturing this package, the chip is bonded to the die pad of a lead frame, and then wire bonding or TAB is used to complete the connections between the perimeter pads on the chip and the fingers on the lead frame. A silica-filled epoxy is injection-molded to encapsulate the device, bonding wires and lead frame. The leads are trimmed and formed in a gull-wing formation. A drawing of a 100 lead PQFP is presented in Fig. 4.27.

Fig. 4.27 Drawing of a 100 lead PQFP with a 25 mil (0.63 mm) lead pitch.

Quad Flat J Packages

The quad flat J type chip carrier, sometimes referred to as (PLCC), is illustrated in Fig. 4.28. This drawing shows J shaped leads on all four sides of the chip carrier. The leads are on 50 mil (1.27 mm) centers and packages are available with lead counts of 18, 20, 28, 32, 44, 52, 68 and 84. Higher lead counts in larger packages are not possible because the flatness of the packages (and the circuit boards) cannot be control closely enough to insure that all of the leads contact the solder pads. Simultaneous contact of the leads to the solder pads is essential to insure quality solder joints.

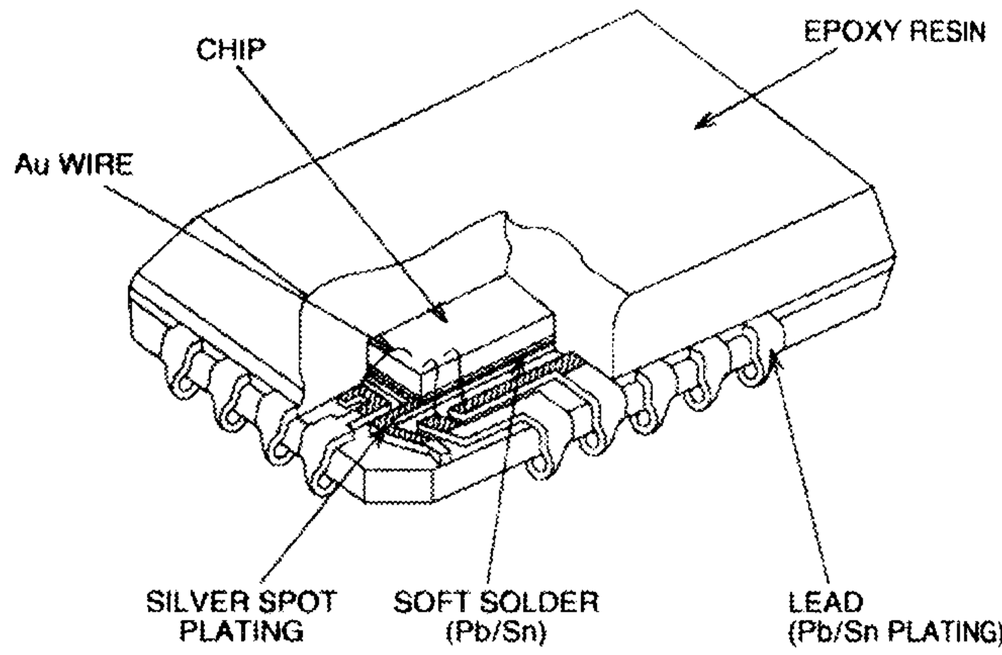

Fig. 4.28 Drawing showing fabrication details of a quad flat J chip carrier.

The J-leaded chip carriers cannot be used to house very high I/O count chips; however, they are much easier to handle than the fine pitch gull wing type chip carriers.

Thin Small Outline Package (TSOP)

Recent developments of portable electronic products such as cell phones, music recorders and cameras have driven the design of thin small outline package (TSOP) to house certain types of chips. A typical example of a Type I package[3] is presented in Fig. 4.29. These are surface mounted chip carriers with gull wing leads. The lead pitch is usually 20 mil (0.5 mm).

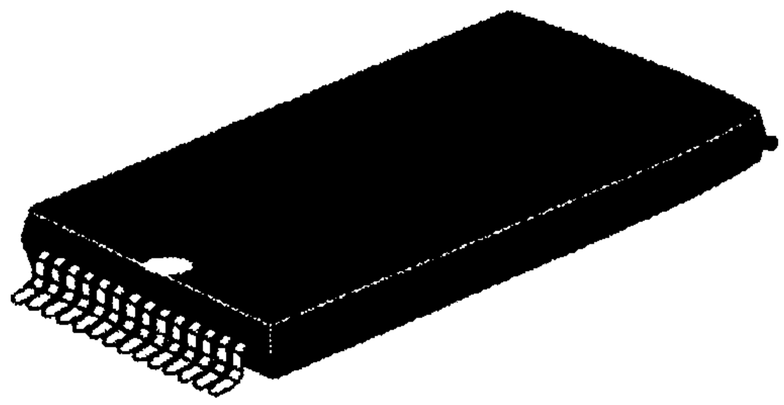

Fig. 4.29 Example of a thin small outline package (TSOP) used to house a flash memory chip.

Size and weight are very important design considerations in developing portable electronic products. Smaller and lighter chip carriers are demanded. To meet this demand, the manufacturers developed a thin chip carrier to reduce the height required above the printed circuit board. They also reduced the pitch of the leads to reduce the area required on the circuit board. An example of a height reduction of four to one afforded by the TSOP compared to a PQFP is shown in Fig. 4.30.

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[3] Type I packages have leads extending from their shorter side and Type II packages have leads extending from their longer side.

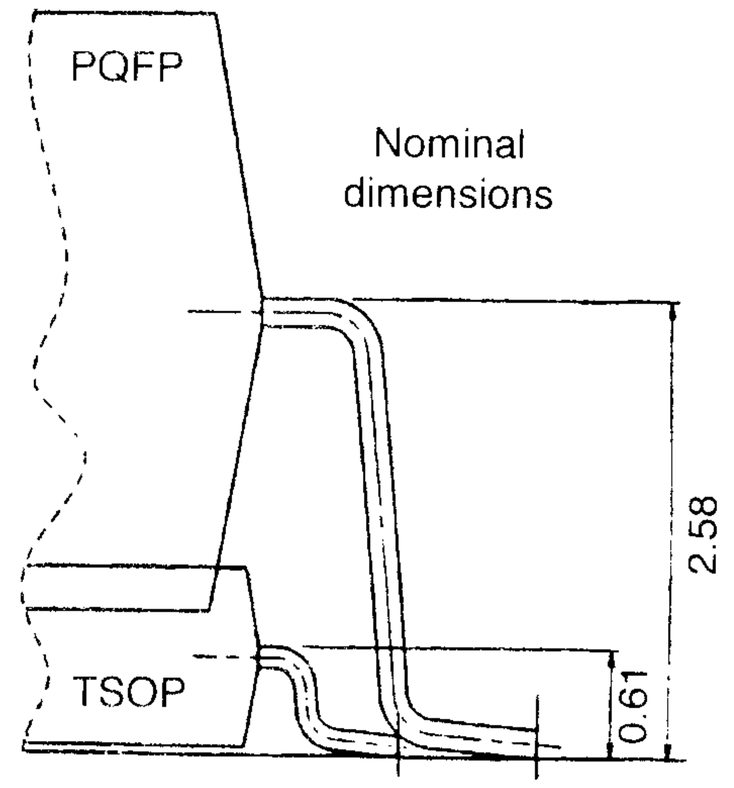

Fig. 4.30 Height reduction achieved in the dimension above a circuit board by using TSOP chip carriers instead of PQFP chip carriers.

4.2.4 Leadless Surface Mounted Chip Carriers

Leads from a chip carrier are a nuisance because they are fragile and easily deformed in shipping and handling. It is possible to eliminate the leads entirely by replacing them with metallized pads fixed directly on the chip carrier as shown in Fig. 4.18. These metallized pads are usually on 50 mil (1.27 mm) centers and provide an area efficient chip carrier. The pads on the chip carrier are connected to corresponding pads on the circuit board by using solder paste that is melted in a soldering process described more completely in Chapter 6.

The area efficiency of the leadless chip carrier is mitigated by a very serious disadvantage involving solder joint failure. The circuit board assembly is subjected to large thermally induced strains due to a mismatch of the coefficients of expansion of the chip carrier and the circuit board materials. Thermal cycling may be encountered in operation due to power on power off, or thermal cycles may be imposed as a manufacturing screening test or in qualification testing. During these thermal cycles, the solder joints are exposed to thermally induced shearing strain of relatively large magnitude. The effect of this strain is to induce fatigue failures of the solder joints. The failures begin with the solder joints located at the corners of the chip carrier and then move inward to more centrally located solder joints. The number of thermal cycles required to initiate fatigue failure depends on the temperature extremes involved in the thermal cycling, the rate of temperature change, the mismatch in the coefficients of thermal expansion and the size of the chip carrier.

4.2.5 Solder Ball Surface Mounted Chip Carriers

Ball-grid-array

The ball-grid-array (BGA), shown in Fig. 4.19, is similar to the pin-grid-array (PGA) except that solder balls have been deployed on its bottom surface instead of pins. The BGA solder balls have a distinct advantage over the PGA's pins in that they can be placed on much closer centers. The solder ball-grid-array on the underside of the package is used to connect the chip carrier to the PCB substrate. The grid spacings have been standardized under JEDEC guidelines. The most commonly used grid spacings are 32, 40 and 50 mil (0.8, 1.0, and 1.27 mm), although finer pitches are sometimes employed in BGA designs. Solder ball diameter varies from 20 to 35 mil (0.50 to 89 mm). With flip chip connections, a

typical commercially available BGA with a 45 mm square body supports a 44 × 44 array of solder balls to provide an I/O count[4] of 1728.

There are many BGA packages, but the die for all types is connected to its substrate by the wire or TAB bonding, illustrated in Fig. 4.31, or by the flip–chip direct attachment that is shown in Fig. 4.32. BGA is often the package of choice for optimizing device electrical performance. They are lightweight, thin with short connections, and they minimize the use of board space.

A schematic illustration of a two-layer, plastic-encapsulated PBGA showing many of the design features of this first level package is presented in Fig. 4.31. The chip is connected to the wiring pads on the package substrate with gold wires. Wiring connections are made using vias which carry the signals from one layer to another in the substrate. Solder balls bonded to the bottom surface of the substrate are then used to connect the PBGA to the printed circuit board in a solder reflow operation. The diameter of the solder balls depend upon their pitch, with diameters that are 50 to 60% of the pitch dimension. The number of I/O in commercially available PBGAs depends on the pitch and the size of the chip carrier. For example, a 40 mm square PBGA with a 50 mil (1.27 mm) pitch is available with 564 I/O and a 35 mm square PBGA with a 40 mil (1.0 mm) pitch is available with 1156 I/O.

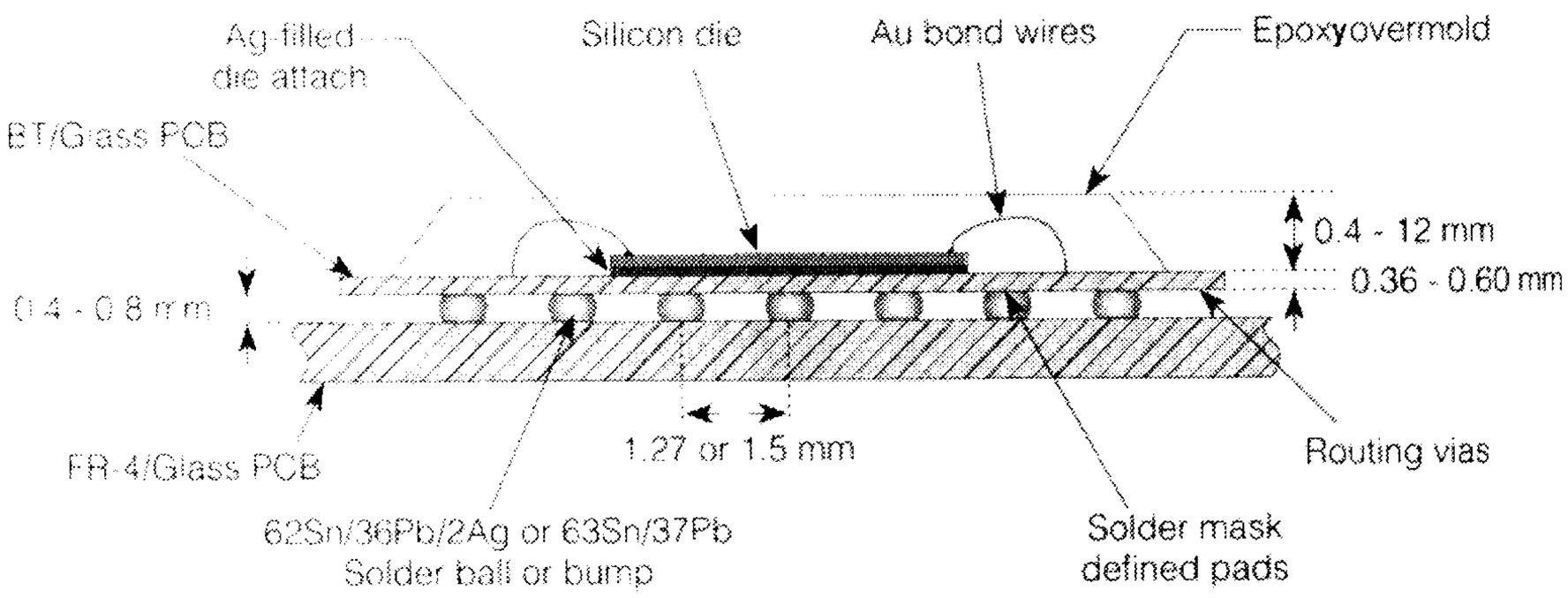

Fig. 4.31 Schematic illustration of wire bonding connections in a two-layered PBGA.

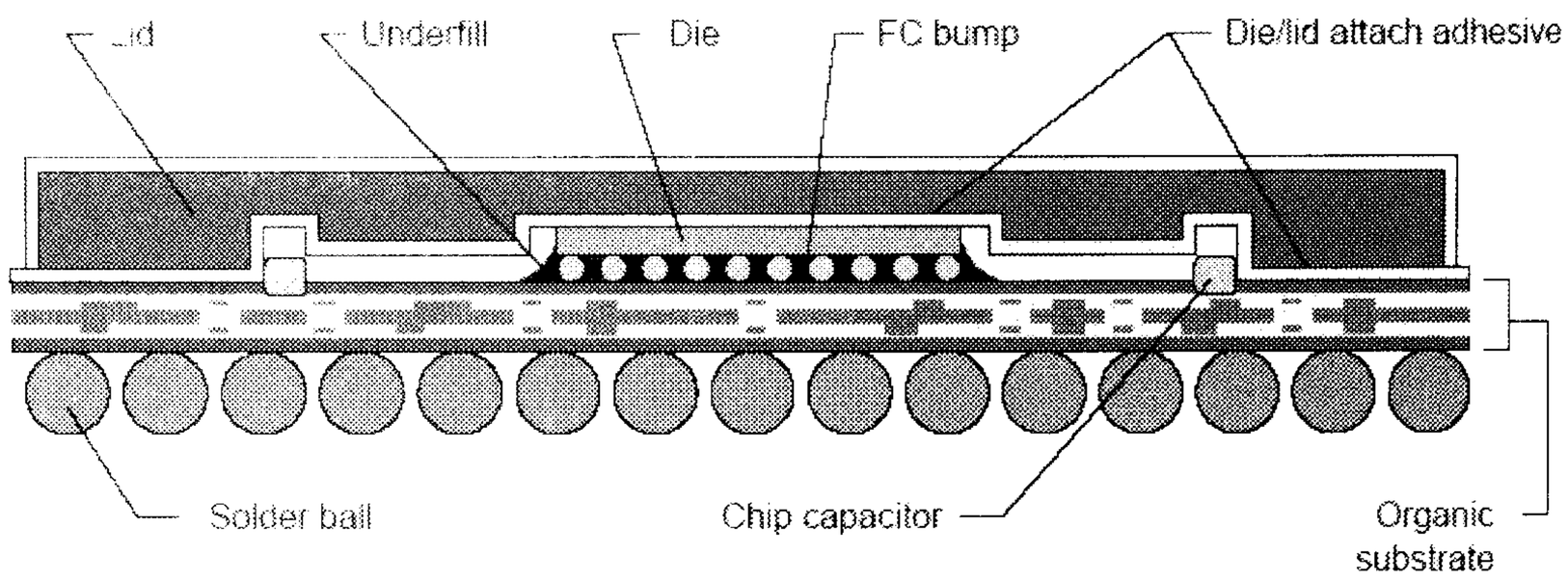

Fig. 4.32 Schematic illustration of flip chip C4 connections in a four-layered BGA.

[4] An array of 44 × 44 solder balls yields an I/O count of 1936. The lower number cited here reflects the fact that the solder balls under the chip were omitted in this design.